



Zero-Delay Clock Buffer

- Maximum rated frequency: 140 MHz
- Low cycle-to-cycle jitter
- Input to output delay, less than 150ps
- External feedback pin allows outputs to be synchronized to the clock input
- 5V tolerant input*
- Operates at 3.3V V_{DD}
- Test mode allows bypass of the PLL for system testing purposes (e.g., IBIS measurements)
- Clock frequency multipliers ½x to 4x dependent on option
- Packages (Pb-free and Green available):
 - 16-pin, 150-mil SOIC (W)
 - 16-pin 173-mil TSSOP (L)

Input Select Decoding for PI6C2408 (-1, -1H, -4)

SEL2	SEL1	OUTA [1-4]	OUTB [1-4]	Output Source	PLL
0	0	3-State	3-State	PLL	OFF
0	1	PLL	3-State	PLL	ON
1	0	CLKIN	CLKIN	CLKIN	OFF
1	1	PLL	PLL	PLL	ON

Input Select Decoding for PI6C2408 (-2, -3)

SEL2	SEL1	OUTA [1-4]	OUTB [1-4]	Output Source	PLL
0	0	3-State	3-State	PLL	OFF
0	1	PLL	3-State	PLL	ON
1	0	CLKIN	CLKIN/2	CLKIN	OFF
1	1	PLL	PLL	PLL	ON

Input Select Decoding for PI6C2408-6

SEL2	SEL1	OUTA [1-4]	OUTB [1-4]	Output Source	PLL
0	0	3-State	3-State	PLL	OFF
0	1	CLKIN	CLKIN/2	CLKIN	OFF
1	0	PLL	PLL	PLL	ON
1	1	PLL	PLL/2	PLL	ON

PI6C2408 Configurations

Device	Feedback From	OUTA [1-4] Frequency	OUTB [1-4] Frequency
PI6C2408-1	OUTA or OUTB	CLKIN	CLKIN
PI6C2408-1H	OUTA or OUTB	CLKIN	CLKIN
PI6C2408-2	OUTA	CLKIN	CLKIN/2
PI6C2408-2	OUTB	2X CLKIN	CLKIN
PI6C2408-3	OUTA	2X CLKIN	CLKIN or $\overline{\text{CLKIN}}$ ⁽¹⁾
PI6C2408-3	OUTB	4X CLKIN	2X CLKIN
PI6C2408-4	OUTA or OUTB	2X CLKIN	2X CLKIN
PI6C2408-6	OUTA	CLKIN	CLKIN or CLKIN/2
PI6C2408-6	OUTB	CLKIN or 2X CLKIN	CLKIN

Note:

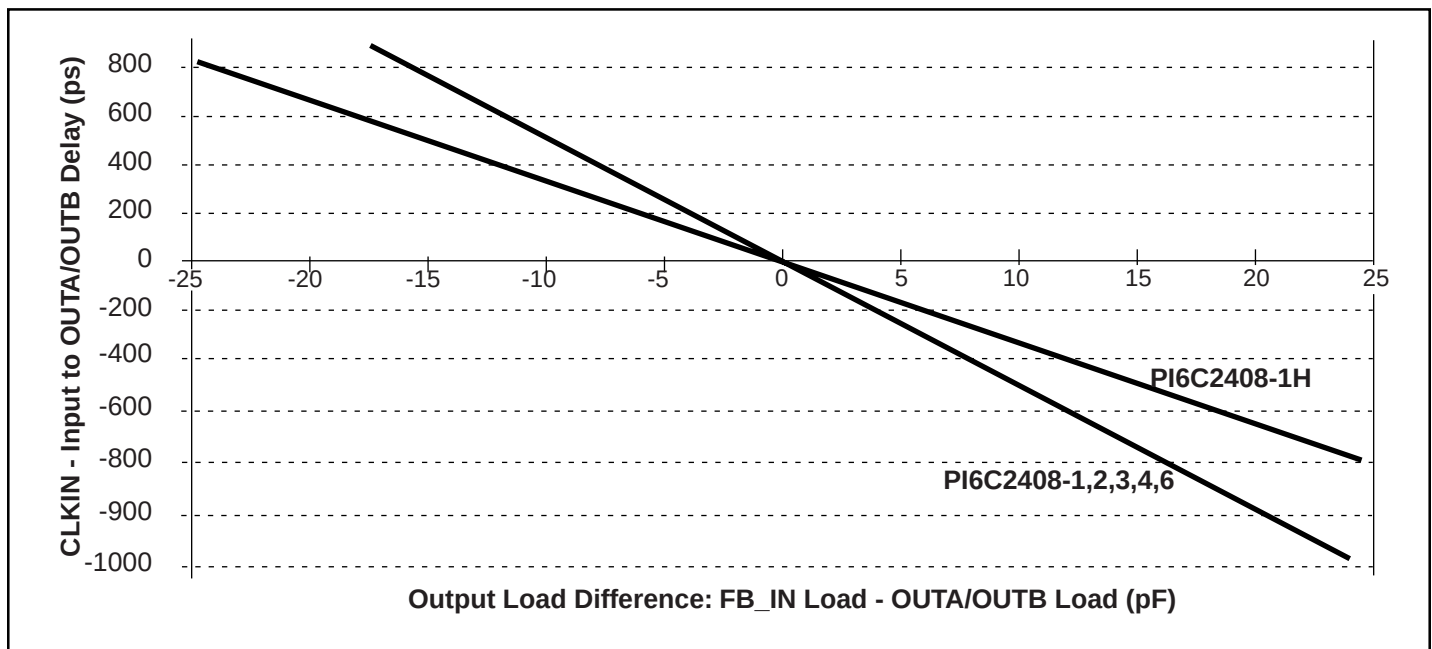
1. Output phase is indeterminant (0° or 180° from CLKIN)

Pin Description

Pin	Signal	Description
1	CLKIN	Input clock reference frequency (weak pull-down)
2, 3, 14, 15	OUTA[1-4]	Clock output, Bank A (weak pull-down)
4, 13	V _{DD}	3.3V supply
5, 12	GND	Ground
6, 7, 10, 11	OUTB[1-4]	Clock output, Bank B (weak pull-down)
8	SEL2	Select input, bit 2 (weak pull-up)
9	SEL1	Select input, bit 1 (weak pull-up)
16	FB_IN	PLL feedback input

Zero Delay and Skew Control

CLKIN Input to Output Bank Delay vs. Difference in Loading between FB_IN pin and OUTA/OUTB pins



The relationship between loading of the FB_IN signal and other outputs determines the input-output delay. Zero delay is achieved when all outputs, including feedback, are loaded equally.

Maximum Ratings

Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage (Except CLKIN)	-0.5V to V _{DD} +0.5V
DC Input Voltage CLKIN	-0.5 to 7V
Storage Temperature	-65°C to +150°C
Maximum Soldering Temperature (10 seconds)	260°C
Junction Temperature	150°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000V

Operating Conditions ($V_{CC}=3.3V\pm0.3V$)

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Commerical Operating Temperature	0	70	°C
	Industrial Operating Temperature	-40	85	
C_L	Load Capacitance, below 100 MHz	—	30	pF
	Load Capacitance, from 100 MHz to 140MHz	—	15	
C_{IN}	Input Capacitance	—	7	

DC Electrical Characteristics for Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		
I_{IL}	Input LOW Current	$V_{IN} = 0V$		50.0	μA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	
V_{OL}	Output LOW Voltage	$I_{OL} = 8mA (-1, -2, -3, -4, -6); I_{OL} = 12mA (-1H)$		0.4	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -8mA (-1, -2, -3, -4, -6); I_{OH} = -12mA (-1H)$	2.4		
I_{DD} (PD mode)	Pwr Dwn Supply Current	SEL1 = 0 (-1, -2, -3, -4, -1H); SEL2 = 0 (-6)		25.0	μA
I_{DD}	Supply Current	Unloaded outputs 100 MHz, Select inputs at V_{DD} or GND		54.0	mA
				70.0 (-1H)	
		Unloaded outputs 66 MHz, CLKIN, except (-1H)		39.0	
		Unloaded outputs 33MHz, CLKIN, except (-1H)		20.0	

AC Electrical Characteristics for Industrial Temperature Devices

Parameters	Name	Test Conditions	Min.	Typ.	Max.	Units
F _O	Output Frequency	30pF load	10.0		100	MHz
		15pF load			140	
t _{DC}	Duty Cycle ⁽¹⁾ (-1, -2, -3, -4, -6)	Measured at V _{DD} /2, F _{OUT} <66.67MHz 30pF load	40.0	50	60.0	%
		Measured at V _{DD} /2, F _{OUT} <140 MHz 15pF load				
		Measured at V _{DD} /2, F _{OUT} <45 MHz 30pF load	45.0		55.0	
	Duty Cycle ⁽¹⁾ (-1H)	Measured at V _{DD} /2, F _{OUT} <66.67MHz 30pF load	45.0		60.0	
		Measured at V _{DD} /2, F _{OUT} <140 MHz 15pF load	40.0		55.0	
		Measured at V _{DD} /2, F _{OUT} <45MHz 30pF load	45.0			
t _R	Rise Time ⁽¹⁾ (-1, -2, -3, -4,)	Measured between 0.8V and 2.0V, 30pF load			2.2	ns
		Measured between 0.8V and 2.0V, 15pF load			1.50	
	Rise Time ⁽¹⁾ (-1H)	Measured between 0.8V and 2.0V, 30pF load			1.50	
t _F	Fall Time ⁽¹⁾ (-1, -2, -3, -4,)	Measured between 0.8V and 2.0V, 30pF load			2.50	
		Measured between 0.8V and 2.0V, 15pF load			1.50	
	Fall Time ⁽¹⁾ (-1H)	Measured between 0.8V and 2.0V, 30pF load			1.25	
t _{SK(O)}	Output to Output Skew within same Bank (-1,-2,-3,-4,-6) ⁽¹⁾	All outputs equally loaded			200	ps
	OUTA to OUTB Skew ⁽¹⁾ (-1,-1H,-4)					
	OUTA to OUTB Skew ⁽¹⁾ (-2,-3,-6)				400	
t ₀	Delay, CLKIN Rising Edge to FB_IN Rising Edge ⁽¹⁾	Measured at V _{DD} /2		0	±150	
t _{SK(D)}	Device-to-Device Skew ⁽¹⁾	Measured at V _{DD} /2 on FB_IN pins of devices		0	500	
t _{SLEW}	Output Slew Rate ⁽¹⁾	Measured between 0.8V & 2.0V on -1H device using Test Crt #2	1			V/ns
t _{JIT}	Cycle-to-Cycle Jitter ⁽¹⁾ (-1,-1H,-4)	Measured at 66.67 MHz, loaded 30pF load			200	ps
		Measured at 140 MHz, loaded 15pF load			100	
	Cycle-to-Cycle Jitter ⁽¹⁾ (-2,-3,-6)	Measured at 66.67 MHz, loaded 30pF load			400	
t _{LOCK}	PLL Lock Time ⁽¹⁾	Stable power supply, valid clocks presented on CLKIN and FB_IN pins			1.0	ms

Notes:

1. See Switching Waveforms on page 7.

DC Electrical Characteristics for Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Units
V _{IL}	Input LOW Voltage	—	—	0.8	V
V _{IH}	Input HIGH Voltage	—	2.0	—	
I _{IL}	Input LOW Current	V _{IN} = 0V	—	50	μA
I _{IH}	Input HIGH Current	V _{IN} = V _{DD}	—	100	
V _{OL}	Output LOW Voltage	I _{OL} = 8mA (–1, –2, –3, –4, –6); I _{OL} = 12mA (–1H)	—	0.4	V
V _{OH}	Output HIGH Voltage	I _{OH} = –8mA (–1, –2, –3, –4, –6); I _{OH} = –12mA (–1H)	2.4	—	
I _{DD} (PD mode)	Power Down Supply Current	SEL1 = 0 (–1, –2, –3, –4, –1H); SEL2 = 0 (–6)	—	12	μA
I _{DD}	Supply Current	Unloaded outputs, 66.67 MHz, Select inputs at V _{DD} or GND	—	39	mA
I _{DD}	Supply Current	Unloaded outputs 100 MHz Select Inputs @ V _{DD} or GND	—	54	

AC Electrical Characteristics for Commercial Temperature Device

Parameters	Name	Test Conditions	Min.	Typ.	Max.	Units
F _O	Output Frequency	30pF load	10		100	MHz
		15pF load			140	
t _{DC}	Duty Cycle ⁽¹⁾ (–1H)	Measured at V _{DD} /2, for high drive output	45	50	55	%
	Duty Cycle (–1, –2, –3, –4, –6)	Measured at V _{DD} /2, for normal drive output	40	50	60	
t _R	Rise Time ⁽¹⁾ @30pF	Measured between 0.8V and 2.0V			2.2	ns
	Rise Time ⁽¹⁾ @15pF				1.5	
	Rise Time ⁽¹⁾ @30pF (–1H)				1.5	
t _F	Fall Time ⁽¹⁾ @30pF				2.2	
	Fall Time ⁽¹⁾ @15pF				1.5	
	Fall Time ⁽¹⁾ @30pF (–1H)				1.25	
t _{SK(O)}	Output to Output Skew ⁽¹⁾ within same bank (–1, –1H, –2, –3, –4, –6)	All outputs equally loaded, V _{DD} /2			200	ps
	OUTA to OUTB Skew ⁽¹⁾ (–1, –1H, –4)	All outputs equally loaded, V _{DD} /2			200	
	OUTA to OUTB Skew ⁽¹⁾ (–2, –3, –6)	All outputs equally loaded, V _{DD} /2			400	
t ₀	Input to Output Delay, CLKIN Rising Edge to FB_IN Rising Edge ⁽¹⁾	Measured at V _{DD} /2		0	±150	
t _{SK(D)}	Device to Device Skew ⁽¹⁾	Measured at V _{DD} /2 on FB_IN pins of devices		0	500	
t _{SLEW}	Output Slew Rate ⁽¹⁾	Measured between 0.8V and 2.0V on –1H device using Test Circuit #2	1			V/ns
t _{JIT}	Cycle-to-Cycle Jitter ⁽¹⁾ (–1, –1H, –4)	Measured at 66.67 MHz, loaded 30pF outputs			200	ps
		Measured at 140 MHz, loaded 15pF outputs			100	
	Cycle-to-Cycle Jitter ⁽¹⁾ (–2, –3, –6)	Measured at 66.7 MHz, loaded 30pF outputs			400	
t _{LOCK}	PLL Lock Time ⁽¹⁾	Stable power supply, valid clocks presented on CLKIN and FB_IN pins			1.0	ms

Notes:

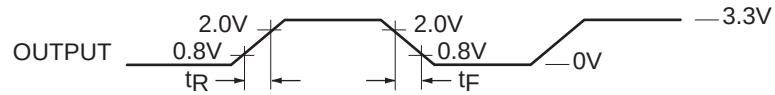
1. See Switching Waveforms on page 7.

Switching Waveforms

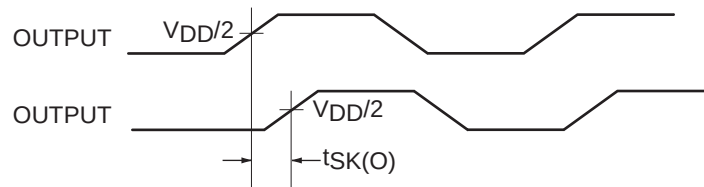
Duty Cycle Timing



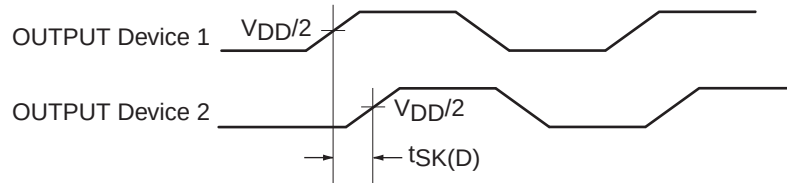
All Outputs Rise/Fall Time



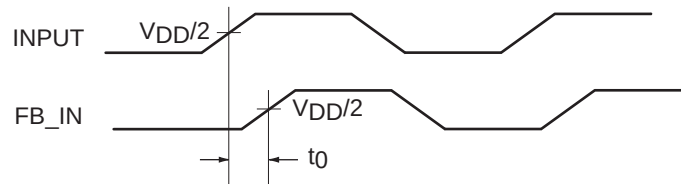
Output-Output Skew



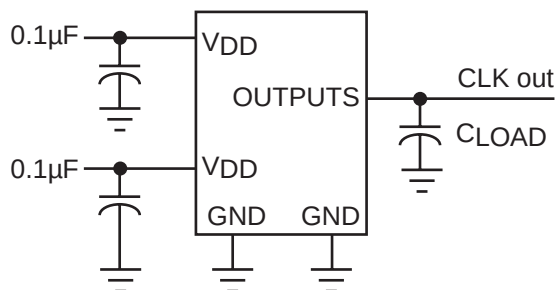
Device-Device Skew



Input-Output Propagation Delay

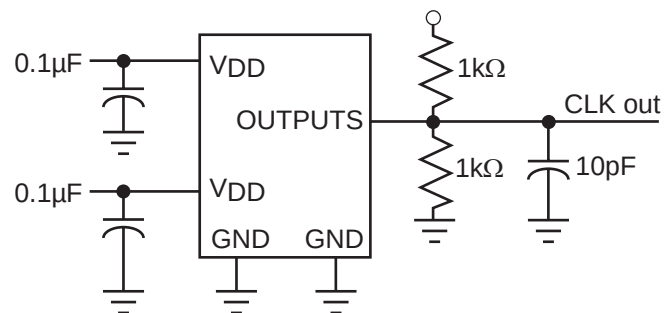


Test Circuit 1



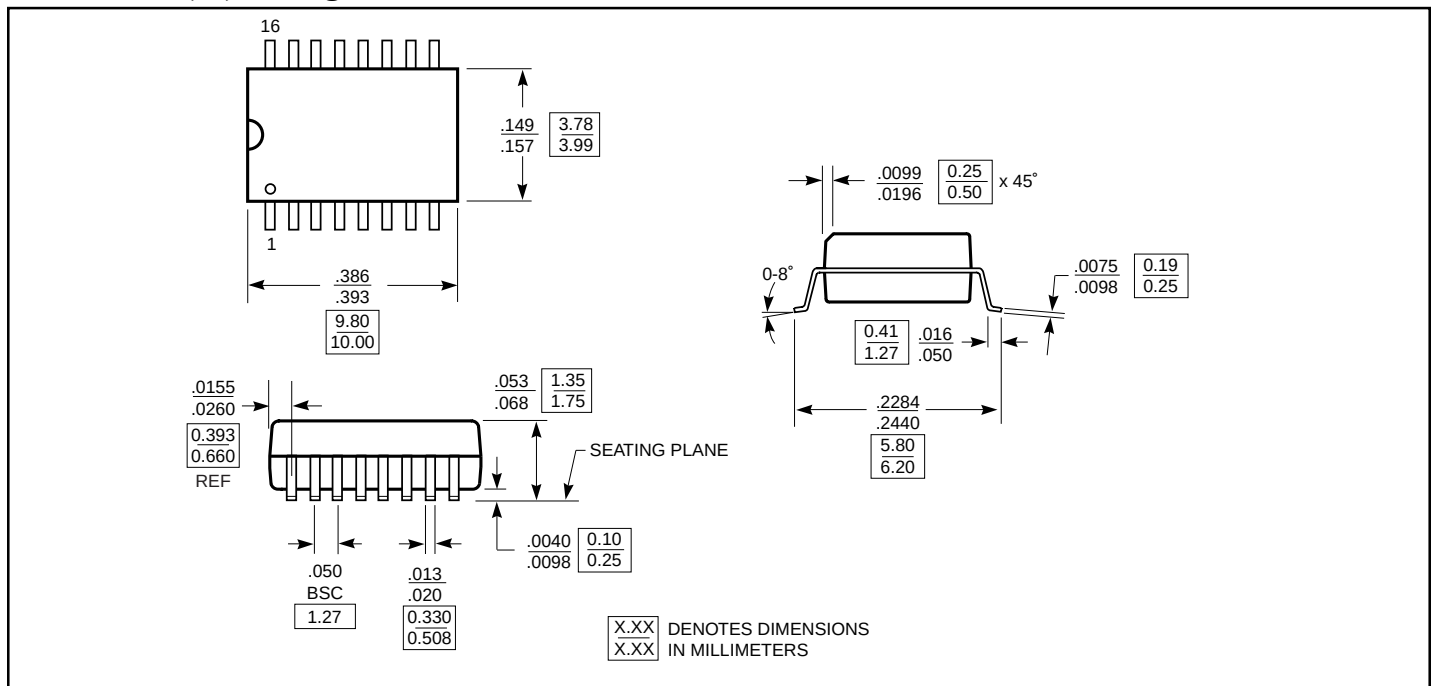
Test Circuit for all parameters except t_{SLEW}

Test Circuit 2

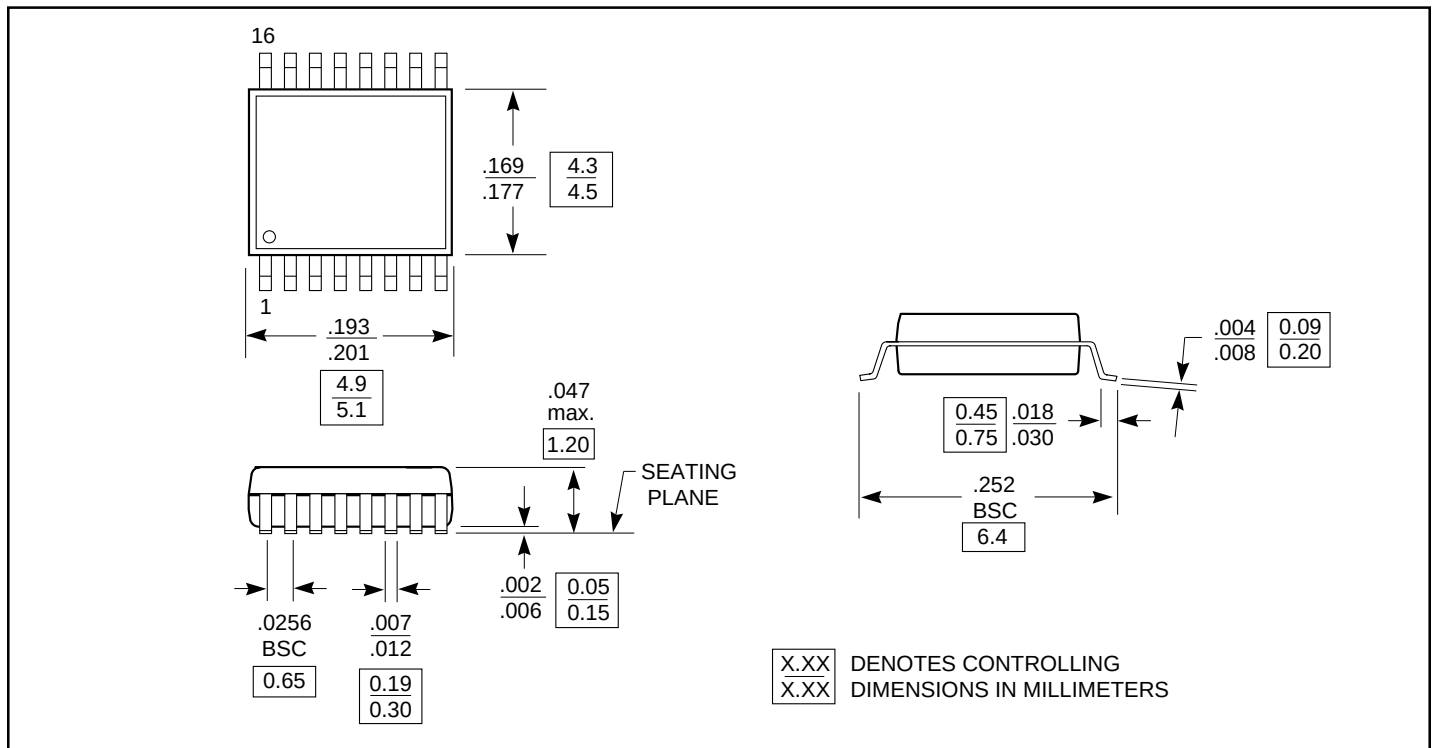


Test Circuit for t_{SLEW} , Output slew rate on -1H device

16-Pin SOIC (W) Package



16-Pin TSSOP (L) Package



Note: Controlling dimensions in millimeters. Ref: JEDEC MS -012 AC

Ordering Information (Commercial Temperature Device)

Ordering Code	Package Code	Package Type	Operating Range
PI6C2408-1W	W16	16-pin 150-mil SOIC	Comercial
PI6C2408-1HW			
PI6C2408-2W			
PI6C2408-3W			
PI6C2408-4W			
PI6C2408-6W			
PI6C2408-1WE		Pb-free and Greem 16-pin 150-mil SOIC	
PI6C2408-1HWE			
PI6C2408-1L	L16	16-pin 173-mil TSSOP	
PI6C2408-1HL			
PI6C2408-3L			
PI6C2408-4L			

Ordering Information (Industrial Temperature Device)

Ordering Code	Package Code	Package Type	Operating Range
PI6C2408-1WI	W16	16-pin 150-mil SOIC	Industrial
PI6C2408-1HWI			
PI6C2408-2WI			
PI6C2408-4WI			
PI6C2408-6WI			
PI6C2408-1LI	L16	16-pin 173-mil TSSOP	
PI6C2408-6LI			
PI6C2408-1LE		Pb-free and Green, 16-pin 173-mil TSSOP	
PI6C2408-1HLE			

Notes:

1. Thermal characteristics can be found on the company web site at <http://www.pericom.com/packaging/>