

HEF4067B-Q100

16-channel analog multiplexer/demultiplexer

Rev. 5 — 25 July 2024

Product data sheet

1. General description

The HEF4067B-Q100 is a single-pole 16-throw analog switch (SP16T) suitable for use in analog or digital 16:1 multiplexer/demultiplexer applications. The switch features four digital select inputs (A0, A1, A2 and A3), sixteen independent inputs/outputs (Yn), a common input/output (Z) and a digital enable input (E). When E is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 - Specified from -40 °C to +85 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Applications

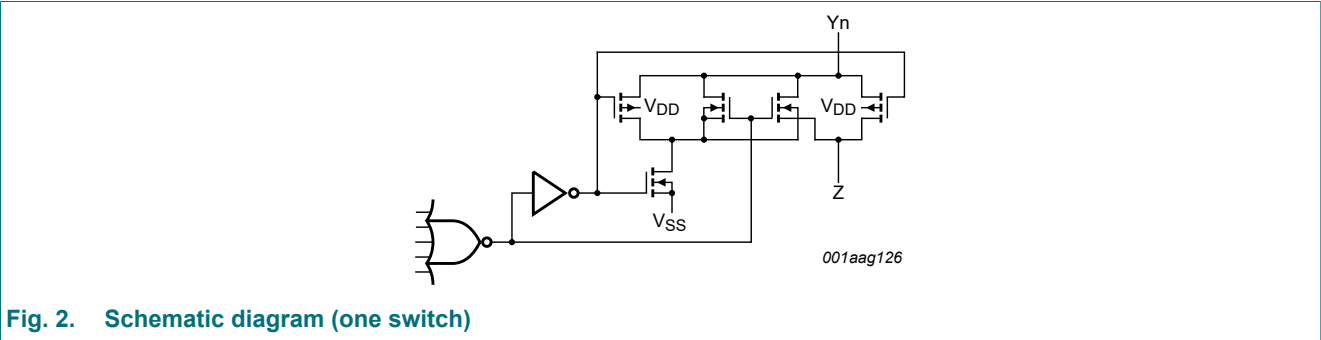
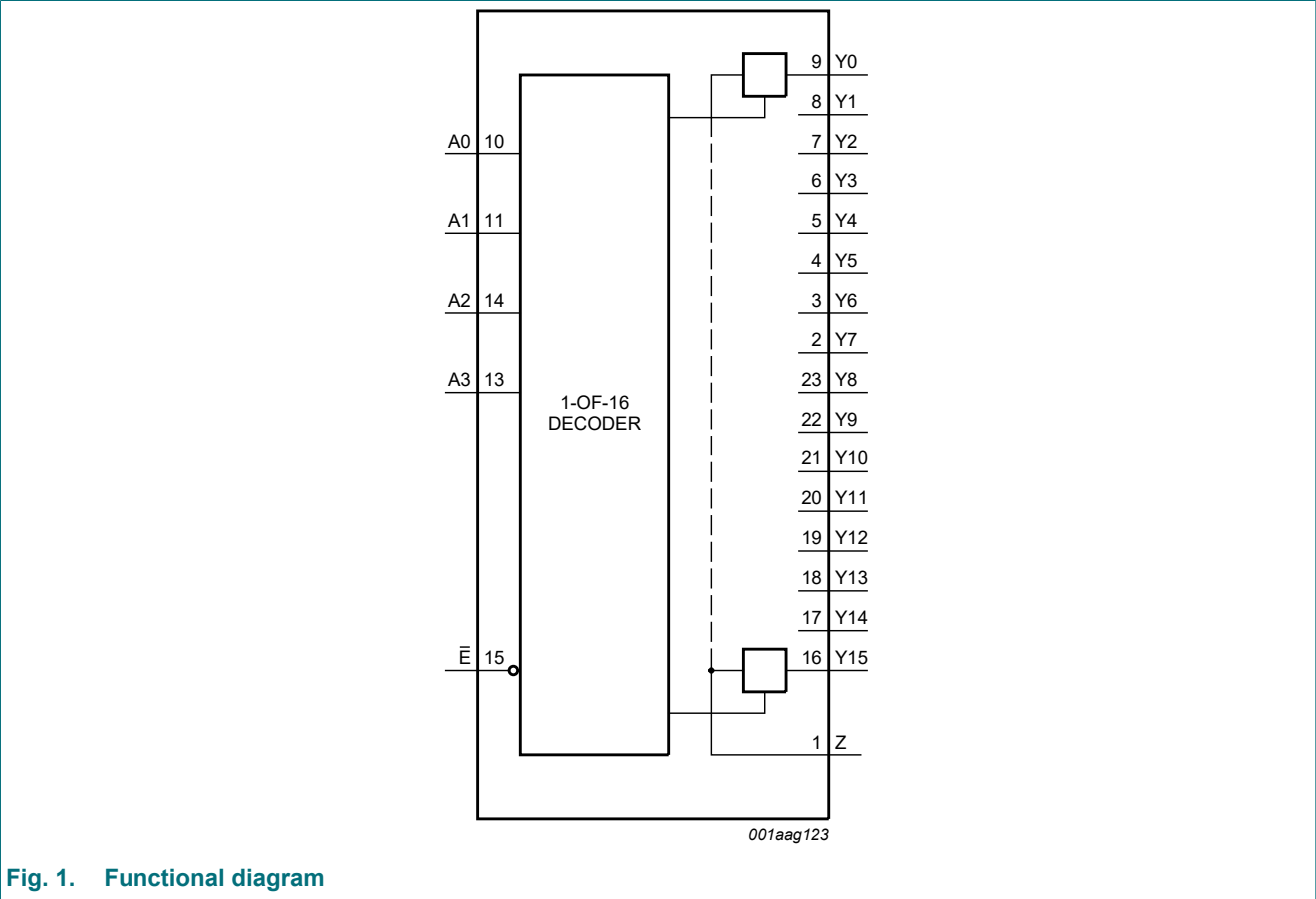
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4067BT-Q100	-40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
HEF4067BTT-Q100	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram



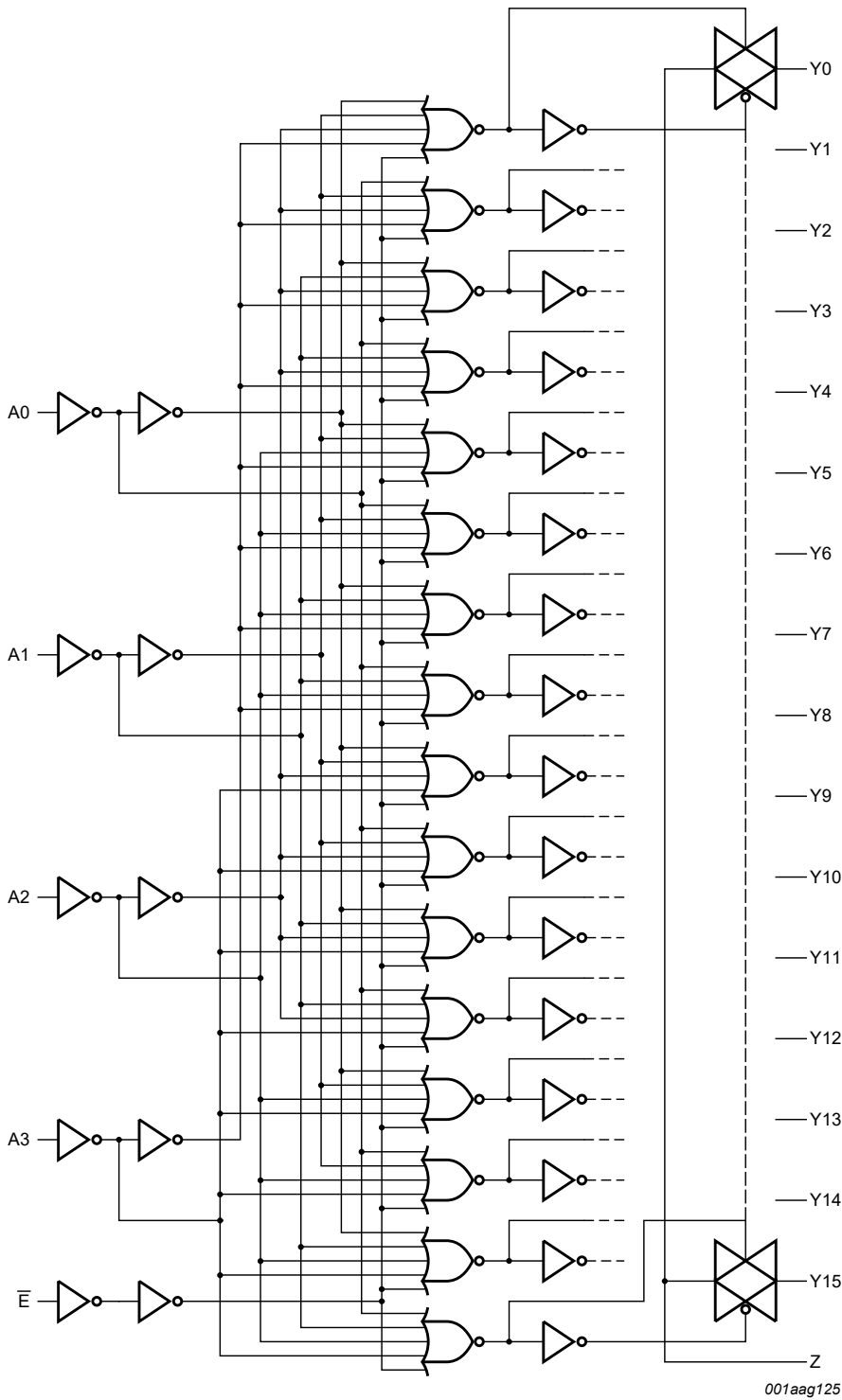
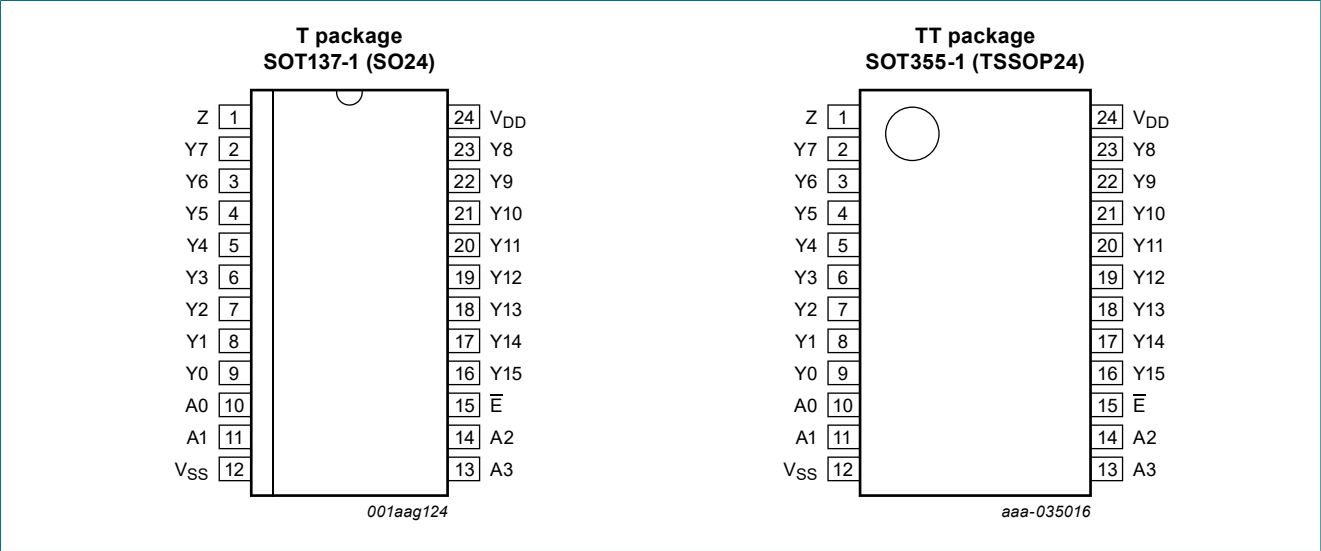


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Z	1	common input/output
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15	9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	independent input/output
A0, A1, A2, A3	10, 11, 14, 13	address input
VSS	12	ground (0 V)
E	15	enable input (active LOW)
VDD	24	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Control	Address				Channel ON
E	A3	A2	A1	A0	
L	L	L	L	L	Y0 = Z
L	L	L	L	H	Y1 = Z
L	L	L	H	L	Y2 = Z
L	L	L	H	H	Y3 = Z
L	L	H	L	L	Y4 = Z
L	L	H	L	H	Y5 = Z
L	L	H	H	L	Y6 = Z
L	L	H	H	H	Y7 = Z
L	H	L	L	L	Y8 = Z
L	H	L	L	H	Y9 = Z
L	H	L	H	L	Y10 = Z
L	H	L	H	H	Y11 = Z
L	H	H	L	L	Y12 = Z
L	H	H	L	H	Y13 = Z
L	H	H	H	L	Y14 = Z
L	H	H	H	H	Y15 = Z
H	X	X	X	X	none

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	pins An and $\bar{E}$; V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{I/O}	input/output current	[1]	-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

[1] To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y_n, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS}.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	supply voltage		3	-	15	V
V _I	input voltage		0	-	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

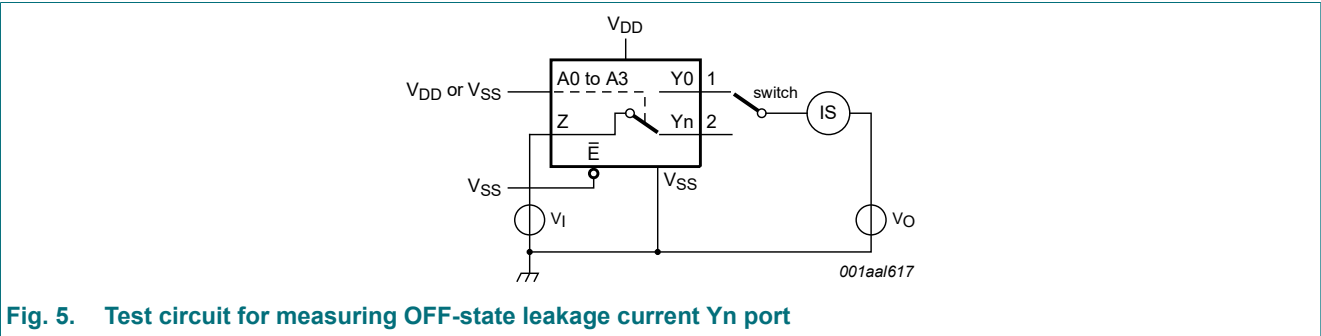
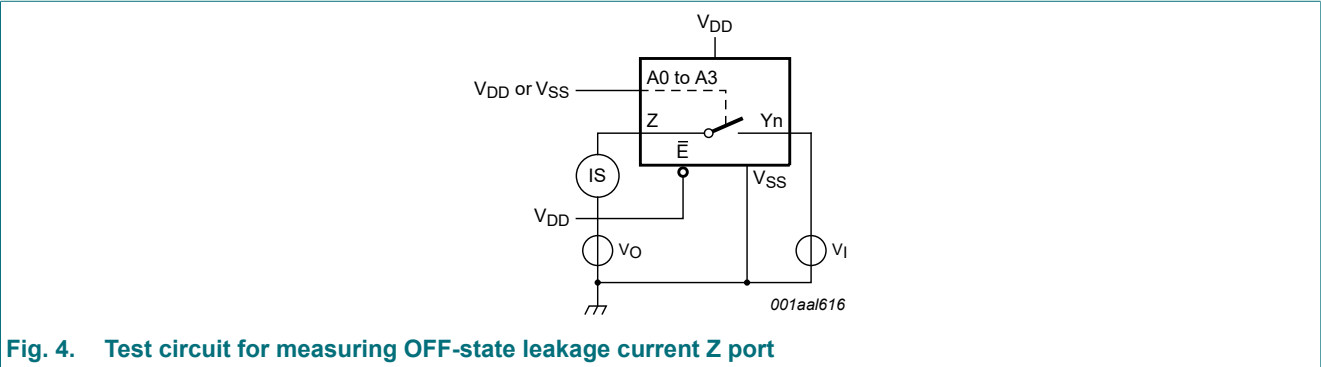
10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		T _{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IL}	LOW-level input voltage	I _O < 1 μA								
		V _O = 0.5 V or 4.5 V	5 V	-	1	-	1	-	1	V
		V _O = 1.0 V or 9.0 V	10 V	-	2	-	2	-	2	V
		V _O = 1.5 V or 13.5 V	15 V	-	2.5	-	2.5	-	2.5	V
V _{IH}	HIGH-level input voltage	I _O < 1 μA								
		V _O = 0.5 V or 4.5 V	5 V	4	-	4	-	4	-	V
		V _O = 1.0 V or 9.0 V	10 V	8	-	8	-	8	-	V
		V _O = 1.5 V or 13.5 V	15 V	12.5	-	12.5	-	12.5	-	V
I _I	input leakage current	V _I = 0 V or 15 V	15 V	-	±0.3	-	±0.3	-	±1.0	μA
I _{S(OFF)}	OFF-state leakage current	Z port; all channels OFF; see Fig. 4	15 V	-	-	-	1000	-	7500	nA
		Yn port; per channel; see Fig. 5	15 V	-	-	-	200	-	1500	nA
I _{DD}	supply current	all valid input combinations; I _O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C _I	input capacitance	digital inputs	15 V	-	-	-	7.5	-	-	pF

10.1. Test circuits



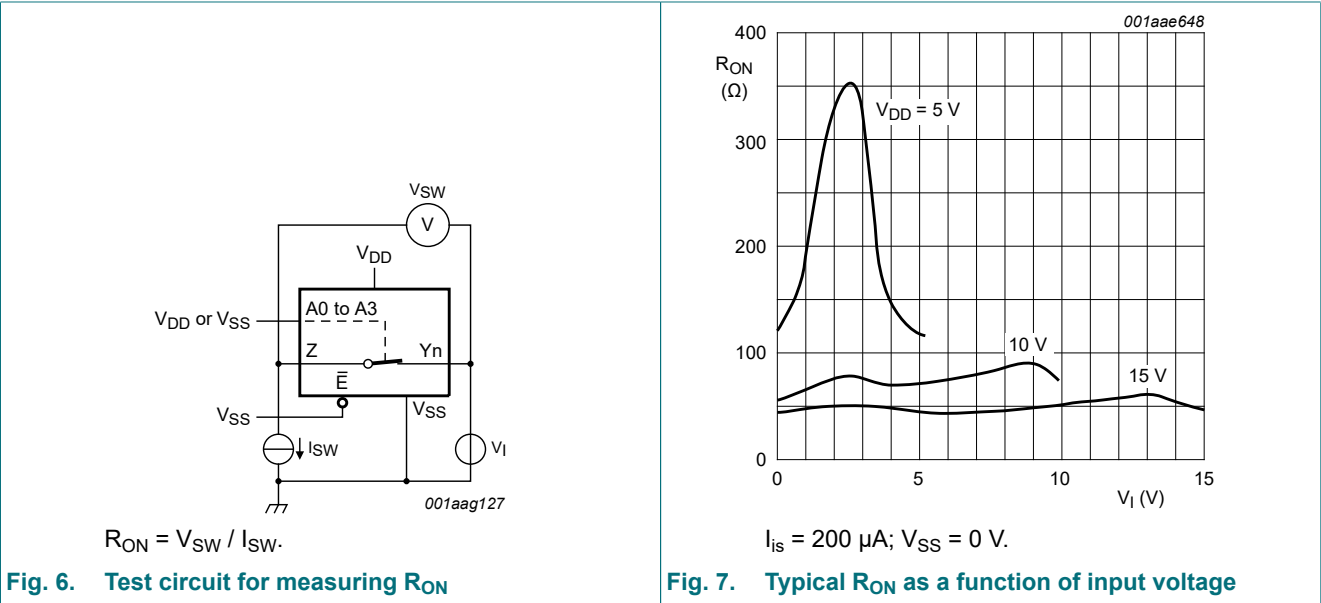
10.2. On resistance

Table 7. ON resistance

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $I_{SW} = 200\text{ }\mu\text{A}$; $V_{SS} = 0\text{ V}$.

Symbol	Parameter	Conditions	V_{DD}	Typ	Max	Unit
$R_{ON(peak)}$	ON resistance (peak)	$V_I = 0\text{ V to }V_{DD}$; see Fig. 6 and Fig. 7	5 V	350	2500	Ω
			10 V	80	245	Ω
			15 V	60	175	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_I = 0\text{ V}$; see Fig. 6 and Fig. 7	5 V	115	340	Ω
			10 V	50	160	Ω
			15 V	40	115	Ω
		$V_I = V_{DD}$; see Fig. 6 and Fig. 7	5 V	120	365	Ω
			10 V	65	200	Ω
			15 V	50	155	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0\text{ V to }V_{DD}$; see Fig. 6	5 V	25	-	Ω
			10 V	10	-	Ω
			15 V	5	-	Ω

10.2.1. On resistance waveform and test circuit



11. Dynamic characteristics

Table 8. Dynamic characteristics
 $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{SS} = 0\text{ V}$; for test circuit see Fig. 11.

Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	Y_n, Z to Z, Y_n ; see Fig. 8	5 V	-	30	60	ns
			10 V	-	15	25	ns
			15 V	-	10	20	ns
		A_n to Y_n, Z ; see Fig. 9	5 V	-	190	380	ns
			10 V	-	70	145	ns
			15 V	-	50	100	ns
t_{PLH}	LOW to HIGH propagation delay	Y_n, Z to Z, Y_n ; see Fig. 8	5 V	-	25	50	ns
			10 V	-	10	20	ns
			15 V	-	10	20	ns
		A_n to Y_n, Z ; see Fig. 9	5 V	-	175	345	ns
			10 V	-	70	140	ns
			15 V	-	50	100	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\bar{E}$ to Y_n, Z ; see Fig. 10	5 V	-	195	385	ns
			10 V	-	140	280	ns
			15 V	-	130	260	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\bar{E}$ to Y_n, Z ; see Fig. 10	5 V	-	215	435	ns
			10 V	-	180	355	ns
			15 V	-	170	340	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\bar{E}$ to Y_n, Z ; see Fig. 10	5 V	-	155	315	ns
			10 V	-	70	135	ns
			15 V	-	50	100	ns

Symbol	Parameter	Conditions	V _{DD}	Min	Typ	Max	Unit
t _{PZL}	OFF-state to LOW propagation delay	$\overline{E}$ to Y _n , Z; see Fig. 10	5 V	-	170	340	ns
			10 V	-	70	140	ns
			15 V	-	50	100	ns

11.1. Waveforms and test circuit

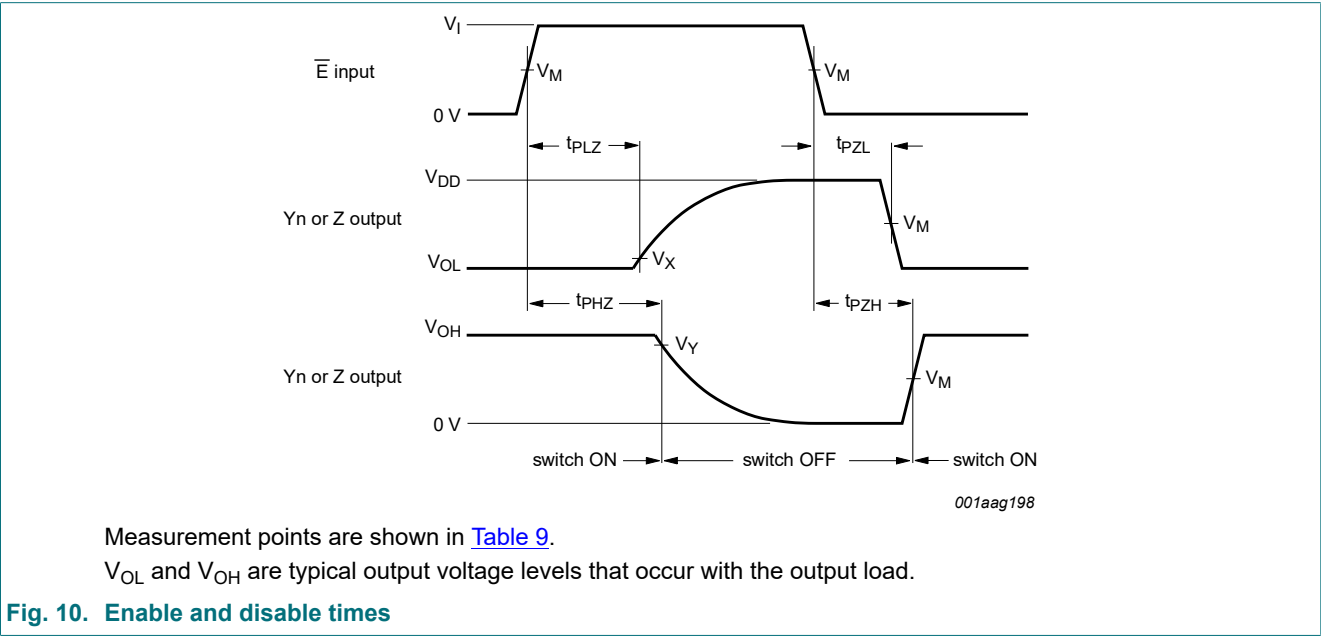
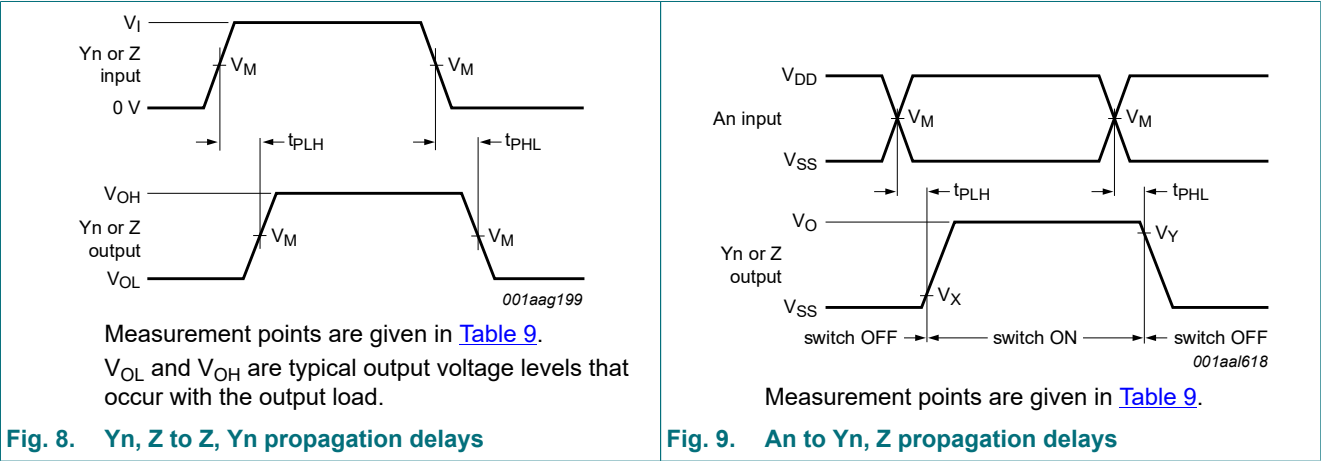


Table 9. Measurement points

Supply voltage	Input		Output		
V _{CC}	V _M	V _I	V _M	V _X	V _Y
5 V to 15 V	0.5 × V _{DD}	GND to V _{DD}	0.5 × V _{DD}	10%	90%

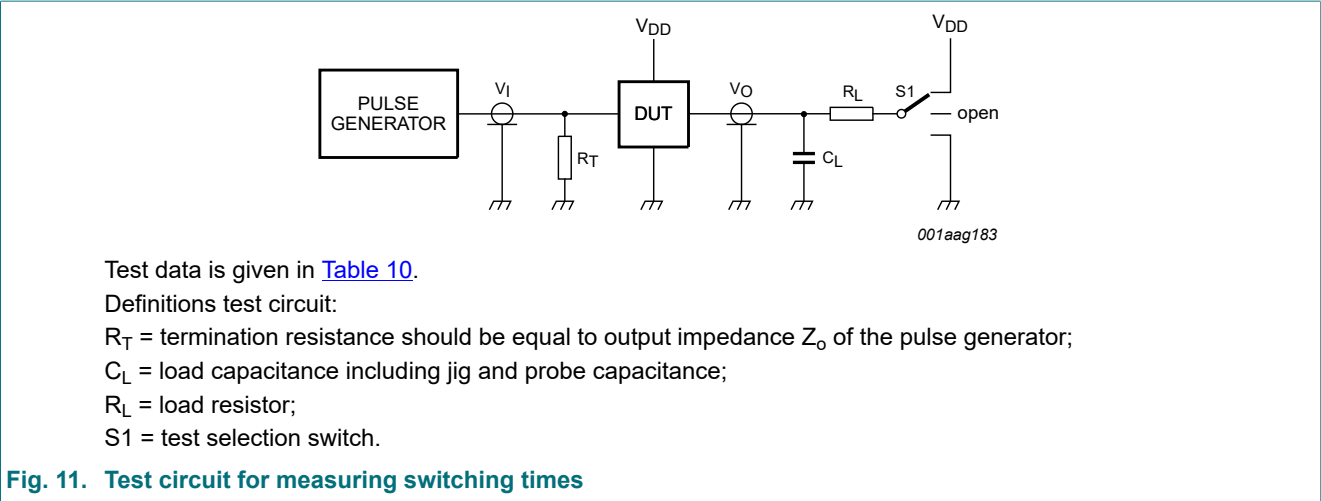


Table 10. Test data

Input				Load		S1 position				
Yn, Z	An and E	t _r , t _f	V _M	C _L	R _L	t _{PHL} [1]	t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	other
V _{DD} or V _{SS}	V _{DD} or V _{SS}	≤ 20 ns	0.5 × V _{DD}	50 pF	10 kΩ	V _{DD} or V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{SS}

[1] For Yn to Z or Z to Yn propagation delays use V_{SS}. For An or to Yn or Z propagation delays use V_{DD}.

11.2. Additional dynamic parameters

Table 11. Additional dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	V _{DD}	Typ	Max	Unit
THD	total harmonic distortion	see Fig. 12 ; R _L = 10 kΩ; C _L = 15 pF; channel ON; V _I = 0.5 × V _{DD} (p-p); f _i = 1 kHz	5 V	0.25	-	%
			10 V	0.04	-	%
			15 V	0.04	-	%
f _(-3dB)	-3 dB frequency response	see Fig. 13 ; R _L = 1 kΩ; C _L = 5 pF; channel ON; V _I = 0.5 × V _{DD} (p-p)	5 V	13	-	MHz
			10 V	40	-	MHz
			15 V	70	-	MHz
α _{iso}	isolation (OFF-state)	see Fig. 14 ; f _i = 1 MHz; R _L = 1 kΩ; C _L = 5 pF; channel OFF; V _I = 0.5 × V _{DD} (p-p)	10 V	-50	-	dB
V _{ct}	crosstalk voltage	digital inputs to switch; see Fig. 15 ; R _L = 10 kΩ; C _L = 15 pF; E or An = V _{DD} (square-wave)	10 V	50	-	mV
Xtalk	crosstalk	between switches; see Fig. 16 ; f _i = 1 MHz; R _L = 1 kΩ; V _I = 0.5 × V _{DD} (p-p)	10 V	-50	-	dB

[1] f_i is biased at 0.5 × V_{DD}; V_I = 0.5 × V_{DD} (p-p).

Table 12. Dynamic power dissipationP_D

P_D can be calculated from the formulas shown; V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V _{DD}	Typical formula for P _D (μW)	where:
P _D	dynamic power dissipation	5 V	$P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f _i = input frequency in MHz; f _o = output frequency in MHz; C _L = output load capacitance in pF; V _{DD} = supply voltage in V; Σ(C _L × f _o) = sum of the outputs.
		10 V	$P_D = 5500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.2.1. Test circuits

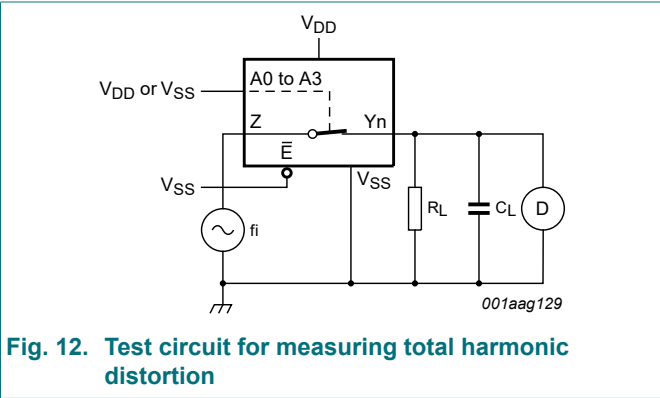


Fig. 12. Test circuit for measuring total harmonic distortion

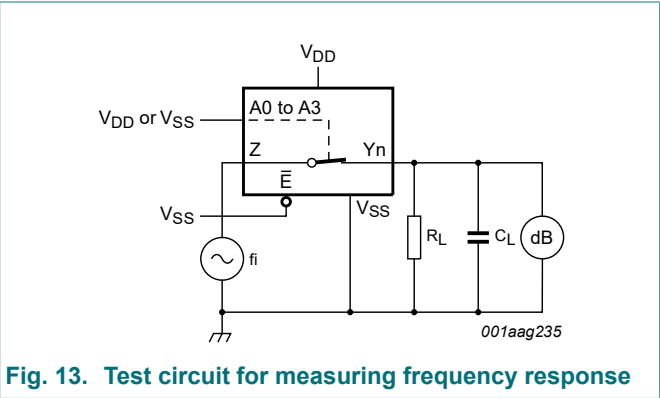


Fig. 13. Test circuit for measuring frequency response

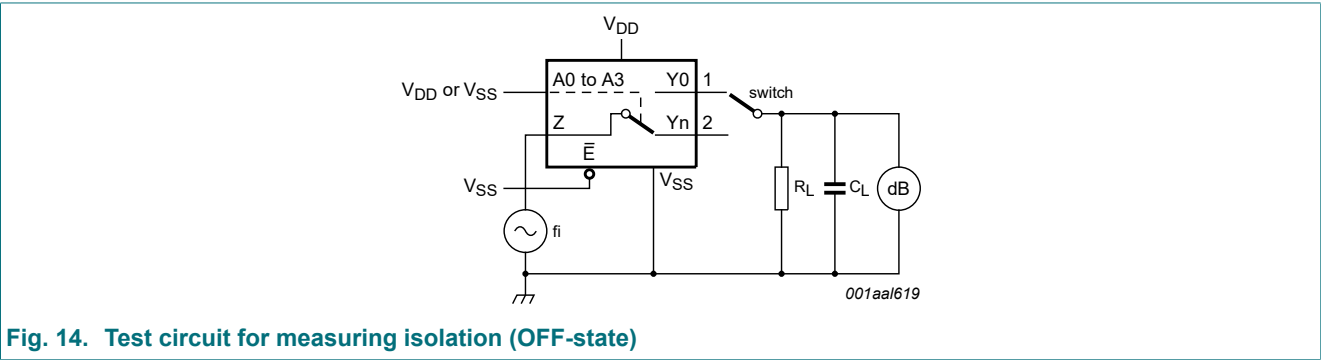


Fig. 14. Test circuit for measuring isolation (OFF-state)

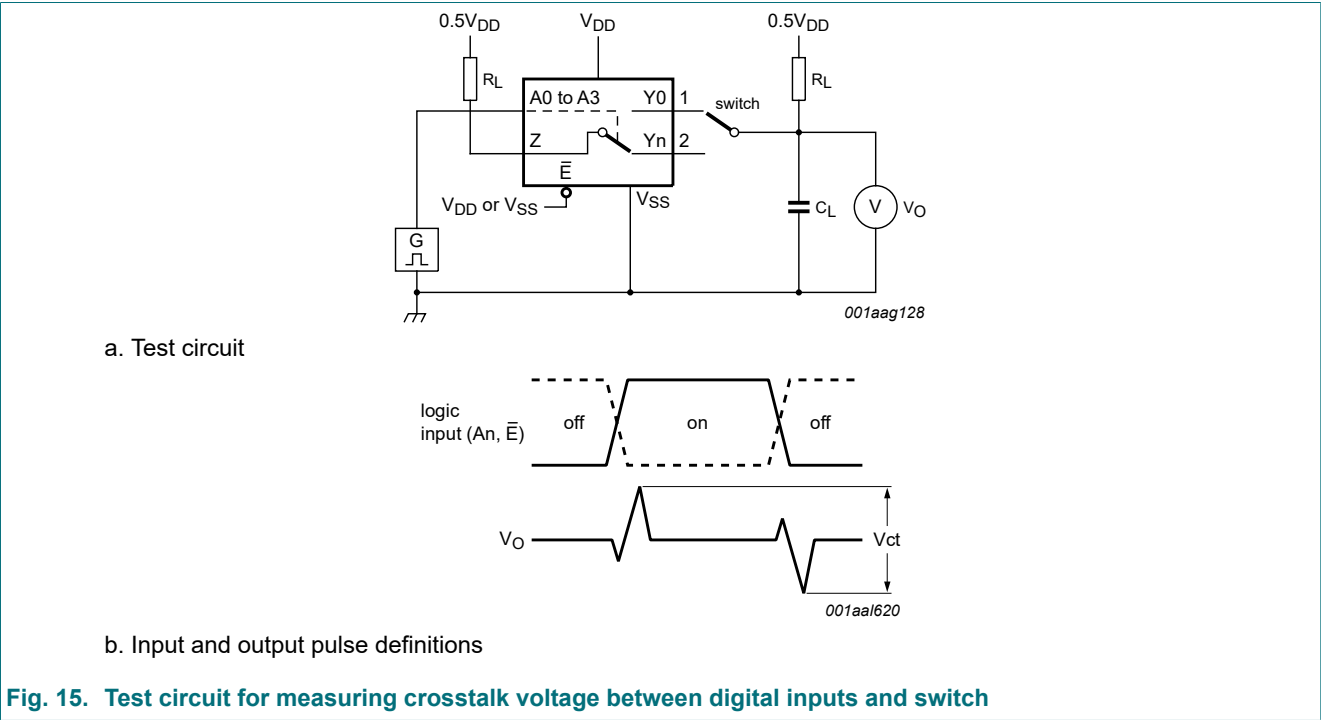


Fig. 15. Test circuit for measuring crosstalk voltage between digital inputs and switch

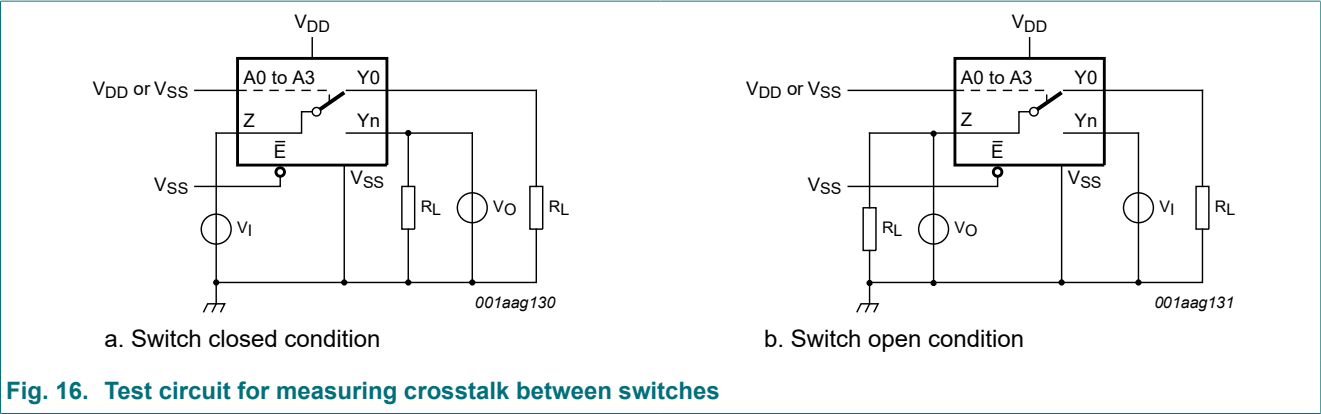


Fig. 16. Test circuit for measuring crosstalk between switches

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

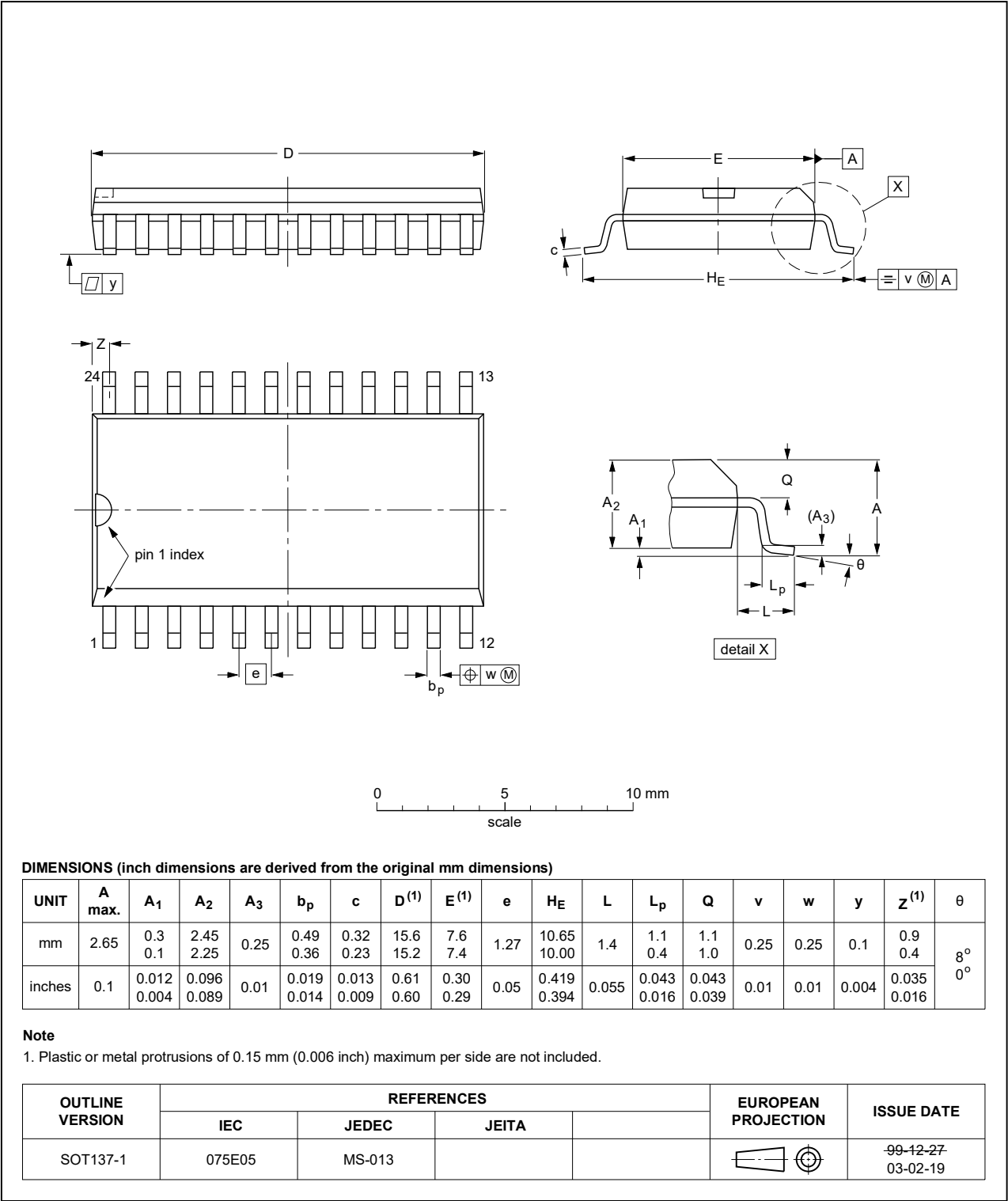


Fig. 17. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

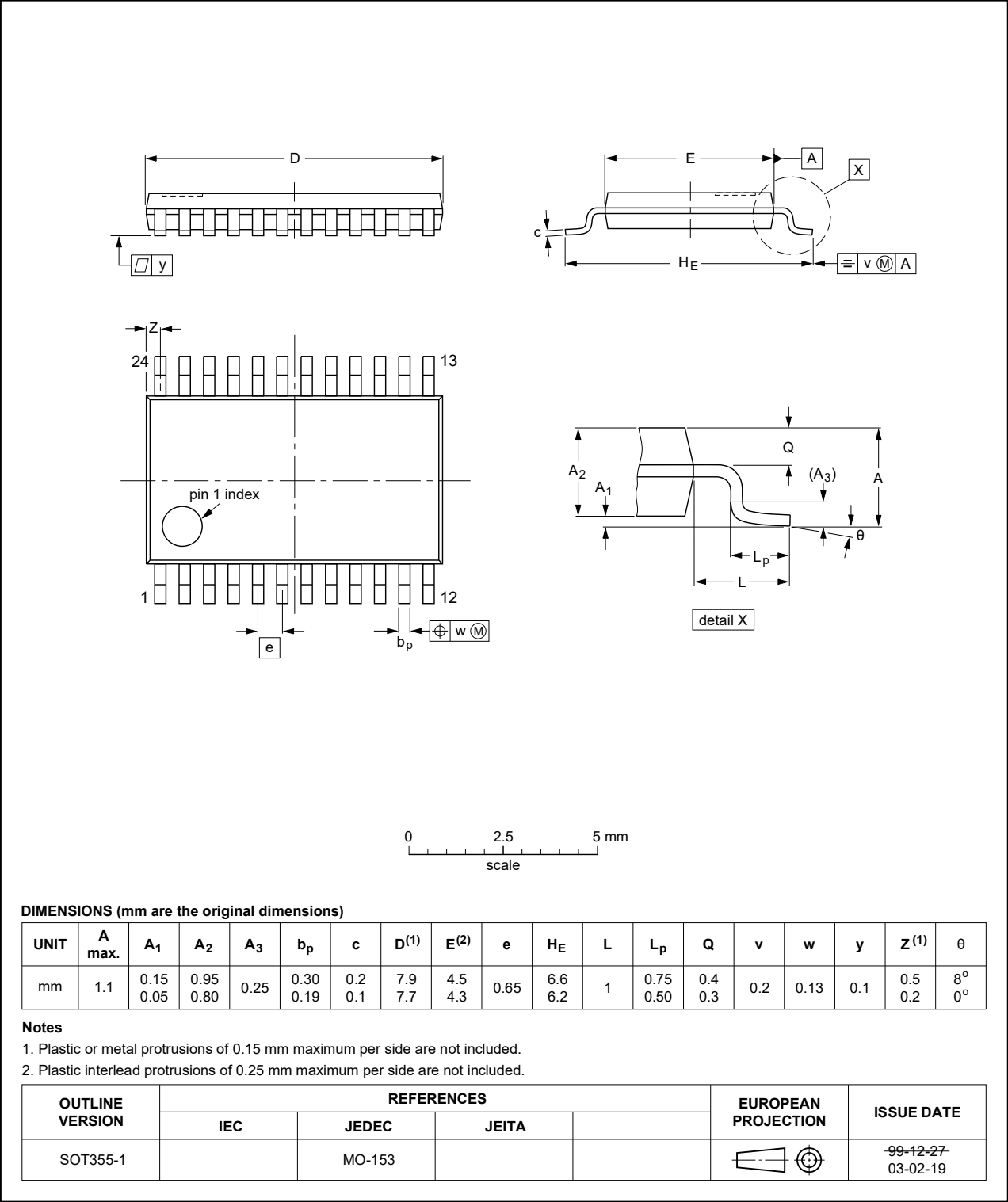


Fig. 18. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4067B_Q100 v.5	20240725	Product data sheet	-	HEF4067B_Q100 v.4
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
HEF4067B_Q100 v.4	20231107	Product data sheet	-	HEF4067B_Q100 v.3
Modifications:	- Table 6: I_{S(OFF)} parameter added for +85 °C, I_{OZ} specification removed. - Type number HEF4067BTT-Q100 (SOT355-1/TSSOP24) added.			
HEF4067B_Q100 v.3	20220110	Product data sheet	-	HEF4067B_Q100 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Section 1 and Section 2 updated.			
HEF4067B_Q100 v.2	20140911	Product data sheet	-	HEF4067B_Q100 v.1
Modifications:	Fig. 15: Test circuit modified			
HEF4067B_Q100 v.1	20130924	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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