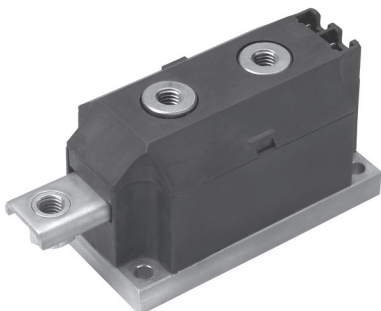


Fast Thyristor/Diode and Thyristor/Thyristor (MAGN-A-PAK Power Modules), 180 A



MAGN-A-PAK

FEATURES

- Fast turn-off thyristor
- Fast recovery diode
- High surge capability
- Electrically isolated baseplate
- 3000 V_{RMS} isolating voltage
- Industrial standard package
- UL approved file E78996 
- Compliant to RoHS directive 2002/95/EC


RoHS
COMPLIANT

PRODUCT SUMMARY

$I_{T(AV)}$	180 A
Type	Modules - Thyristor, Fast

DESCRIPTION

These series of MAGN-A-PAK modules are intended for applications such as self-commutated inverters, DC choppers, electronic welders, induction heating and others where fast switching characteristics are required.

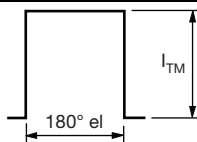
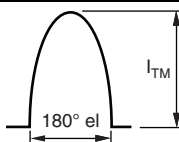
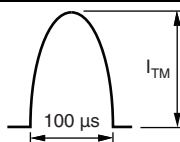
MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$		180	A
	T_C	85	°C
$I_{T(RMS)}$		400	
I_{TSM}	50 Hz	7130	A
	60 Hz	7470	
I^2t	50 Hz	255	kA ² s
	60 Hz	232	
$I^2\sqrt{t}$		2550	kA ² √s
t_q		20/25	μs
t_{rr}		2	
V_{DRM}/V_{RRM}		800/1200	V
T_J	Range	- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} MAXIMUM AT $T_J = 125\text{ °C}$ mA
VSK.F180-	08	800	800	50
	12	1200	1200	

CURRENT CARRYING CAPABILITY							
FREQUENCY							UNITS
50 Hz	370	530	565	800	2400	3150	A
400 Hz	435	650	670	1000	1540	2050	
2500 Hz	290	430	490	720	610	830	
5000 Hz	240	345	390	540	390	540	
10 000 Hz	170	270	290	390	-	-	
Recovery voltage V_r	50		50		50		V
Voltage before turn-on V_d	80 % V_{DRM}		80 % V_{DRM}		80 % V_{DRM}		
Rise of on-state current di/dt	50		-		-		A/μs
Case temperature	85	60	85	60	85	60	°C
Equivalent values for RC circuit	10/0.47		10/0.47		10/0.47		Ω/μF

ON-STATE CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			180	A
					85	°C
Maximum RMS current	I _{T(RMS)}	As AC switch			400	A
Maximum peak, one-cycle non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	7130	
		t = 8.3 ms			7470	
		t = 10 ms	100 % V _{RRM} reapplied		6000	
		t = 8.3 ms			6280	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		255	kA ² s
		t = 8.3 ms			232	
		t = 10 ms	100 % V _{RRM} reapplied		180	
		t = 8.3 ms			164	
Maximum I ² √t for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reapplied			2550	kA ² √s
Low level value or threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)} < I < π × I _{T(AV)}), T _J = T _J maximum			1.30	V
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.38	
Low level value on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)} < I < π × I _{T(AV)}), T _J = T _J maximum			0.90	mΩ
High level value on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			0.71	
Maximum on-state voltage drop	V _{TM}	I _{pk} = 600 A, T _J = T _J maximum, t _p = 10 ms sine pulse			1.84	V
Maximum holding current	I _H	T _J = 25 °C, I _T > 30 A			600	mA
Typical latching current	I _L	T _J = 25 °C, V _A = 12 V, R _a = 6 Ω, I _g = 1 A			1000	



SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS
			K	J	
Maximum non-repetitive rate of rise	di/dt	Gate drive 20 V, 20 Ω, tr ≤ 1 ms, VD = 80 % VDRM TJ = 25 °C	800		A/μs
Maximum recovery time	trr	ITM = 350 A, di/dt = - 25 A/μs, VR = 50 V, TJ = 25 °C	2		μs
Maximum turn-off time	tq	ITM = 750 A; TJ = 125 °C; di/dt = - 25 A/μs; VR = 50 V; dV/dt = 400 V/μs linear to 80 % VDRM	20	25	

TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$f = 50\text{ Hz}$, $d\% = 50$	60	W
Maximum peak average gate power	$P_{G(AV)}$	$T_J = 125\text{ }^{\circ}\text{C}$, $f = 50\text{ Hz}$, $d\% = 50$	10	
Maximum peak positive gate current	I_{GM}	$T_J = 125\text{ }^{\circ}\text{C}$, $t_p \leq 5\text{ ms}$	10	A
Maximum peak negative gate voltage	$-V_{GM}$		5	V
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25\text{ }^{\circ}\text{C}$, $V_{ak} 12\text{ V}$, $R_a = 6\text{ }\Omega$	200	mA
DC gate voltage required to trigger	V_{GT}		3	V
DC gate current not to trigger	I_{GD}	$T_J = 125\text{ }^{\circ}\text{C}$, rated V_{DRM} applied	20	mA
DC gate voltage not to trigger	V_{GD}		0.25	V

3

ΔR_{thJC} CONDUCTION				
CONDUCTIONS ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.009	0.006	$T_J = 125\text{ }^{\circ}\text{C}$	K/W
120°	0.010	0.011		
90°	0.014	0.015		
60°	0.020	0.020		
30°	0.032	0.033		

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

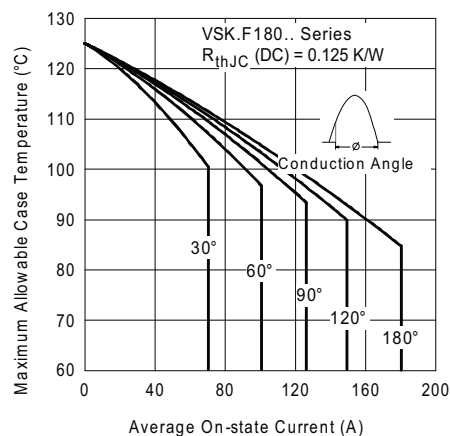


Fig. 1 - Current Ratings Characteristics

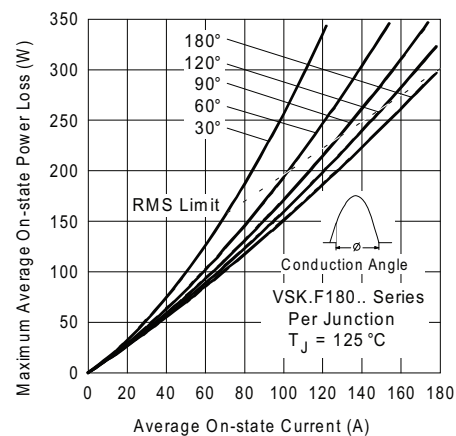


Fig. 3 - On-State Power Loss Characteristics

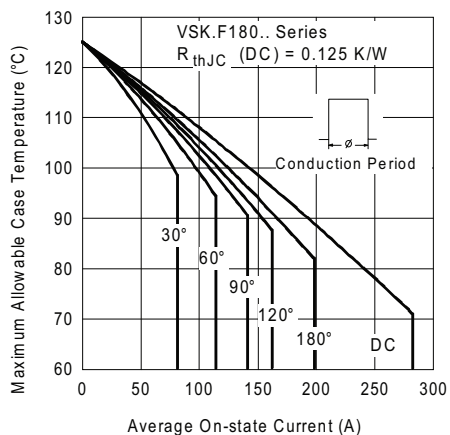


Fig. 2 - Current Ratings Characteristics

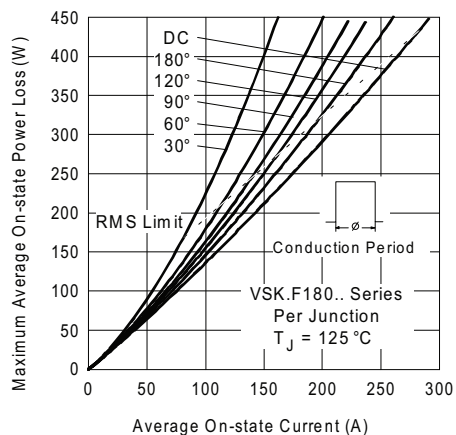


Fig. 4 - On-State Power Loss Characteristics

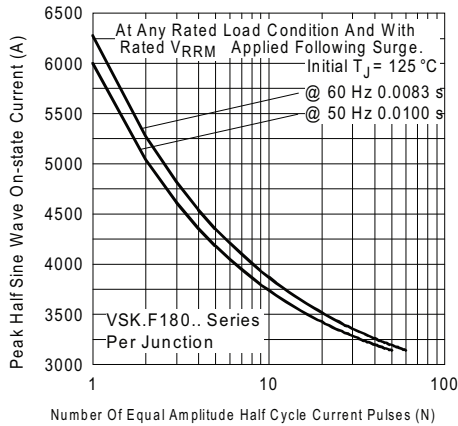


Fig. 5 - Maximum Non-Repetitive Surge Current

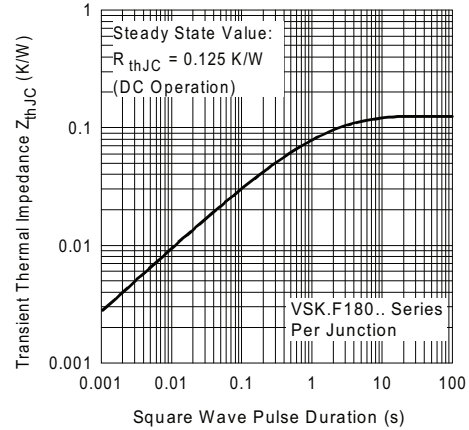


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

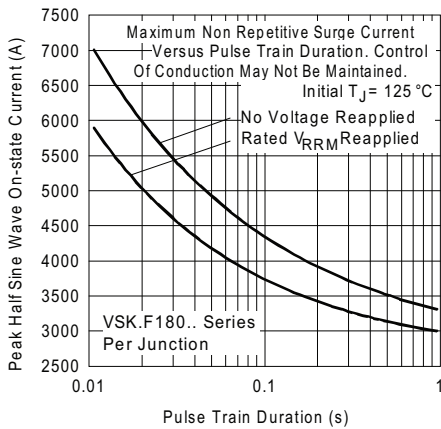


Fig. 6 - Maximum Non-Repetitive Surge Current

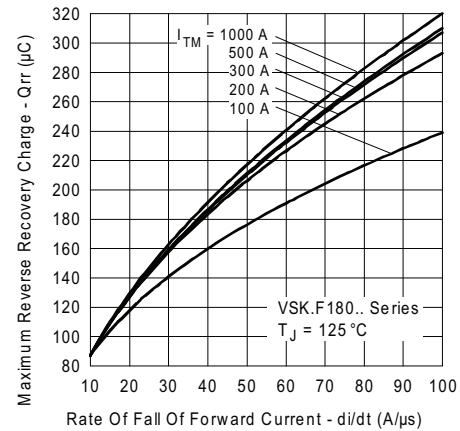


Fig. 9 - Reverse Recovery Charge Characteristics

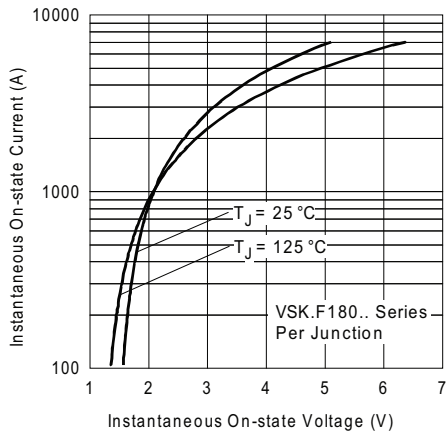


Fig. 7 - On-State Voltage Drop Characteristics

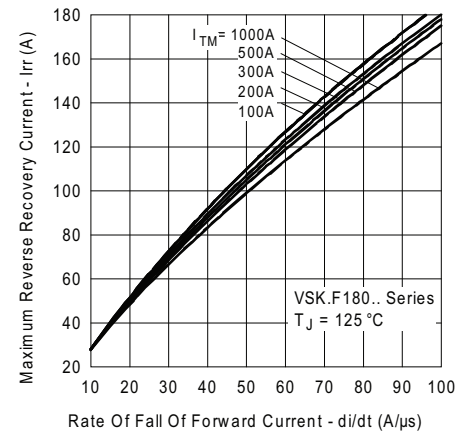


Fig. 10 - Reverse Recovery Current Characteristics

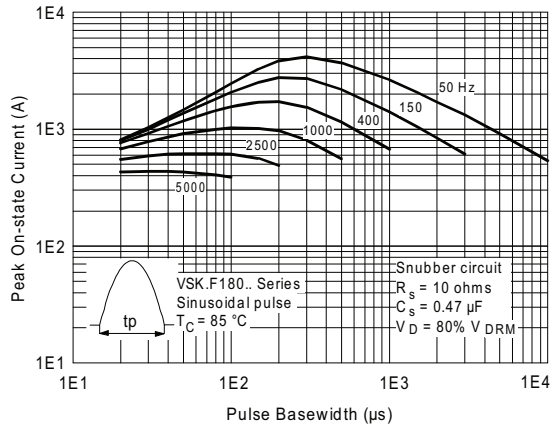


Fig. 11 - Frequency Characteristics

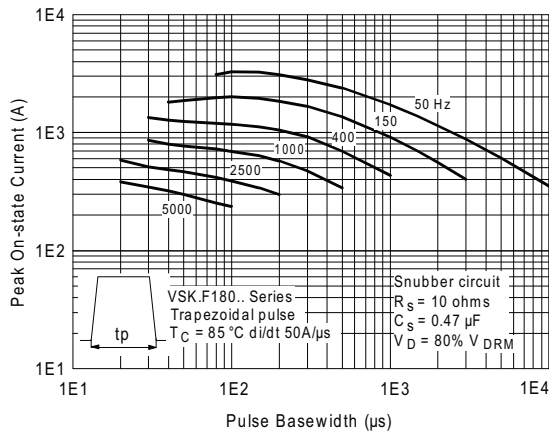
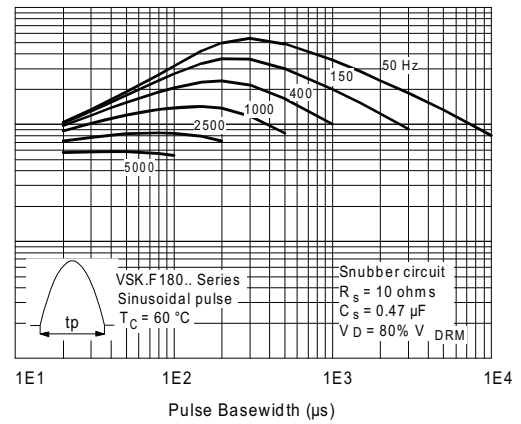


Fig. 12 - Frequency Characteristics

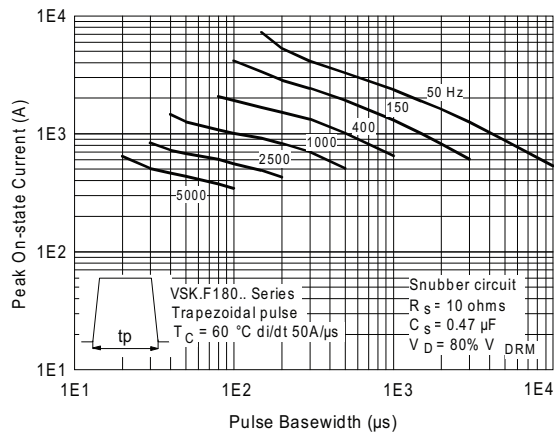
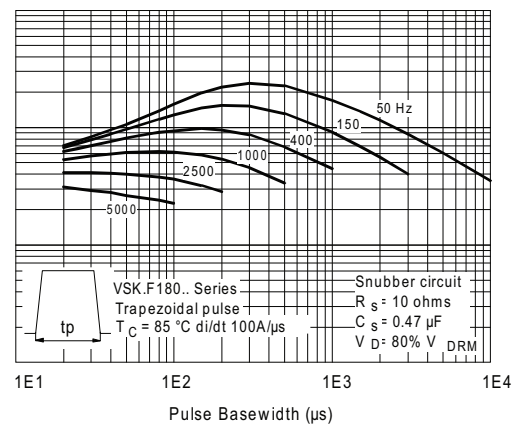
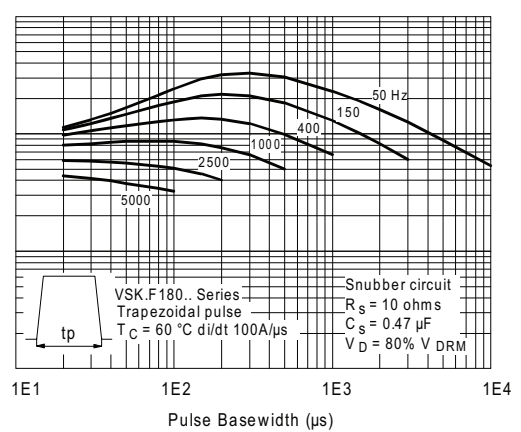


Fig. 13 - Frequency Characteristics



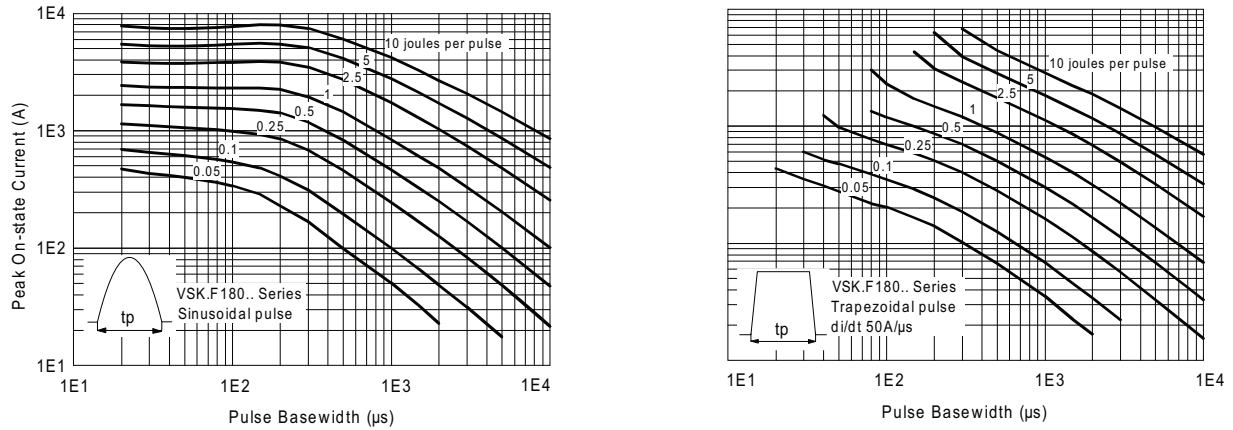


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

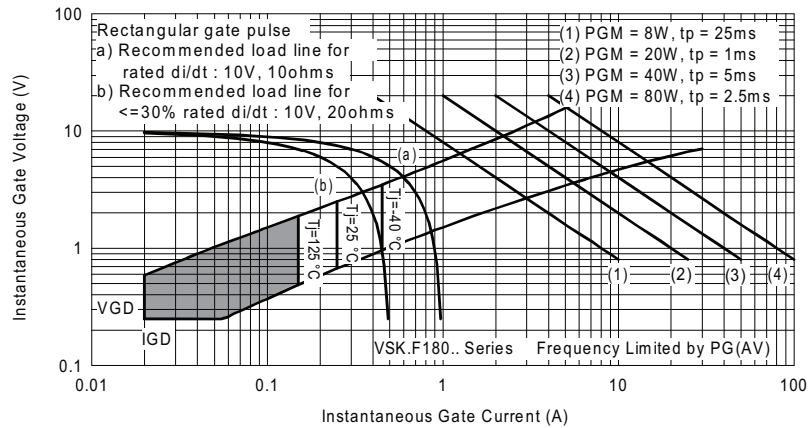


Fig. 15 - Gate Characteristics

Vishay Semiconductors Fast Thyristor/Diode and Thyristor/Thyristor
(MAGN-A-PAK Power Modules), 180 A



1	-	Module type
2	-	Circuit configuration (see circuit configuration table)
3	-	Fast SCR
4	-	Current rating: $I_{T(AV)} \times 10$ rounded
5	-	Voltage code $\times 100 = V_{RRM}$ (see Voltage Ratings table)
6	-	dV/dt code: $H \leq 400 \text{ V}/\mu\text{s}$
7	-	t_q code: $K \leq 20 \mu\text{s}$ $J \leq 25 \mu\text{s}$
8	-	P = Lead (Pb)-free

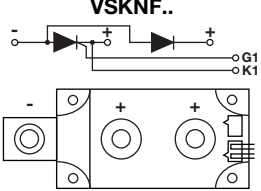
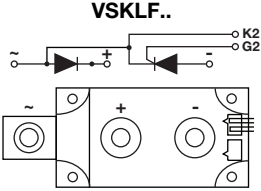
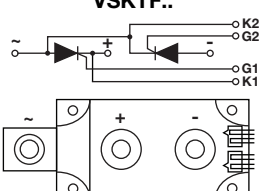
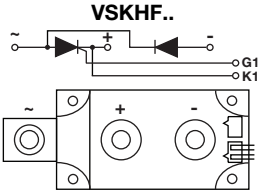
- To order the optional hardware go to www.vishay.com/doc?95172

www.vishay.com
8

For technical questions within your region, please contact one of the following:
DiodesAmericas@vishay.com, DiodesAsia@vishay.com, DiodesEurope@vishay.com

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Revision: 19-Jul-10

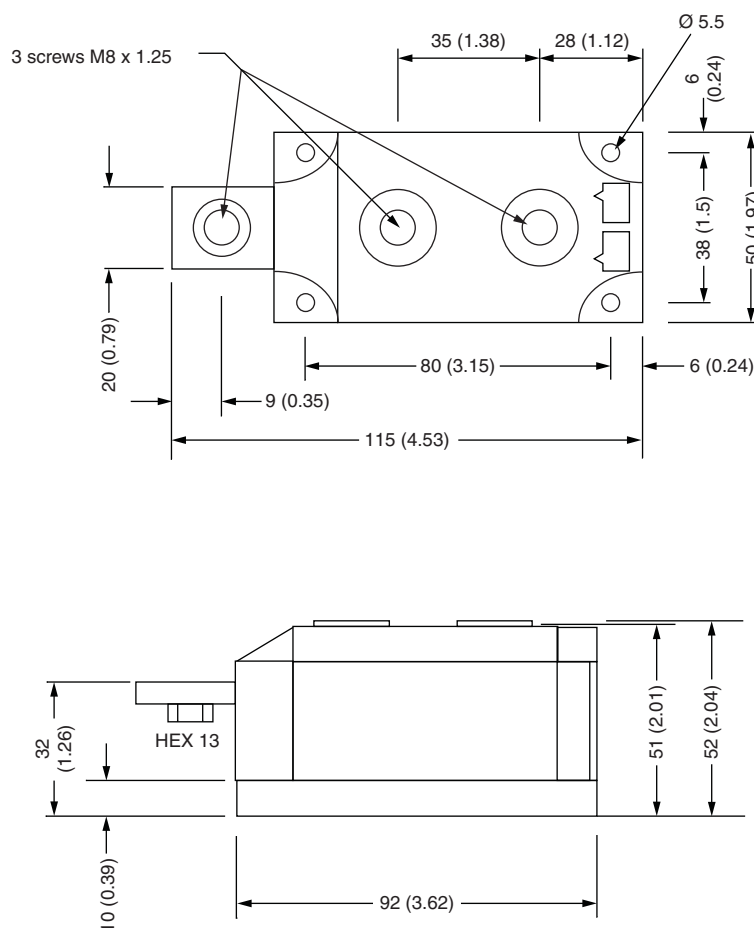


CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
SCR/diode common anodes	N	
SCR/diode doubler circuit, negative control	L	
Two SCRs doubler circuit	T	
SCR/diode doubler circuit, positive control	H	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95086

MAGN-A-PAK

DIMENSIONS in millimeters (inches)



Notes

- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94 V-0



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