TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

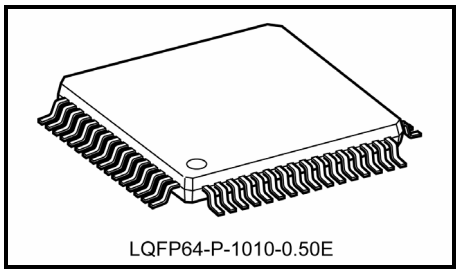
TC9349AFG

Single-Chip DTS Micro controller (DTS-21)

The TC9349AFG is a single-chip DTS micro controller for portable audio incorporating 30 MHz prescaller, PLL, and LCD driver. In Addition to an IF counter, serial interface, and buzzer function, the device supports and interrupt function, timer counter, pulse counter Electronic volume function and A/D converter.

The LCD driver features built-in 1/4 duty, 1/2 bias or 1/3 bias and a 3 V voltage doubler boosting circuit, implementing stable LCD.

The power supply voltage ranges from 0.9 V to 1.8 V. Because of its low-current consumption, the device is suitable for use in digital tuning system in portable equipment such as headphone stereos.



LQFP64-P-1010-0.50E

Weight: 0.32 g (typ.)

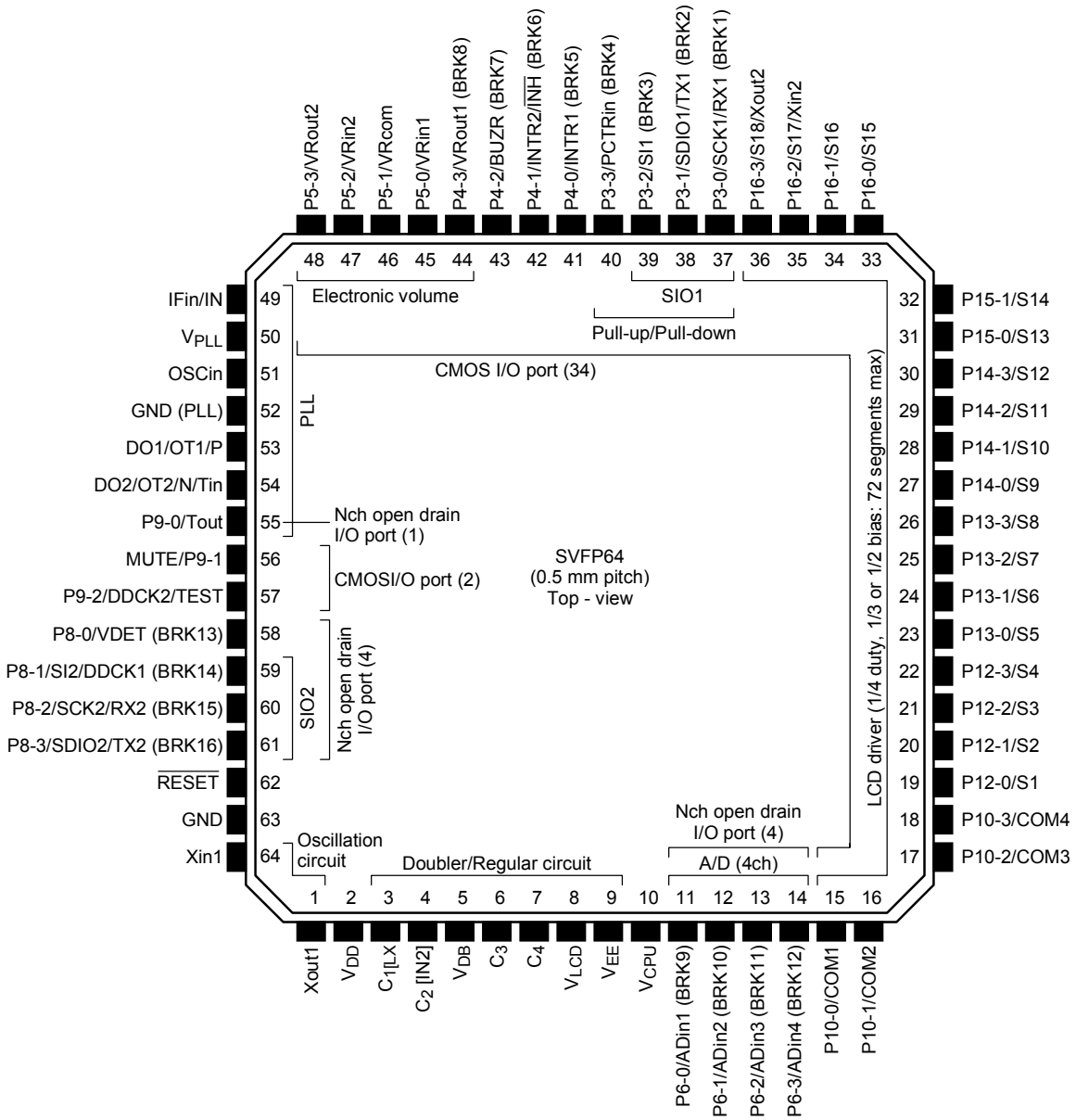
Features

- CMOS DTS micro controller LSI with built-in prescaller, PLL and LCD driver
- Operating Voltage range: VDD = 0.9 to 1.8 V (typ.: 1.5 V)
- Current dissipation: When CPU in operation: IDD = 150 μA (typ.)
  When PLL in operation: IDD = 1mA (typ. At inputting OSCin = 30 MHz)
- Operating temperature range: Ta = −10 to 60°C
- Program memory (ROM): 16-bit × 8192 steps
- Data memory (RAM): 4-bit × 512 words
- Oscillator frequency: Crystal oscillator: 75 kHz (Crystal oscillator)
  High speed oscillator: 300 to 600 kHz (Ceramic oscillator or Crystal oscillator)
- Instruction execution time: Crystal oscillator: 40 μs, High speed oscillator: 5 to 10 μs
- Interrupt: External: 2 system (INTR1, INTR2 pin)
  Internal: 4 system (Serial-interface, Timer-port, Timer-counter, Detected for decreasing voltage)
- Interrupt stack: 4 level × 26 bit-register, Data select, Carry flag, Data register
- Address stack: 16 level × 13 bit (Program counter)
- I/O port: CMOS I/O port: 36 (max), Nch open drain I/O port: 9 (max), Exclusive output port: 2(max),
  Exclusive input port: 1 (max)
- LCD driver: 1/4 duty, 1/2bias or 1/4 duty, 1/3 bias: 72 segments (max)
- Serial Interface: 1 system, 2 channel (Nch open drain, CMOS I/O port), 3kind (3-wired, 2-wired, UART)
- Buzzer: 4 kind of frequency (1 kHz, 1.56 kHz, 2.08kHz, 3 kHz),
  4 mode (Continuous, single-shot, 10 Hz Intermittent, 10 Hz intermittent 1 Hz interval)
- Timer counter: 8 bit, 2 kind of timer clock (25 kHz, 1 kHz),
  2 mode (Timer counter, Pulse width measure (INTR1pin))
- Pulse counter: 8 bit up/down counter
- Electronic volume: 2 channel, 32 step (0dB to -78dB, -∞dB)
- A/D converter: 6 bit, 4 channel, changing time: 240 μs
- Amplifier for LPF: 5.5 V output max. (Tout, Tin)
- DC-DC converter of VT: 2 stage (0.75 V, 1.0 V) voltage detected (VDET)
  15 kind of doubler clock, 2 type doubler clock output
  (CMOS output: DDCK2, Nch output: DDCK1)

- DC-DC converter of CPU: Charge-pump type or Switching regulator type (selectable by Al switch)
  2 kind of doubler clock: 75 kHz Crystal oscillator,
  High speed oscillator clock (300 to 600 kHz)
  Setting doubler voltage for 3 stage (2.0 V, 2.5 V, 3.0 V)
- Programmable counter: 16 bit HF mode: 1/15,16 pulse swallow type (1 to 30 MHz, Vin = 0.1Vp-p (min))
  LF mode: 12 bit direct divider type (0.5 to 4 MHz, Vin = 0.1Vp-p (min))
- Reference frequency: 10 kinds (1 kHz, 1.3889 kHz, 1.5625 kHz, 2.7778 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz, 25 kHz)
- Phase comparator: 2 (max), setting for "H"/"L" level, High-impedance and built-in output resistor by program. (0 kΩ, 5 kΩ, 50 kΩ, 100 kΩ) (DO1/DO2)
  It's possible to automatic change of output resistor for phase difference by program. (DO2)
- General purpose If counter: 20 bits, 0.03 to 12 MHz, Vin = 0.1Vp-p (min)
- Back up function: 3 modes (Clock stop: Crystal oscillator Stop, Hard wait: Only crystal oscillator operating, Soft wait: CPU intermittent operating)
- Reset function: Built-in Power on reset circuit (selectable by Al switch)
- Detected decrease voltage function: It's possible to detect the voltage by 25 mV step in VDD = 0.850 V to 1.225 V.
  It's possible to select the CPU stop function by detected decreasing voltage.
- Package: QFP-64 (0.5 mm pith, 1.4 mm thick)
- EEPROM product: TC93E49FG

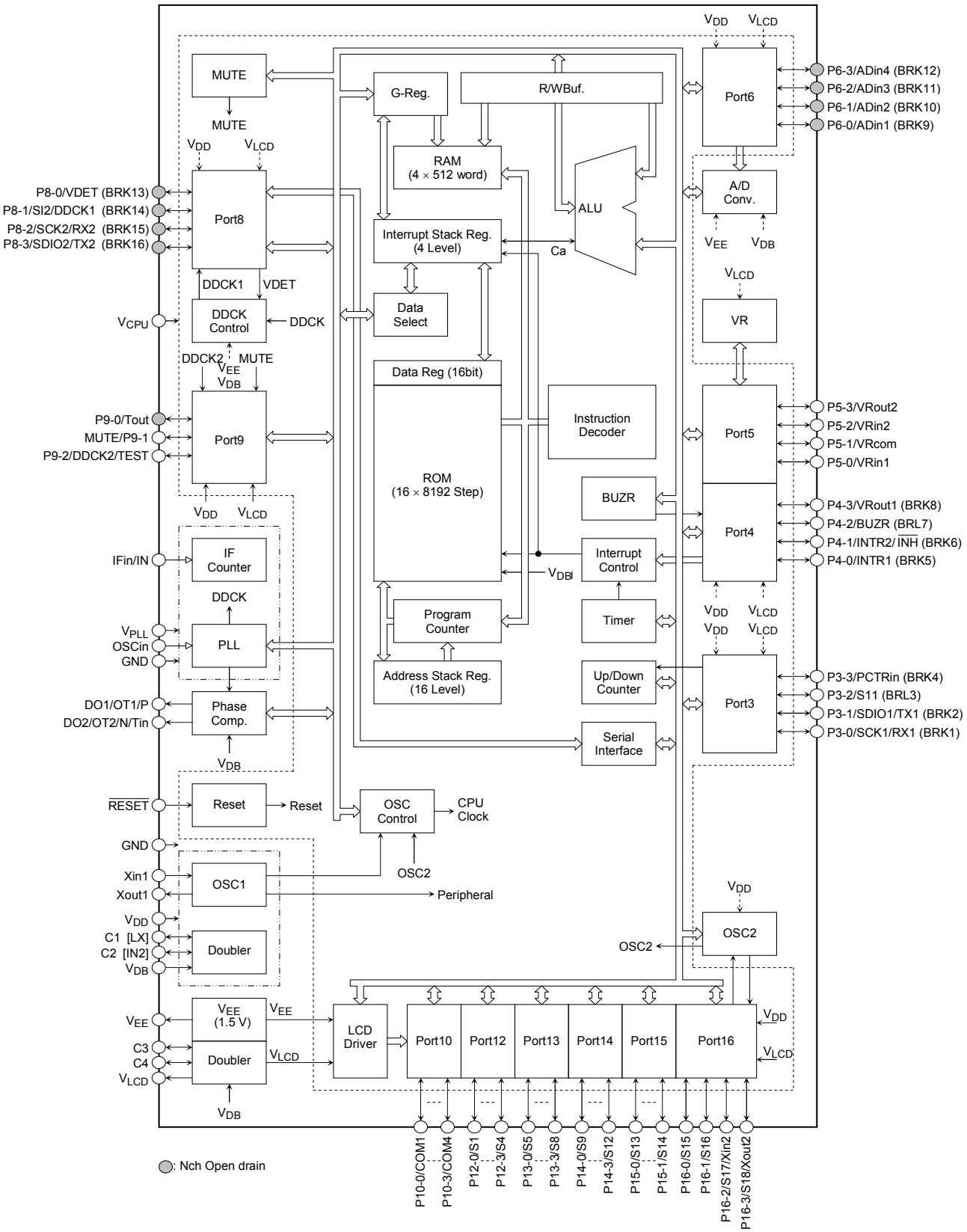
Note: Handle with care to prevent devices from deterioration by static electricity.

Pin Assignment

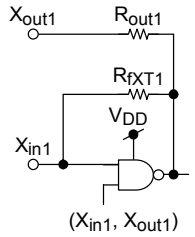
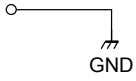
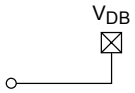


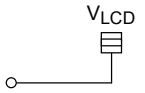
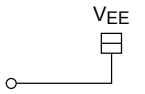
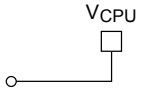
[ ]: AI option

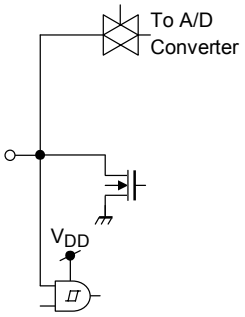
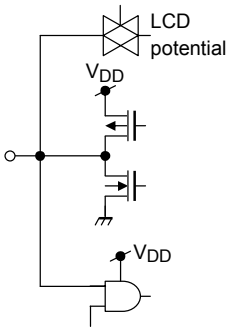
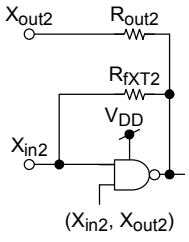
Block Diagram

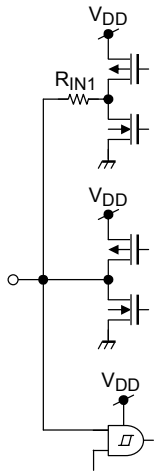


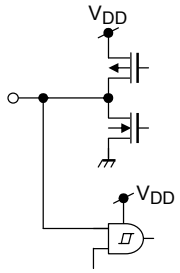
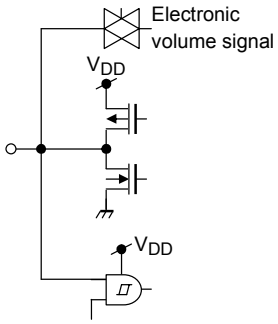
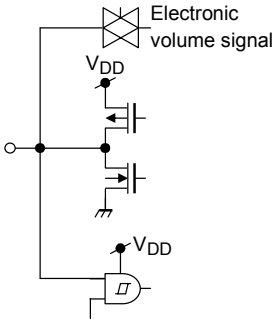
Description of Pin Function

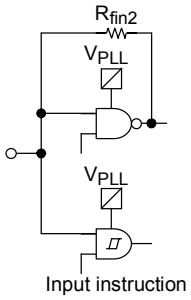
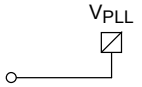
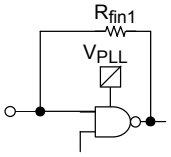
PIN No.	Symbol	Pin Name	Function and Operation	Remarks
64	Xin1	Crystal oscillator pin	Crystal oscillator pins. A reference 75 KHz crystal resonator is connected to the Xin1 and Xout1 pins.	
1	Xout1			
68	GND	Power-supply pins	Power supply pin for Crystal oscillator and doubler circuit for CPU (V_{DB}). Normally, V_{DD} = 0.9 to 1.8 V is applied. VDD potential can detect the range of the power decreased voltage function voltage 0.850 V to 1.225 V at 25 mV step by the decrease voltage detection circuit. If V_{DD} potential becomes below setting voltage, CPU can be stopped for CPU incorrect operation prevention. Note: After reset function, the decrease voltage detection voltage is setup to V_{DD} = 0.85 V and CPU stop function will be in a enable state.	
2	V_{DD}			
3	C1 [LX]	Doubler output pins for CPU	Doubler output pins for CPU. Doubler system can select to a charge pump or a switching regulator type by AI switch. When a doubler clamp is permitted, a voltage can select for three kinds of 2.0 V/2.5 V/3.0 V. A doubler clock can select 75 kHz/37.5 kHz or high-speed oscillator clock. Usually, Connects to the capacitor for stabilization (0.1 μF, 10 μF typ.) to V_{DB} pin and supplies V_{DB} potential to the power supply only for CPU (V_{CPU}). The potential is supplied to the power supply of A/D converter, and a 1.5 V constant voltage circuit (V_{EE}). In a charge pump system, the voltage stepped-up by the doubler capacitor between C1 and C2 (0.47 μF typ,). When clamp enable is set up, it is doubled below in setting voltage. In a switching regulator system, it can select he voltage stepped-up method CMOS or N-ch open drain output by LX pin from external transistor and internal capacitor (aluminum option). At that time, C2 pin is set to Input port. Note: During reset or clock stop instruction execution, V_{DB} pin set-up to V_{DD} level, and LX pin set-up to “HZ” at the time of “L” level and Nch open drain output at the time of CMOS output.	—
4	C2 [IN2]			—
5	V_{DB}			

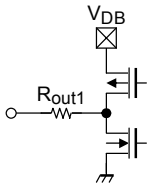
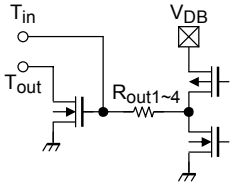
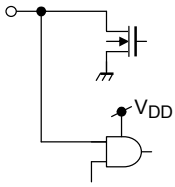
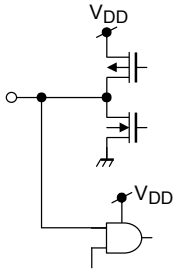
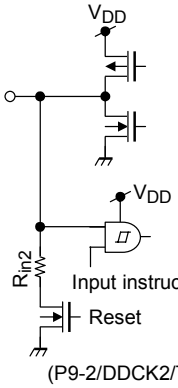
PIN No.	Symbol	Pin Name	Function and Operation	Remarks
6	C3	Doubler output pin for LCD driver	Doubler output pin for LCD driver. V_{LCD} pin output 3 V regular voltage on which twice of V_{EE} voltage by the capacitor for step-up between C3 and C4 pin. V_{LCD} potential is supplied to the I/O Port, the power supply of LCD driver, and the electronic volume power supply. Usually, the capacitor for stabilization (0.1 μF typ.) is connected between V_{LCD} pin and GND. The capacitor for step-up voltage (0.1 μF typ.) is connected to C3 and C4 pin. Note: During reset or clock stop instruction executing, V_{LCD} pin is set up as V_{CPU} power supply level.	—
7	C4			—
8	V_{LCD}			
9	V_{EE}	Constant voltage output pin	Constant voltage output pin. V_{EE} pin output 1.5 V (typ.) constant voltage power supply. V_{EE} potential is used for voltage step-up for CPU, clamp funciton of DC-DC converter and reference voltage of A/D converter. The capacitor for stabilization (0.47 μF typ.) is connected to V_{EE} pin. Note: During reset or clock stop instruction execution, V_{EE} pin is set up as high impedance.	
10	V_{CPU}	CPU power supply pin	CPU power supply pin. The voltage is appleid from 1.2 to 3.6 V. When it is necesarry memory back up, V_{DB} potential apply to this pin and hold this pin's potential. In back up state(In executing CKSTP instruction),it becomes low consumption(under 0.5 μA), it can decrease power supply until 0.75 V. If voltage is applied to this pin, the device system is reset and the program starts from address "0". (Power on reset) Note: To operate the power-on reset, the power supply should start up in under from 10 to 100 ms. Note: The power-on reset function can be enabled/disabled using the AI switch. Note: Use it by $V_{CPU} \leq V_{LCD}$.	

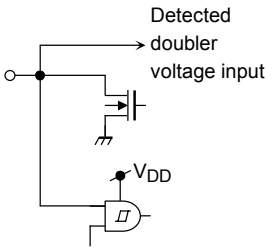
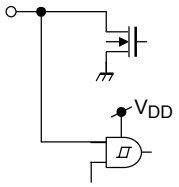
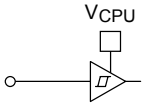
PIN No.	Symbol	Pin Name	Function and Operation	Remarks
11~14	P6-0/ A/Din1 (BRK9) ~ P6-3/ A/Din4 (BRK12)	I/O port 6 / A/D analog input	4-bit I/O ports, allowing input and output to be programmed in 1 bit units. If it is set as the input state of an I/O Port or a backup release enable state, the backup state can be canceled by changing input state in the clock stop mode and the wait mode. I/O ports are N-ch open drain output. Up to the V_{DB} voltage can be applied to the A/D input pins. Pins P6-0 to P6-3 can also be used for analog input to the built-in 6 bit, 4-channel A/D converter. The conversion time of the built-in A/D converter using the successive comparison method is 240 µs. The necessary pin can be programmed to A/D analog input in 1 bit units. Up to the doubled voltage V_{DB} ($V_{DD} \times 2$) can be input as the A/D input voltage. The A/D converter and all associated controls are performed via sortware.	 Input instruction / Back up release enable
15 ~ 18	P10-0/COM1 ~ P10-3/COM4	I/O port 10 /LCD common output	22-bit I/O ports, allowing input and output to be programmed in 1-bit units. It can be set as LCD driver output by the program. Together with COM1 to COM4 and S1 to S18 pin, a matrix is formed that can display a maximum of 72 segments. When LCD OFF bit is set to "0", all of 8 pins of P10-0 to P12-3 become LCD output of COM1 to COM4 and S1 to S4 pin. Other LCD driver combination pins (S5 to S18) can be set to LCD driver output for every pin. A drive system can select two kinds, 1/4 duty-1/2 bias system (frame frequency: 62.5 kHz) and 1/4 duty-1/3 bias system (frame frequency: 125 kHz). When 1/2 bias system is setup, common output potential is V_{LCD}, 1/2 V_{LCD} and GND. When 1/3 bias system is setup, common output potential is V_{LCD}, 1/3 V_{LCD}, 2/3 V_{LCD} and GND. If "1" is set as DISP OFF bit, common output is not select waveform and LCD display will be all switched off. P16-2 and P16-3 pin can be set as the high-speed oscillation pins Xin2 and Xout2 by the program. A 300-600 kHz ceramic oscillator or a crystal oscillator is connected to Xin2 and Xout2 pin. This oscillation clock can be changed to CPU operation clock and operate CPU at high speed. At executing clock stop instruction, an oscillation is stopped. Note: In case of changing CPU clock to a high-speed oscillator, change after 100ms or more passes after high-speed oscillator enable.	 Input instruction  (Xin2, Xout2)
19 ~ 22	P12-0/S1 ~ P12-3/S4	I/O port 12 /LCD segment output		
23 ~ 26	P13-0/S6 ~ P13-3/S8	I/O port 13 /LCD segment output		
27 ~ 30	P14-0/S9 ~ P14-3/S12	I/O port 14 /LCD segment output		
31 ~ 32	P15-0/S13 / P15-1/S14	I/O port 15 /LCD segment output		
33 ~ 36	P16-0/S15 /Xin2 ~ P16-3/S18 /Xout2	I/O port 16 /LCD segment output /High speed oscillator		

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
37 38 39 40	P3-0/SCK1 /RX1 (BRK1) P3-1/SDIO1 /TX1 (BRK2) P3-2/SI1 (BRK3) P3-3/PCTRin (BRK4)	I/O port 3 /Serial clock input/ output1/UART input1 /Serial data input/ output1/UART output1 /Serial data input 1 /Pulse counter input	4-bit CMOS I/O Port, allowing input and output to be programmed in 1bit units. When I/O port is set as input, it allows pull-up/pull down state to be programmed in 1bit units. If it is set as the input state of an I/O Port or a backup release enable state, the backup state can be canceled by changing input state in the clock stop mode and the wait mode. P3-0 to P3-2 pin is used as input/output pin of a serial interface circuit. It corresponds to 2 wired type, 3wired type and UART type. Because of selecting serial clock edge, serial clock input/output and clock frequency, it's easy to communicate and control various LSI. When interruption of a serial interface circuit is permitted, after serial interface operation is completed, interruption occurs and a program is jumped to the 4th address. P3-3 pin is used as 8bit pulse counter input PCTRin. Because of selecting standup/falling/both of edge of input and rise count/down count, it can use as an input of a tape count etc.	 Input instruction/ Release enable

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
41 42 43	P4-0/INTR1 (BRK5) P4-1/INTR2 / $\overline{\text{INH}}$ (BRK6) P4-2/BUZR (BRK7)	I/O port4 /External interrupt input1 /External interrupt input2 /PLL inhibit input /Buzzer output	8-bit CMOS I/O Port, allowing input and output to be programmed in 1bit units. When P4-0 to P4-3 port is set as input, it allows pull-up/pull down state to be programmed in 1bit units. If it is set as the input state of an I/O Port or a backup release enable state, the backup state can be canceled by changing input state in the clock stop mode and the wait mode. P4-0 and P4-1 pin is used as external interrupt input INTR1 and INTR2. When external interruption is permitted, over 3 clock of CPU (40 μs: using 75 kHz oscillator) is inputted to INTR1, INTR2 pin, interruption will occur and a program will be jumped to the 1st or 2nd address. Input interruption can select the logic of an input, rising edge/falling edge, both of edge by 1 pin. The signal inputted from INTR1 pin can measure pulse width using the 8 bits timer of insides. It can use for detection of a remote control signal etc. P4-1 pin is used as PLL inhibit input $\overline{\text{INH}}$. If $\overline{\text{INH}}$ pin is set as PLL inhibit enable state, PLL is in a stop state among "L" level of $\overline{\text{INH}}$ pin. P4-2 pin is used as the buzzer output. The buzzer output can select 4 kinds of 1/1.56/2.08/3 kHz frequencies with 4modes: continuous output, single-shot output, 10 Hz intermittent outputs and 10 Hz intermittent 1 Hz interval output. P4-3 and P5-0 to P5-3 pins are used as input/output pin of electronic volume. There are two electronic volumes and they can select of an I/O port or electronic volume for every channel. Attenuation can be controlled from 0dB to -78dB and ∞dB by 32 steps.	 Input instruction/ Release enable (P4-0 to P4-2)
44	P4-3/VRout1 (BRK8)	I/O port4 /Electronic volume output1		 Input instruction / Back up release enable (P4-3)
45 46 47 48	P5-0/VRin1 P5-1/VRcom P5-2/VRin2 P5-3/VRout2	I/O port5 /Electronic volume input1 /Electronic volume reference voltage input /Electronic volume input2 /Electronic volume output2		 Input instruction (P5-0 to P5-3)

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
49	IFin/IN	IF signal input /Input port	IF signal input pin. The input frequency is between 0.03 to 12 MHz. A built-in input amp. And C coupling allow operation at low-level input. The IF counter is a 20 bit counter with optional gate time of 4,16,32,64 ms. 20 bits data can be readily stored in memory. In Manual mode, gate On/Off can be performed using an instruction. The input pin is used as an input port (IN port). In this case, the pin is CMOS input. It can count input clocks using the IF counter. Note: When it is set as IF input and PLL of mode, the pin becomes high impedance at the time. Note: The power supply voltage of this circuit is used V_{PLL} power supply. For this reason, an input state cannot be read in the V_{PLL} power supply OFF state.	
50	V_{PLL}	PLL Power supply pin	Pin to which power is applied for PLL prescaler. Normally, the supply voltage is applied from 0.9 to 1.8 V. It becomes low consumption current at the time. Usually, it connects with VDD pin and is used.	
52	GND (PLL)			
51	OSCin	Local oscillation signal input	It is a programmable counter input pin. It can select the pulse-swallow type (HF mode) or the direct divide type (LF mode) by a program. The local oscillation output of 1 to 30 MHz is input in HF mode; 0.5 to 4 MHz in LF mode. With an input amp incorporated, capacitive-coupling, small-amplitude operation. Note: The input is at high impedance in PLL off mode.	

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
53 54	DO1/OT1/P DO2/OT2/N /Tin	Phase comparator output 1 /output port 1 /P output Phase comparator output 2 /output port 2 /N output /Tr. input for LPF	PLL phase comparator output pins. In tri-state output, when the programmable counter divider output is higher than the reference frequency, the pins output High level; when the output is lower than the reference frequency, the pins output Low level. When the outputs match, the pins go to high impedance. The doubler voltage V_{DB} is used for a phase comparator power supply and "H" level outputs the V_{DB} power supply potential. DO1 and DO2 pins are built-in 3 kinds (5 k, 50 k, and 100 kΩ) of output resistance, and can change output resistance individually. DO2 pin can change output resistance automatically according to the phase difference of PLL and then lock-up time is improvable. It can possible to high- impedance, output port (OT1, OT2) and a phase comparator charge pump control signal (P/N) by program. When it set to a phase comparator charge pump control signal (P/N) output, dividing output of programmable counter output of "H/L" level at higher than standard frequency, "L/H" level at lower than standard frequency and "L/L" level in coincidence.	 (DO1/OT1/P, DO2/OT2)  (T_{in}, T_{out}) Note: T_{in}/T_{out} setting  Input instruction (P9-0)
55 56 57	P9-0/Tout MUTE/P9-1 P9-2/DDCK2 /TEST	I/O port 9 /Tr. Output for LPF /Mute output /Clock output2 for doubler /TEST mode input	P9-1 to P9-2 pin is 2-bit CMOS I/O Port, P9-0 pin is 1-bit Nch open drain I/O allowing input and output to be programmed in 1 bit unit, P9-1 pin is used as MUTE output. Normally, MUTE output uses as muting control signal output. MUTE bit can be set to "1" by input change of an I/O Port input release (BRK) pin, and a setup of MUTE output logic can set up by the program. During system reset ($\overline{\text{RESET}}$ = "L"), P9-2 pin is pulled down and become test mode input. For this reason, to be open or input "L" level during reset condition. NchFET transistor for low path filter amplifier (5.5 V resisting pressure) can be used by program. As for FET transistor, Tin pin is set as gate input and Tout pin is set as drain output.	 Input instruction (MUTE/P9-1)  Input instruction, Reset (P9-2/DDCK2/TEST)

PIN No.	Symbol	Pin Name	Function and Operation	Remarks
58 59 60 61	P8/O port 8 /VDET (BRK13) P8-1/SI2 /DDCK1 (BRK14) P8-2/SCK2 /RX2 (BRK15) P8-3/SDIO2 /TX2 (BRK16)	I/O port 8 /Detected doubler voltage input /Serial data input2 /Doubler clock output 1 Serial clock input/output 2 /UART input2 /Serial clock input/output2 /UART output2	A port 8 is 4-bit Nch open drain I/O Port. It can control ON/OFF of an output transistor for every bit by the program. When an output is set as OFF, this pin can be used as an input port. If it is set as a backup release enable state, the backup state in the clock stop mode and the wait mode can be canceled by change of the input pin. An I/O Port is Nch open drain structure, and input and output by 5.5 V are possible for it. This pin is used and the switching regulator for VT can be constituted. It's doubled doubler clock output: DDCK1 (P8-1) or DDCK2 (P9-2), its divided voltage is input to the detected doubler voltage VDET pin (P8-0) and controlled doubler clock. DDCK1 output is a Nch output of 5.5 V resisting pressure and can be doubled Vt doubled voltage to 5 V by using external transistor. DDCK2 output is a CMOS output and can be doubled by using external transistor. The doubler clock can be select three kinds of divided frequency of a crystal oscillator, high-speed oscillator, and OSCin input. Moreover, the comparator reference potential of VDET input can be select two kinds of 0.75 V/1.0 V by the program. P8-1 to P8-3 pin is use as both input and output pin of a serial interface circuit (SIO). The serial interface circuit corresponds to 2 wired type, 3 wired type, and UART. Since serial clock edge selection, serial clock input-and-output selection, and clock frequency selection can be performed, it can do easy control of various LSI and communication between controllers. Moreover, when interruption of a serial interface circuit is permitted, after serial interface operation is completed, interruption occurs and a program is jumped to the 3rd address.	 Input instruction / Back up release enable (P8-0)  Input instruction / Back up release enable (P8-1 to P8-3)
62	$\overline{\text{RESET}}$	Reset input	Input pin for system reset signals. $\overline{\text{RESET}}$ takes place while at low level; at high level, the program starts from address "0". Normally, if voltage is applied to V_{CPU} pin, the system is reset (power on reset). Accordingly, this pin should be set to high level during operation. This IC is not built-in Power on reset circuit. In case of applying reset, make a reset pin into "L" level. Since pull-up resistor is not built in a reset pin, make a reset pin into V_{CPU} level during IC operation except the time of reset.	

Description of Operations

○ CPU

The CPU consists of a program counter, a stack register, an ALU, program memory, data memory, a G-register, a data register, a DAL address register, a carry flip-flop (F/F), a judge circuit, interrupt stuck register and an interrupt circuit.

1. Program Counter (PC)

The program counter is a 14-bit binary up counter used to address program memory (ROM). The program counter is cleared by a system reset and starts from address 0.

The PC is normally incremented by 1 at the execution of each instruction. However, executing a Jump or Call instruction loads the address specified in the instruction's operand to the PC.

When an instruction with a skip function (for example, the AIS, SLTI, TMT, and RNS instructions) is executed and the result matches the skip condition, the PC is incremented by 2 and the next instruction is skipped.

When an interrupt is received, the system loads the vector address corresponding to the interrupt.

Note: Program memory (ROM) uses the address range 0000H to 1FFFH. Access to addresses outside this range is prohibited.

Instruction	Contents of program counter (PC)													
	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
JUMP A/DDR1	0	← Instruction operand (ADDR1) →												
CALL A/DDR2	0	← Instruction operand (ADDR2) →												
DAL A/DDR3, (r) (DAL bit = 0)	0	0	0	0	← Instruction operand (ADDR3) →						← Contents of general register (r) →			
DAL (DA) (DAL bit = 1)	← DAL address register (AR) →													
RN, RNS, RNI	← Contents of stack register →													
When interrupt received	← Vector addresses for interrupt →													
Power-on reset, reset by RESET pin	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Interrupt source	Vector Address
INTR1 pin	0001H
INTR2 pin / Timer port	0002H
Serial interface / Timer port / Detective decrease voltage	0003H
Timer counter	0004H

2. Address Stack Register (ASR)

The address stack register consists of 16 × 14 bits. When a subroutine call instruction is executed or an interrupt is processed, this register stores a value equal to the contents of the program counter + 1 (that is, the return address). Executing a return instruction (RN, RNS, RNI) loads the contents of the address stack register to the program counter. The address stuck register is arranged on I/O map and can do read-out / writing by input and-output instruction. The stack register can nest to 16 stack levels.

3. ALU

The arithmetic and logic unit (ALU) has a binary 4-bit parallel addition-subtraction function, a logical operation function, a compare function, and a multiple bit judge function. The CPU does not include an accumulator; all operations directly use the contents of the data memory.

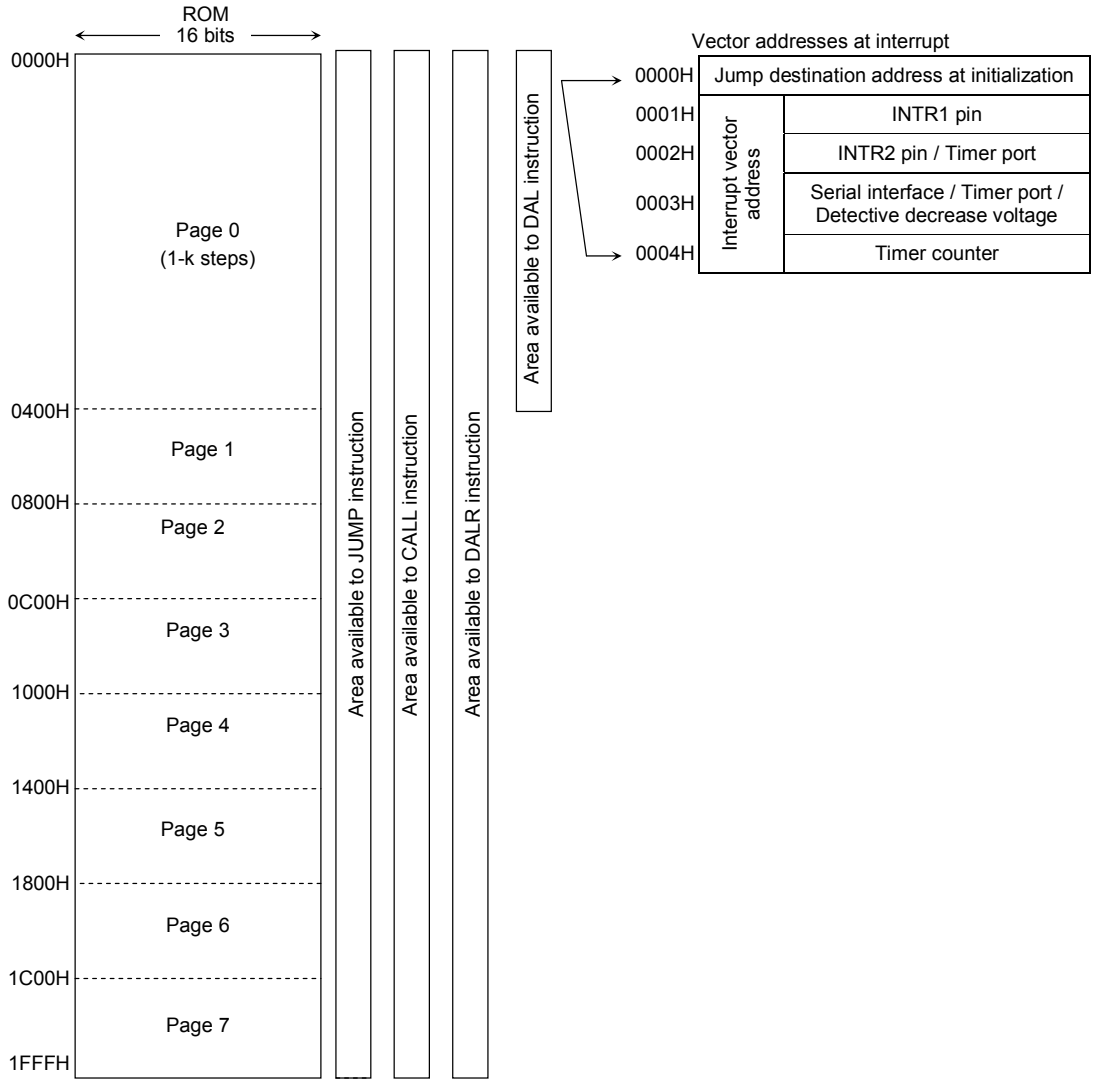
4. Program Memory (ROM)

The program memory consists of 16 bits × 8192 steps and used for storing programs. The useable address range consists of 8192 steps between address 0000H to 1FFFH.

The program memory is divided into 8192 separate steps and consists of page 0 to 7. The JUMP instruction and CALL instruction cab be freely used throughout all 8192 steps. In case of executing data refer DAL (DAL instruction), the program memory address 0000H to 03FFH (page 0) are used as data area and executing indirect refer DAL instruction (DALR instruction), the program memory address 0000H to 0FFFFH (page 0 to 3) are used as data area. The 16 bit contents of this can be loaded into the data register by executing these instructions.

Note: Set the data area in program memory to addresses outside the program loop.

Note: The program counter which designates to program memory has 14 bits and can designates program memory to 3FFF address. Do not specify not exisiting range from 2000H to 3FFFH.



5. Data Memory (RAM)

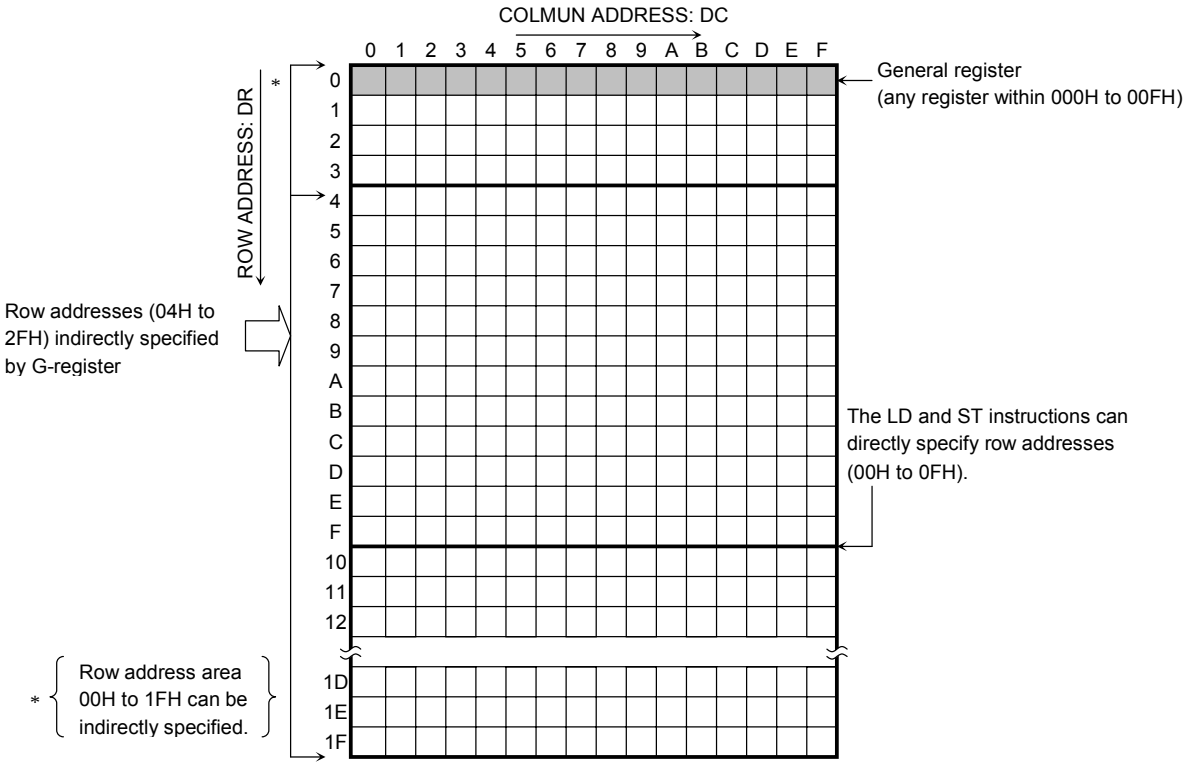
Data memory of 4 bits × 512 words and used for string data. These 512 words are expressed in row address (6 bits) and a column address (4 bits). 348 words (row address = 04H to 1FH) within the data memory are addressed indirectly by G-register. Owing to this, it is necessary to specify the row address with the G-register before the data in this area can be processed.

The address 00H to 0FH within the data memory are known as general registers, and can be used simply by specifying the relevant column address (4 bit). These sixteen general registers can be used for operations and transfers with the data memory, and may also be used as normal data memories.

Note: The column address (4 bits) that specifies the general register is thee register number of the general register.

Note: All row addresses (00H to 1FH) can be specified indirectly with the G-register.

Note: The LD and ST instructions can directly address 256 words of data memory (row address area 00H to 0FH).



6. G-Register (G-REG)

The G-register is a 5-bit register used for addressing the row address (DR= 00H to 1FH) of the data memory's 512 words. This register is arranged on I/O map and accessed by input-and-output instruction. The 5-bit contents can be directly set by execution of STIG instruction. (Refer to section in Register Ports.) The contents of this register are validated when the MVGD instruction or MVGS instruction are executed, and not affected through the execution of any other instructions. The contents of G-register is evacuated to an interruption stack register when interrupt request generates and return to G-register at the time of executing RNI instruction. (Refer to section in Interruption Stack Register.)

7. Data Register (DATA REG)

The data register consists of 1 × 16 bits and loaded with 16 bits of data from anywhere in program memory on execution of the DAL instruction. This register is used as one of the ports and the contents are loaded into the data memory in units of 4 bits when IN1 instruction from among the I/O instruction is executed. (Refer to section in Register Ports.) The contents of data register is evacuated to an interruption stack register when interrupt request generates and return to data register at the time of executing RNI instruction. (Refer to section in Interruption Stack Register.)

8. DAL Address Register (AR)

The DAL address register consists of 1 × 14 bits. When DALR instruction is executed, the data of the program memory of the address specified by the DAL address register is loaded to a data register and +1 increment of the contents of a DAL address register is carried out automatically. The contents of data register are able to transfer to DAL address register on execution of the MVAR instruction. DAL address register is arranged on I/O map and accessed by input and output instruction.
(Refer to section in Register Ports.)

9. Carry F/F (Ca Flag)

This is set when either Carry or Borrow are issued in the result of calculation instruction execution and is reset if neither of these is issued. The contents of a carry flag change is only the case where addition, subtraction, CLT, CLTC, SHRC, RORC instructions is executed and the contents do not change at the time of execution of other instructions. The contents of carry flag is evacuated to an interruption stack register when interrupt request generates and return to carry flag at the time of executing RNI instruction.
(Refer to section in Register Ports.)

10. Interrupt Stuck Resister (ISR)

This register consists of 4 × 26 bits. When interruption occurs, the contents of G-register (5 bit), data select (4 bit), carry flag (1bit) and data register (16 bit) are stored in an interruption stack register, and executes evacuation processing automatically. After an interruption processing end, these contents are execution of a RIN instruction and return to each register. The stuck level of interrupt stack register is 4 levels and nesting is 4 levels. (Refer to section in Interrupt Stuck Register.)

11. Judge Circuit (J)

This circuit judges the skip conditions when an instruction equipped with the skip function is executed. The program counter is increased in increments of two when the skip conditions are satisfied, and the subsequent instruction is skipped. There are 15 instructions equipped with a wide variety of skip functions available. (Refer to section in the items marked with a"*" symbol in the Table instruction functions and operational instructions)

12. Interrupt Circuit

An interruption circuit branches to each vector address by the demands from circumference hardware and performs each interruption processing. (Refer to section in the interruption functional item)

13. Instruction Set List

A total of 59 instruction sets are available, and all of these are single-word instructions. These instructions are expressed with 6-bit instruction code.

Upper 2 bits / Lower 4 bits		00		01		10		11	
		0		1		2		3	
0000	0	AI	M, I	TMTR	r, M	JUMP	ADDR1	SLTI	M, I
0001	1	AIC	M, I	TMFR	r, M			SGEI	M, I
0010	2	SI	M, I	SEQ	r, M			SEQI	M, I
0011	3	SIB	M, I	SNE	r, M			SNEI	M, I
0100	4	ORIM	M, I	LD	r, M*			TMTN	M, N
0101	5	ANIM	M, I					TMT	M, N
0110	6	XORIM	M, I					TMFN	M, N
0111	7	MVIM	M, I					TMF	M, N
1000	8	AD	r, M	ST	M*, r	CAL	ADDR2	IN1	M, C
1001	9	AC	r, M					IN2	M, C
1010	A	SU	r, M					IN3	M, C
1011	B	SB	r, M					OUT1	M, C
1100	C	ORR	r, M	CLT	r, M			OUT2	M, C
1101	D	ANDR	r, M	CLTC	r, M			OUT3	M, C
1110	E	XORR	r, M	MVGD	r, M			DAL	ADDR3, r
1111	F	MVSR	M1, M2	MVGS	M, r			SHRC RORC STIG SKP, SKPN RN, RNS WAIT CKSTP XCH DI, EI, RNI DALR MVAR NOOP	M M I* P M

14. Table of Instruction Functions and Operational Instructions

(Description of the symbols used in table)

M	; Data memory address Normally, one of the addresses from among addresses 00H to 03FH in the data memory.
M*	; Data memory address (256 words) One of the addresses from among addresses 000H to 0FFH in the data memory. (Effective only at the time of ST and LD instruction execution)
r	; General register An address in the data memory range 000H to 00FH.
PC	; Program counter (14 bits)
ASP	; Address stuck pointer (14 bits)
ASR	; Address stuck register (14 bits)
ISP	; Interrupt stuck pointer (2 bits)
ISR	; Interrupt stuck register (26 bits)
G	; G-register (5 bits)
DATA	; Data register (16 bits)
I	; Immediate data (4 bits)
I*	; Immediate data (6 bits; Effective only at the time of STIG instruction execution)
N	; Bit position (4 bits)
–	; All "0"
C	; Code of port (4 bits)
CN	; Code number of port (4 bits)
RN	; General register No. (4 bits)
ADDR1	; Program memory address (14 bits)
ADDR2	; Program memory address within page 0 to 3 (12 bits)
ADDR3	; Upper 6 bits of program memory address within page 0
AR	; DAL address register (14 bit)
Ca	; Carry
CY	; Carry flag
P	; Wait condition
b	; Borrow
IN1~IN3	; The ports used during the execution of instruction IN1 to IN3
OUT1 ~ OUT3	; The ports used during the execution of instruction OUT1 to OUT3
( )	; Contents of registers or data memory
[ ] C	; Contents of the port indicating code No. C (4 bits)
[ ]	; Contents of data memory indicating the register or data memory
[ ] P	; Contents of program memory (16 bits)
IC	; Instruction code (6 bits)
*	; Commands equipped with skip function
DC	; Data memory column address (4 bits)
DR	; Data memory row address (2 bits)
DR*	; Data memory row address (4 bits, Effective only at the time of ST and LD instruction execution)
(M) b0 ~ (M) b3	; Bit data of data memory contents (1 bit)

Inst-ruction set	Mnemonic		Skip function	Function Description	Operation Description	Machine language (16 bits)			
						IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Addition instruction	AI	M, I		Add immediate data to memory	M ← (M) + I	000000	DR	DC	I
	AIC	M, I		Add immediate data to memory with carry	M ← (M) + I + ca	000001	DR	DC	I
	AD	r, M		Add memory to general register	r ← (r) + (M)	001000	DR	DC	RN
	AC	r, M		Add memory to general register with carry	r ← (r) + (M) + ca	001001	DR	DC	RN
Subtraction instruction	SI	M, I		Subtract immediate data from memory	M ← (M) − I	000010	DR	DC	I
	SIB	M, I		Subtract immediate data from memory with borrow	M ← (M) − I − b	000011	DR	DC	I
	SU	r, M		Subtract memory from general register	r ← (r) − (M)	001010	DR	DC	RN
	SB	r, M		Subtract memory from general register with borrow	r ← (r) − (M) − b	001011	DR	DC	RN
Compare instruction	SLTI	M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	DR	DC	I
	SGEI	M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	DR	DC	I
	SEQI	M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	DR	DC	I
	SNEI	M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	DR	DC	I
	SEQ	r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	010010	DR	DC	RN
	SNE	r, M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	010011	DR	DC	RN
	CLT	r, M		Set carry flag if general register is less than memory, or reset if not	(CY) ← 1 if (r) < (M) or (CY) ← 0 if (r) ≧ (M)	011100	DR	DC	RN
	CLTC	r, M		Set carry flag if general register is less than memory with carry or reset if not	(CY) ← 1 if (r) < (M) + (ca) or (CY) ← 0 if (r) ≧ (M) + (Ca)	011101	DR	DC	RN

Inst-ruction set	Mnemonic	Skip function	Function Description	Operation Description	Machine language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Transfer instruction	LD r, M*		Lo A/D memory to general register	r ← (M*)	0101	DR* (4 bits)	DC	RN
	ST M*, r		Store memory to general register	M* ← (r)	0110	DR* (4 bits)	DC	RN
	MVSR M1, M2		Move memory to memory in same row	(DR, DC1) ← (DR, DC2)	001111	DR	DC1	DC2
	MVIM M, I		Move immediate data to memory	M ← I	000111	DR	DC	I
	MVGD r, M		Move memory to destination memory referring to G-register and general register	[(G), (r)] ← (M)	011110	DR	DC	RN
	MVGS M, r		Move source memory referring to G-register and general register to memory	(M) ← [(G), (r)]	011111	DR	DC	RN
	STIG I*		Move immediate data to G-register	G ← I*	111111	I*		0010
	MVAR		Move DATA register data to DAL Address register	AR← (DATA)	111111	—	—	1001
I/O instruction	IN1 M, C		Input IN1 port data to memory	M ← [IN1] C	111000	DR	DC	CN
	OUT1 M, C		Output contents of memory to OUT1 port	[OUT1] C ← (M)	111011	DR	DC	CN
	IN2 M, C		Input IN2 port data to memory	M ← [IN2] C	111001	DR	DC	CN
	OUT2 M, C		Output contents of memory to OUT2 port	[OUT2] C ← (M)	111100	DR	DC	CN
	IN3 M, C		Input IN3 port data to memory	M ← [IN3] C	111010	DR	DC	CN
	OUT3 M, C		Output contents of memory to OUT3 port	[OUT3] C ← (M)	111101	DR	DC	CN
Logical Operation instruction	ORR r, M		Logical OR of general register and memory	r ← (r) ∨ (M)	001100	DR	DC	RN
	ANDR r, M		Logical AND of general register and memory	r ← (r) ∧ (M)	001101	DR	DC	RN
	ORIM M, I		Logical OR of memory and immediate data	M ← (M) ∨ I	000100	DR	DC	I
	ANIM M, I		Logical AND of memory and immediate data	M ← (M) ∧ I	000101	DR	DC	I
	XORIM M, I		Logical exclusive OR of memory and immediate data	M ← (M) ∀ I	000110	DR	DC	I
	XORR r, M		Logical exclusive OR of general register and memory	r ← (r) ∀ (M)	001110	DR	DC	RN

Inst-ruction set	Mnemonic	Skip func-tion	Function Description	Operation Description	Machine language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Bit judge instruction	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	010000	DR	DC	RN
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	010001	DR	DC	RN
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	110101	DR	DC	N
	TMF M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = all "0"	110111	DR	DC	N
	TMTN M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = not all "1"	110100	DR	DC	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	110110	DR	DC	N
	SKP	*	Skip if carry flag is true	Skip if (CY) = 1	111111	00	—	0011
	SKPN	*	Skip if carry flag is false	Skip if (CY) = 0	111111	01	—	0011
Subroutine instruction	CALL ADDR2		Call subroutine	ASR ← (PC) 1 and PC ← ADDR2 ASP ←(ASP) + 1	101	ADDR2 (13 bits)		
	RN		Return to main routine	PC ← (ASR) ASP ←(ASR) - 1	111111	10	—	0011
	RNS	*	Return to main routine and skip unconditionally	PC ← (ASR) and skip ASP ←(ASR) - 1	111111	11	—	0011
Jump instruction	JUMP ADDR1		Jump to Address specified	PC ← ADDR1	10	ADDR1 (13 bits)		
Interrupt instruction	DI		Reset IMF (Note)	IMF ← 0	111111	00	—	0111
	EI		Set IMF (Note)	IMF ← 1	111111	01	—	0111
	RNI		Return to main routine and set IMF (Note)	PC ← (ASR) PC ← (ASR) – 1 Ca, G, DATA SELECT ← (ISR) ISP ← (ISP) – 1 IMF ← 1	111111	11	—	0111

Note: The IMF bit is an interrupt master enable flag and located on the I/O map. (Refer to the section in the interrupt functions.)

Inst-ruction set	Mnemonic	Skip func-tion	Function Description	Operation Description	Machine language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Other instructions	SHRC M		Shift memory bits to right direction with carry	0 → (M) b3 → (M) b2 → (M) b1 → (M) b0→ (CY)	111111	DR	DC	0000
	RORC M		Rotate memory bits to right direction with carry	→ (M) b3 → (M) b2 → (M) b1→ (M) b0 → (CY)	111111	DR	DC	0001
	XCH M		Exchange memory bits mutually	(M) b3 ↔ (M) b0, (M) b2 ↔ (M) b1	111111	DR	DC	0110
	DAL ADDR3, r		Load program in page 0 to DATA register (Note)	DATA ← [ADDR3 + (r)] P in page 0	111110	ADDR3 (6 bits)		RN
	DALR		Load program memory referring to DAL address register to DATA register and increments DAL address register (Note)	DATA ← [(AR)]P AR ← (AR) + 1	111111	—	—	1000
	WAIT P		At P = "0" H, the condition is CPU waiting (soft wait mode) At P = "1" H, expect for clock generator, all function is waiting (hard wait mode)	Wait at condition P	111111	P	—	0100
	CKSTP		Clock generator stop	Stop clock generator to MODE condition	111111	—	—	0101
	NOOP		No operation	—	111111	—	—	1111

Note: The lower 4 bits of the 10 bits of program memory specified by the DAL instruction (DAL ADDR3r) are used for indirectly addressing the contents of the general registers. The 13 bits of ptogram memory specified by DALR instruction are uesd for indirectly addressing.

Note: The DAL address register (AR) is located on the I/O map. (Refer to the section in the register ports.)

Note: The DAL instruction and DALR instruction execution time is two machine cycles.

O I/O Map

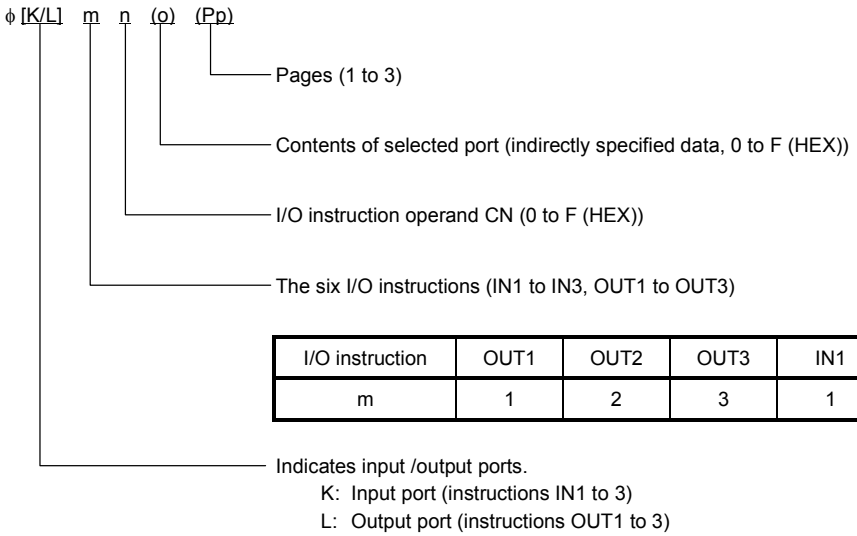
All the ports within the device are expressed with a matrix of six I/O instructions (OUT1 to 3 instructions and IN1 to 3 instructions) and 4-bit code number.
The allocation of these ports is shown on the following page in the form of an I/O map. The ports used in the execution of the various I/O instructions on the horizontal axis of the I/O map are allocated to the port code numbers indicated on the vertical axis. The G-register, data register and DAL bits are also used as ports.
The OUT1 to 3 instructions are specified as output ports and the IN 1 to 3 instructions are specified as input ports.

Note: The ports indicatedc by the angled lines on the I/O map do not actually exist within the device.
The contents of other ports and data memories are not affect ed when data is output to a non-existent output port with the execution of the output instruction. The data loaded from data memories when a non-existent input port has been specified with the execution of an input instruction becomes “1”.

Note: The outout ports marked with an asterisk (*) on the I/O map are not used. Data output to these ports assume the don’t care’s status.

Note: The Y1 contents of the ports expressed in 4 bits correspond to the data memory data’s low order bit and the Y8 contents correspond to the hig order bits.

The ports specified with the six I/O instructions and code No. C are coded in the following manner

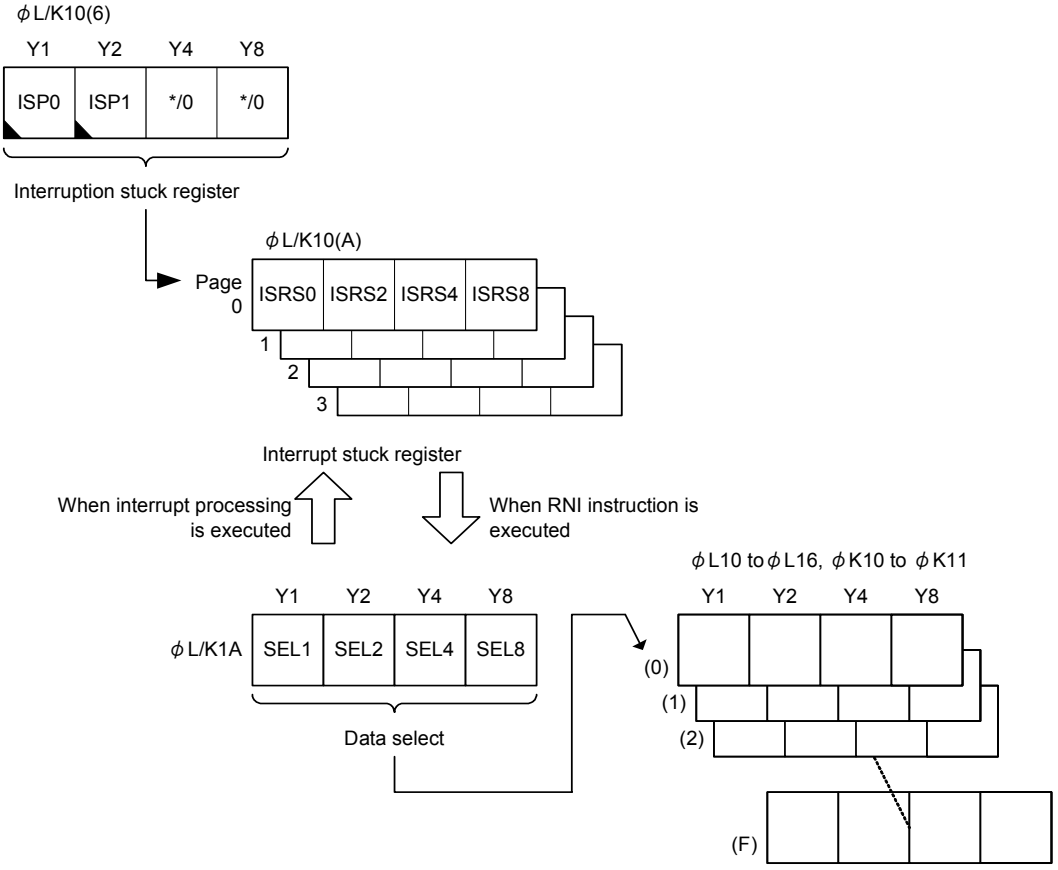


I/O instruction	OUT1	OUT2	OUT3	IN1	IN2	IN3
m	1	2	3	1	2	3

(Example): The G-register is set by the OUT1 instruction with codes 8 and 9. Therefore, the notation is ϕL18 and ϕL19.

Data port (ϕL10 to 16, ϕK10 to 11) on the I/O map is divided into 16 and is indirect designated by the contents of the data select port (ϕL/K1A). The indirect designated port is accessed OUT1 instruction which is designated to the operand [CN = 0 to 6H] or IN1 instruction which is designated to the operand [CN = 0 to 1H]. Whenever it accesses the data port, the data select port is +1 increment automatically. The data select port has 4 bit interrupt stack register.

When interrupt request generates, the 4 bit data select port is evacuated to an interruption stack register which is designated by interrupt stack pointer and return at the time of executing RNI instruction.



< Indirect specification by the data selection port >

I/O Map (IN1 (M, C), IN2 (M, C), IN3 (M, C), OUT1 (M, C), OUT2 (M, C), OUT3 (M, C))

Page 1	ϕL1				ϕL2				ϕL3				ϕK1				ϕK2				ϕK3			
	OUT1				OUT2				OUT3				IN1				IN2				IN3			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	Data port 1				Interrupt enable flag								Data port 1				Interrupt enable flag							
					EF1 (INTR1)	EF2 (INTR2/TM)	EF3 (SIO/TP/W)	EF4 (TIMER)									EF1 (INTR1)	EF2 (INTR2/TM)	EF3 (SIO)	EF4 (TIMER)				
1	Data port 2				Interrupt latch reset								Data port 2				Interrupt Latch							
					ILR1 (INTR1)	ILR2 (INTR2/TM)	ILR3 (SIOTP/W)	ILR4 (TIMER)									ILR1 (INTR1)	ILR2 (INTR2/TM)	ILR3 (SIOTP/W)	ILR4 (TIMER)				
2	Data port 3				INTR1 control		INTR2 control		I/O port 3 output data				IF data 1				Interrupt master flag				I/O port 3 input data			
					POS1	NEG1	POS2	NEG2	-0	-1	-2	-3	F0	F1	F2	F3	IMF	0	0	0	-0	-1	-2	-3
3	Data port 4				AD converter control				I/O port 4 output data				IF data 2				A/D converter data				I/O port 4 input data			
					AS SEL0	AS SEL1	AS SEL2	STA	-0	-1	-2	-3	F4	F5	F6	F7	AD0	A/D1	A/D2	A/D3	-0	-1	-2	-3
4	Data port 5				DO1 control				I/O port 5 output data				IF data 3				A/D converter data				I/O port 5 input data			
					R0	R1	M0	M1	-0	-1	-2	-3	F8	F9	F10	F11	AD4	A/D5	Busy	0	-0	-1	-2	-3
5	Data port 6				DO2 control 1				I/O port 6 output data				IF data 4				Input exclusive port input data				I/O port 6 input data			
					R0	R1	M0	M1	-0	-1	-2	-3	F12	F13	F14	F15	Unknown	IN2	Unknown	Unknown	-0	-1	-2	-3
6	Data port 7				DO2 control 2								IF data 5				STOP F/F	BUZER 10Hz	VDO OFF F/F	0				
					AUTO1	ENA	CK0	CK1					F16	F17	F18	F19								
7	LCD driver control				UNLOCK RESET			LPFON	I/O port 8 output data				IF monitor				Unlock detect				I/O port 8 input data			
	DISP OFF	LCD OFF	BIAS	*		PN	POL		-0	-1	-2	-3	Busy	MANUAL	OVER	0	UNLOCK	ENA	Unknown	Unknown	-0	-1	-2	-3
8	G-register 1				MUTE	MUTE control							G-register 1				MUTE	MUTE control			I/O port 9 input data			IN
	G0	G1	G2	G3		POL	Break	MUTE ENA					G0	G1	G2	G3		IO1	POL	0	-0	-1	-2	
9	G-register 2												G-register 2								I/O port 10 input data			
	G4	*	*	*									G4	0	0	0					-0	-1	-2	-3
A	Data select				Timer reset		Timer port interrupt control		I/O port 3 control				Data select				Timer							
	S1	S2	S4	S8	2Hz F/F	Clock	CK SEL	ENA	-0	-1	-2	-3	SEL1	SEL2	SEL4	SEL8	2Hz F/F	10Hz	100Hz	200Hz				
B	CA flag	*	*	*	Pulse counter control 1				I/O port 4 control				CA flag	0	0	0	Pulse counter data				I/O port 12 input data			
					POS	NEG	DOWN	*	-0	-1	-2	-3					PC0	PC1	PC2	PC3	-0	-1	-2	-3
C	Data-register 1 (DATA)				Pulse counter control 2				I/O port 5 control				Data-register 1 (DATA)				Pulse counter data				I/O port 13 input data			
	d0	d1	d2	d3	CTR RESET	OVER RESET	*	*	-0	-1	-2	-3	d0	d1	d2	d3	PC4	PC5	PC6	PC7	-0	-1	-2	-3
D	Data-register 2 (DATA)				Timer counter control				I/O port 16 control				Data-register 2 (DATA)				Pulse counter data				I/O port 14 input data			
	d4	d5	d6	d7	CK	PW	CR Disable	CR	-0	-1	-2	-3	d4	d5	d6	d7	OVER	0	0	0	-0	-1	-2	-3
E	Data-register 3 (DATA)				Timer counter interrupt detect data 1								Data-register 3 (DATA)				Timer counter data 1				I/O port 15 input data		0	0
	d8	d9	d10	d11	ID0	ID1	ID2	ID3					d8	d9	d10	d11	CT0	CT1	CT2	CT3	-0	-1		
F	Data-register 4 (DATA)				Timer counter interrupt detect data 2				I/O port 16 data				Data-register 4 (DATA)				Timer counter data 2				I/O port 16 input data			
	d12	d13	d14	d15	ID4	ID5	ID6	ID7	-0	-1	-2	-3	d12	d13	d14	d15	CT4	CT5	CT6	CT7	-0	-1	-2	-3

Refer to next page

ϕL/K1A

Data selection			
SEL1	SEL2	SEL4	SEL8

I/O / ϕL/K1A	ϕL10				ϕK10			
	OUT1				IN1			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	Address stack pointer (ASP)				Address stack pointer (ASP)			
	ASP0	ASP1	ASP2	ASP3	ASP0	ASP1	ASP2	ASP3
1	Address stack select				Address stack select			
	ASS0	ASS1	ASS2	ASS3	STKS0	STKS1	STKS2	STKS3
2	Address stack register 1 (ASR)				Address stack register 1 (ASR)			
	ASR0	ASR1	ASR2	ASR3	ASR0	ASR1	ASR2	ASR3
3	Address stack register 2 (ASR)				Address stack register 2 (ASR)			
	ASR4	ASR5	ASR6	ASR7	ASR4	ASR5	ASR6	ASR7
4	Address stack register 3 (ASR)				Address stack register 3 (ASR)			
	ASR8	ASR9	ASR10	ASR11	ASR8	ASR9	ASR10	ASR11
5	Address stack register 4 (ASR)				Address stack register 4 (ASR)			
	ASR12	ASR13	*	*	ASR12	ASR13	0	0
6	Interrupt stack pointer (ISP)				Interrupt stack pointer (ISP)			
	ISP0	ISP1	*	*	ISP0	ISP1	0	0
7	Interrupt stack select				Interrupt stack select			
	ISS0	ISS1	*	*	ISS0	ISS1	0	0
8	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRG0	ISRG1	ISRG2	ISRG3	ISRG0	ISRG1	ISRG2	ISRG3
9	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRG4	*	*	*	ISRG4	0	0	0
A	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRdS0	ISRdS1	ISRdS2	ISRdS3	ISRdS0	ISRdS1	ISRdS2	ISRdS3
B	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRCA	*	*	*	ISRCA	0	0	0
C	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRd0	ISRd1	ISRd2	ISRd3	ISRd0	ISRd1	ISRd2	ISRd3
D	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRd4	ISRd5	ISRd6	ISRd7	ISRd4	ISRd5	ISRd6	ISRd7
E	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRd8	ISRd9	ISRd10	ISRd11	ISRd8	ISRd9	ISRd10	ISRd11
F	Interrupt stack register (ISR)				Interrupt stack register (ISR)			
	ISRd12	ISRd13	ISRd14	ISRd15	ISRd12	ISRd13	ISRd14	ISRd15

ϕL11				ϕK11			
OUT1				IN1			
Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
DAL Address 1 (AR)				DAL Address 1 (AR)			
AR0	AR1	AR2	AR3	DA0	DA1	DA2	DA3
DAL Address 2 (AR)				DAL Address 2 (AR)			
AR4	AR5	AR6	AR7	DA4	DA5	DA6	DA7
DAL Address 3 (AR)				DAL Address 3 (AR)			
AR8	AR9	AR10	AR11	DA8	DA9	DA10	DA11
DAL Address 4 (AR)				DAL Address 4 (AR)			
AR12	AR13	TROM	*	DA12	DA13	TROM	0
Serial interface output data 1				Serial interface input data 1			
SO0	SO1	SO2	SO3	SI0	SI1	SI2	SI3
Serial interface output data 2				Serial interface input data 2			
SO4	SO5	SO6	SO7	SI4	SI5	SI6	SI7
Serial interface output data 3				Serial interface input data 3			
SO8	SO9	SOE	SOF	SI8	SI9	SIE	SIF
Serial interface control 1				Serial interface monitor 1			
M0	M1	PORT SEL	SIO	BUSY1	SOERR	RX F/F	BUSY2
Serial interface control 2				Serial interface monitor 2			
CK0	CK1	OSC0	OSC1	OCT0	OCT1	OCT2	OCT3
Serial interface control 3				Serial interface monitor 3			
MASTER	POL	NchS	SIS	ICT0	ICT1	ICT2	ICT3
Serial interface control 4							
STPS	SWENA	MSB	SOS				
Serial interface control 5							
STA0	STA1	STA2	STA3				
Serial interface control 6							
STP0	STP1	STP2	STP3				
Serial interface control 7				Decrease voltage detected voltage trimming register			
TSTA1	TSTA2	STP	F/F RESET	TR0	TR1	TR2	TR3
Decrease voltage detected control 1				Constant voltage trimming register			
WAIT ENA	INH ENA	VSTOP ENA	*	TT0	TT1	TT2	TT3
Decrease voltage detected control 2				PLL amplifier trimming register			
STOP F/F RESET	INT LB SEL	TIM SEL	BREAK ENA	TA0	TA1	TA2	TA3

ϕL/K1A

Data selection			
S1	S2	S4	S8

I/O / ϕL/K1A	ϕL12 OUT1 Y1	Y2	Y4	Y8	ϕL13 OUT1 Y1	Y2	Y4	Y8	ϕL14 OUT1 Y1	Y2	Y4	Y8	ϕL15 OUT1 Y1	Y2	Y4	Y8	ϕL16 OUT1 Y1	Y2	Y4	Y8
0	I/O port 9 output data								S13				Buzzer output control 1				IF counter control 1			
	-0	-1	-2	*					COM1	COM2	COM3	COM4	BF0	BF1	*	BEN	NC	IFin	Prescaller IN	0
1	I/O port 10 output data								S14				Buzzer output control 2				IF counter control 2			
	-0	-1	-2	-3					COM1	COM2	COM3	COM4	BM0	BM1	BUZR ON	POL	STA/$\overline{\text{STP}}$	MANUAL	G0	G1
2	I/O port 11 output data								S15				Electric volume data 1				TEST port 1			
	-0	-1	-2	-3					COM1	COM2	COM3	COM4	VR0	VR1	VR2	VR3	#0	#1	#2	#3
3	I/O port 12 output data								S16				Electric volume data 2				TEST port 2			
	-0	-1	-2	-3					COM1	COM2	COM3	COM4	VR4	*	*	*	#4	*	*	*
4	I/O port 13 output data				S1				S17				Electric volume control							
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	CH1	CH2	VR MUTE	-∞dB				
5	I/O port 14 output data				S2				S18				DC-DC converter control 1							
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	VDET SEL	0	VDET ENA	*				
6	I/O port 15 output data				S3				Interrupt priority 1		Interrupt priority 2		DC-DC converter control 2							
	-0	-1	*	*	COM1	COM2	COM3	COM4	PRI1-0	PRI1-1	PRI2-0	PRI2-1	DD0	DD1	DD2	DD3				
7					S4				Interrupt priority 3		Interrupt priority 4		DC-DC converter control 3							
					COM1	COM2	COM3	COM4	PRI3-0	PRI3-1	PRI4-0	PRI4-1	DDCK1/2	DDCK ENA	POL	*				
8	I/O port 9 control				S5				Doubler voltage control for CPU				PLL mode select							
	*	-1	-2	*	COM1	COM2	COM3	COM4	VC0	VC1	CLAMP	OSC2	HF	*	*	0				
9	I/O port 10 control				S6				I/O port 2 brake permit											
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	BP3	BP4	BP6	BP8				$\overline{\text{INH}}$ ENA				
A					S7				I/O port 3 pull-up				Programmable counter 1							
					COM1	COM2	COM3	COM4	PU30	PU31	PU32	PU33	P0	P1	P2	P3				
B	I/O port 12 control				S8				I/O port 3 pull-down				Programmable counter 2							
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	PD30	PD31	PD32	PD33	P4	P5	P6	P7				
C	I/O port 13 control				S9				I/O port 13 / Segment select				Programmable counter 3							
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	S5	S6	S7	S8	P8	P9	P10	P11				
D	I/O port 14 control				S10				I/O port 14 / Segment select				Programmable counter 4				Decrease voltage detected voltage trimming register			
	-0	-1	-2	-3	COM1	COM2	COM3	COM4	S9	S10	S11	S12	P12	P13	P14	P15	TR0	TR1	TR2	TR3
E	I/O port 15 control				S11				I/O port 15 / Segment select				Reference select				Constant voltage trimming register			
	-0	-1	*	*	COM1	COM2	COM3	COM4	S13	S14	*	*	R0	R1	R2	R3	TT0	TT1	TT2	TT3
F					S12				I/O port 16 / segment select				Clock generator control				PLL amplifier trimming register			
					COM1	COM2	COM3	COM4	S15	S16	S17	S18	INV ON	OSC2 ON	CK SEL	*	TA0	TA1	TA2	TA3

○ System Reset

The device's system will be reset when the $\overline{\text{RESET}}$ pin is subject to the "L" level or when a voltage of 0 V → 1.2 V to 3.6V is supplied to the V_{CPU} pin (power-on reset). The program will start from "0" address immediately after about 100 ms stand-by time as starting low speed oscillator has passed following system reset. The $\overline{\text{RESET}}$ terminal should be fixed at the "H" level as the power-on reset function is used under normal condition.

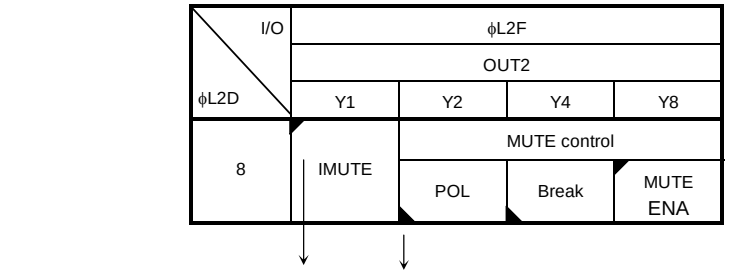
Note: The input circuit of $\overline{\text{RESET}}$ pinoperates V_{CPU} power supply andInput voltage levels is 0 V to V_{CPU}.

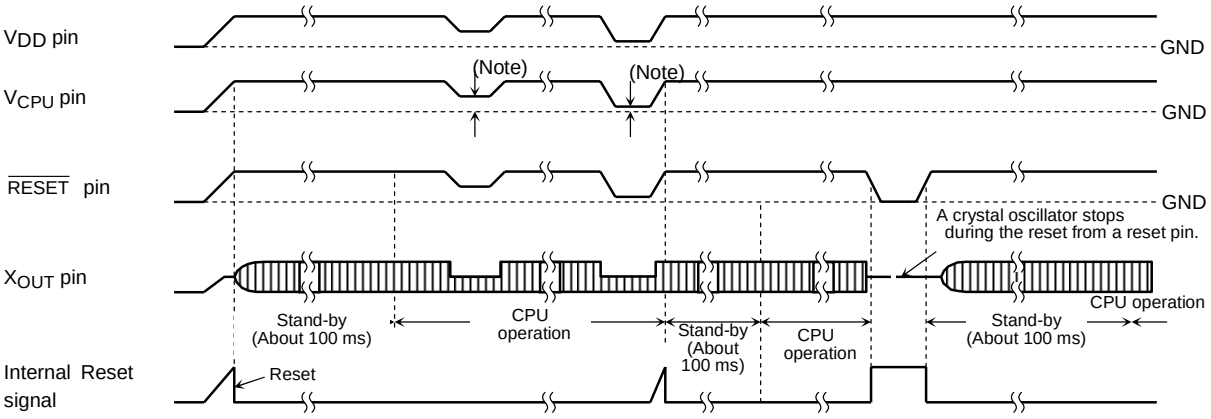
Note: A power-on reset circuit operates in the power supply standup of the V_{CPU} power supply.

Note: A power-on reset function can be forbidden with AI switch. Please specify power-on reset prohibition and specification in ES order request sheet. In addition, reset with a pin the case where a power-on reset function is forbidden.

Note: The LCD common output and the segument output will be fixed at ther "L" level during system reset and during the subsequent stand-by period.

Note: Inside shown in the above-mentioned I/O map the port that is not initialized after system reset, it is necessary to initialize port by the program. The inside port on the I/O map, the port or bit ◣ mark on I/O map is set to "0" after system reset and ◤ mark's port or bit is set to "1". No mark port or bit is unfixed.





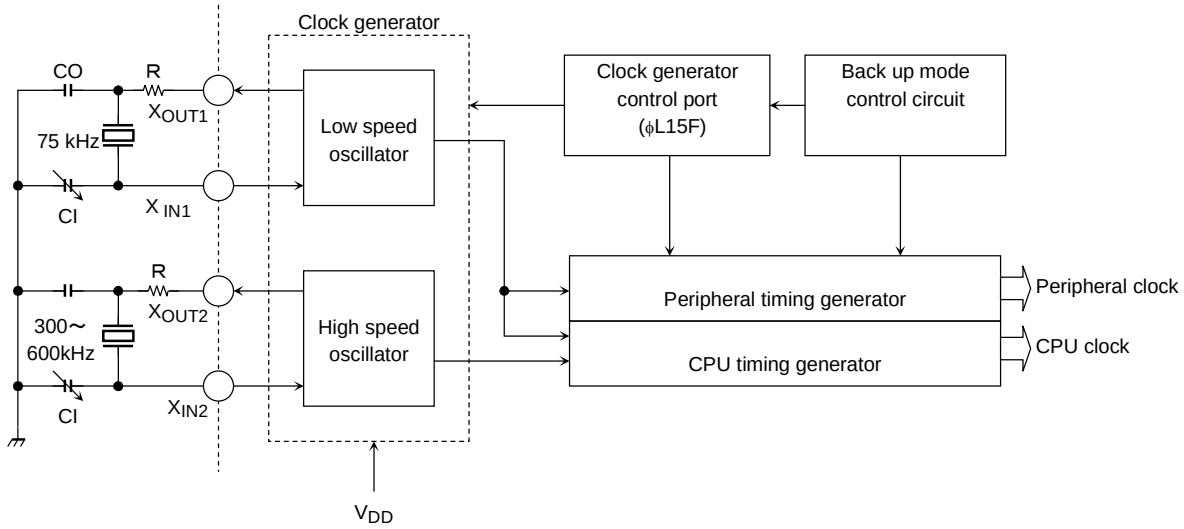
< Timing of operation >

Note: When V_{DD} power supply voltage may becomes under 0.9V or VCPU power supply voltage may becomes under 1.2V, set to clock stop mode and operates reset funciton. It will be reset if a power supply is re-impressed below from 0.3 to 0.6 V. grade. (Power-on reset)

Note: Usually, a V_{CPU} pin is supplied from doubler voltage V_{DB} pin. Refer to the backup mode item.

○ System Clock Control Circuit

System clock control circuit consists of clock generator, clock generator control port, timing generator and back up mode control circuit.



Note: It is necessary to use a crystal resonator with a low CI value and favorable start-up characteristics.

Note: Adjust and determine external resistance and the constant of a capacitor as the actually used crystal resonator.

Note: Low speed oscillator and High speed oscillator builds in schmit circuit.

Note: The power supply of low speed oscillator and High speed oscillator uses V_{DD} pin.

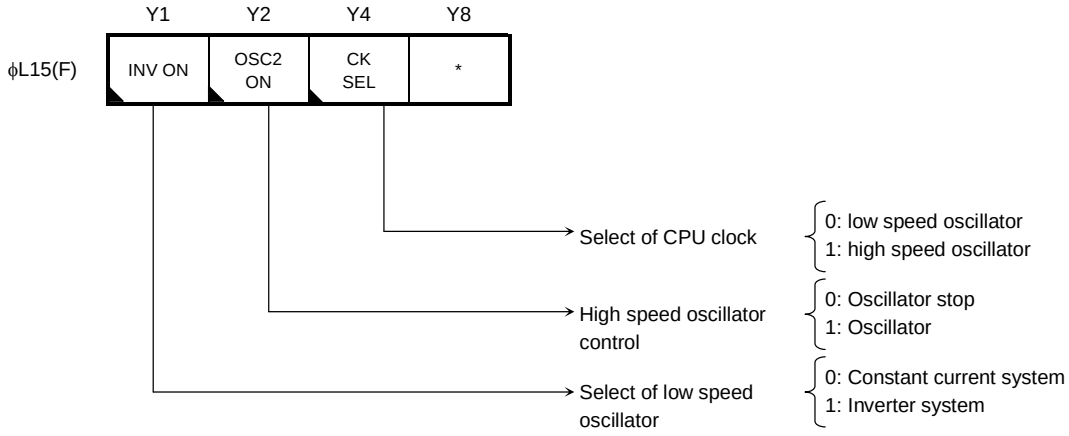
1. Clock Generator

Clock generator generates the standard clock used as the standard of the system clock supplied to a core based CPU and circumference hardware. It builds in low speed oscillator and High speed oscillator. 75kHz crystal resonator is connect to X_{IN1} and X_{OUT1} pin and 300 to 600kHz ceramic resonator or a crystal resonator is connected to X_{IN2} to X_{OUT2} pin.

CPU clock and doubler clock (V_{DB} doubler or doubler for VT) can be changed to a high-speed oscillation clock by the program. Since timer, reference frequency, etc. are using the 75 kHz clock at this time, it has neither measurement of timer time, nor the influence on PLL.

2. Clock Generator Control Port

Clock generator control port controls of low speed oscillator and high speed oscillator.



$OSC2_{ON}$ bit controls on / off of high speed oscillator. If "1" is set to this bit, high speed oscillator is permitted and an oscillation is started.

CK SEL bit changes a CPU operation clock to low speed or high speed oscillator clock. After reset, CPU operates with 75 kHz low speed clock. At the time of high-speed clock use, after setting an $OSC2_{ON}$ bit as "1" and stabilizing high speed oscillator frequency, it changes to a high speed clock. INV ON bit can change the circuit form of 75 kHz low speed oscillator. Usually, it sets to constant current type.

Note: High speed oscillatorclock can be used for doubler clock of V_{DB} pin or doubler clock for VT(DDCK1/DDCK2).

Note: Control of CK SEL bit is only the change of a CPU operation clock, in addition it does not have the influence on PLL, a timer, etc.

Note: Circuit type of 75kHz low speed oscillator is used for constant current system. If it is set as an inverter system, the output level of a crystal oscillator rises. Please use this system, only when investigating the influence of the tuner characteristic on a crystal oscillator., it uses this system.

○ DC-DC Converter for CPU

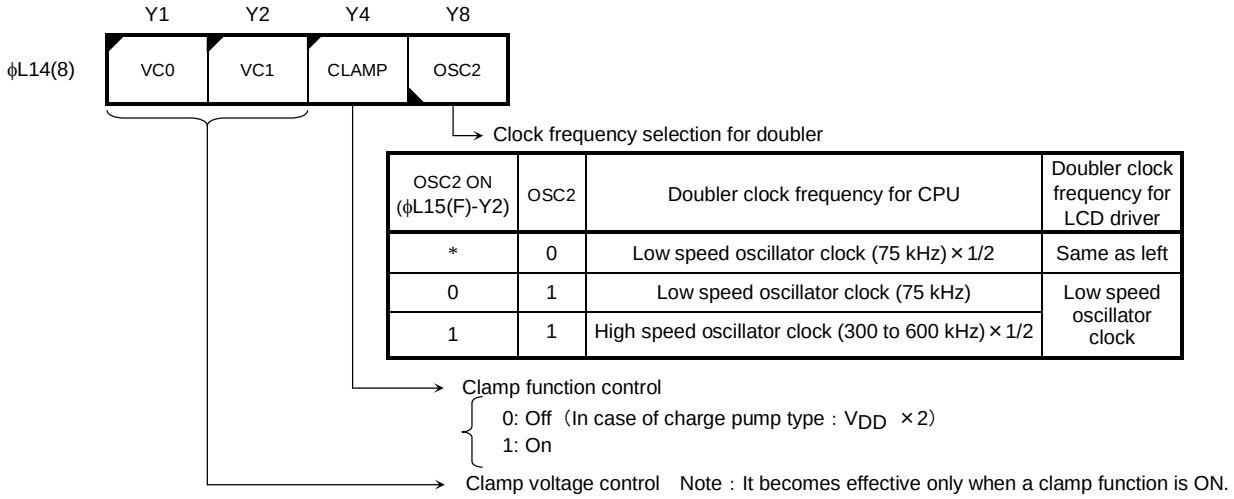
The DC-DC converter is built in as power supply for CPU. CPU doubler circuit can select two kinds of doubler system, the charge pump system by the capacitor and the switching regulator system (CMOS or Nch open drain output) with a coil by the Al option. Usually, use the charge pump system.

Switching regulator system supplies the generation electric power of the coil is supplied to V_{DB} pin and dublered by switching the Nch open drain output (LX output). In this system, the supply for the V_{DB} potential to exceed maximum rating (4.0V) is generated. In order to make it not exceed the maximum ratings, the clamp control function is built in. A clamp setup can set up the potential of 2.0, 2.5 and 3.0V by the program. Since doubler current capability can be taken as compared with a charge pump douler system, it can be used as the photo-diode for tapes, or a power supply of external IC. Furthermore, in the system which needs current capability, LX output is set to CMOS output (Al option), and dobuler with an external transistor.

The charge pump method with the capacitor charges with the V_{DD} level between C1 and C2 pin, and the doubler potential twice the V_{DD} potential is output to the V_{DB} pin. It is necessary to note it because the pressure potential decreases, too, when the twice the voltage of the V_{DD} pin decreases following the clamping setting when clamping is set by this system.

Three kinds of 1/2 frequency of 37.5 kHz, 75 kHz, and a high-speed oscillation clock can select as a doubler clock. After reset, the frequency of 37.5 kHz is outputted. Please decide the doubler clock according to the doubler ability to request.

The doubler V_{DB} potential is supplied to the A/D converter and the V_{EE} constant voltage circuit. Moreover, the V_{DB} potential is usually supplied to the V_{CPU} pin through Schottky diode.



OSC2 ON (ϕL15(F)-Y2)	OSC2	Doubler clock frequency for CPU	Doubler clock frequency for LCD driver
*	0	Low speed oscillator clock (75 kHz) × 1/2	Same as left
0	1	Low speed oscillator clock (75 kHz)	Low speed oscillator clock
1	1	High speed oscillator clock (300 to 600 kHz) × 1/2	

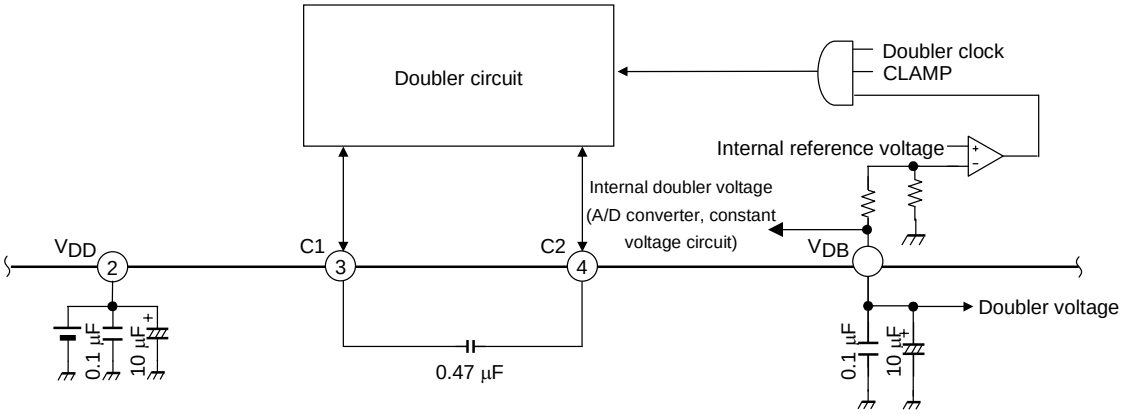
VC0	VC1	Clamp voltage
0	0	Prohibition
0	1	2.0V
1	0	2.5V
1	1	3.0V

Output type select of doubler output pin C1（Al option）

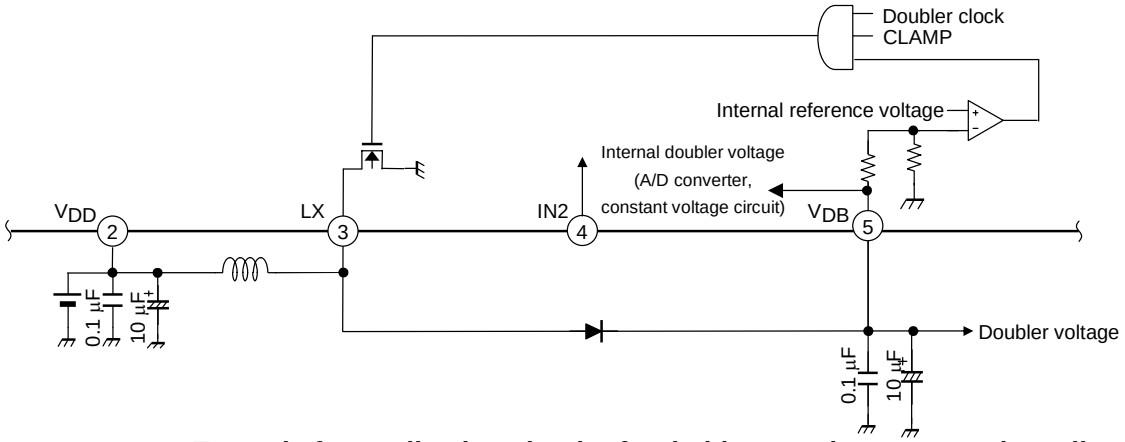
Output type	External parts	Doubler type	C1 pin status at the time of stopping doubler
CMOS	Cpacitor	Charge pump type	High impedance
Nch open drain	Coil	Switching regulator type	High impedance
CMOS	Buffer + coil	Switching regulator type	“L” level output

Note: If "1" is set to OSC2 bit, the doubler clock for LCD driver is also changed simultaneously.

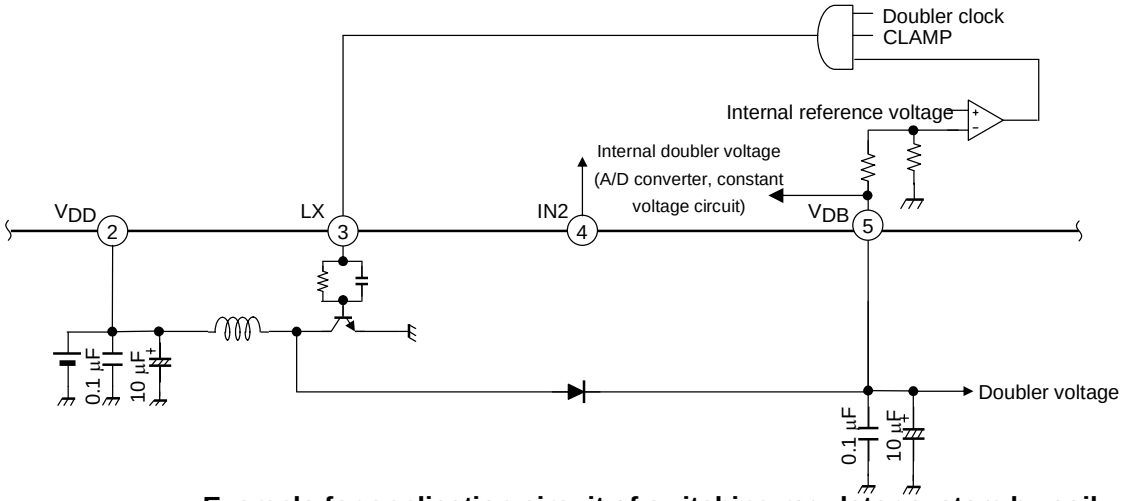
Note: When only CPU operation, we will recommend the clamping setting to be adjusted to 2.0V for the operation current decrease.



Example for application circuit of charge pump doubler system by capacitor



Example for application circuit of switching regulator system by coil
（Doubler output pin LX: Nch open drain output）



Example for application circuit of switching regulator system by coil
（Doubler output pin LX: CMOS output）

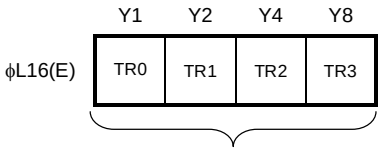
Note: In the switching regulator system, pin number 4pin can be used as an input port. Moreover, please decide the coil constant for doubler according to the doubler ability to request.

Note: The V_{DB} pin is fixed at the V_{DD} pin level while executing the clock stop instruction.

Note: The state of LX pin under clock stop instruction execution of a switching regulator system serves as the "L" level in the time of high impedance and a CMOS output by the time of Nch open drain.

○ Constant Voltage Circuit (V_{EE})

The constant voltage circuit (V_{EE}) is built in as for the reference voltage of an A/D converter, CPU and the DC-DC converter for VT, and a LCD driver. The doubler V_{DB} pin power supply for CPU is used for the constant voltage circuit and outputs the constant voltage of 1.5V from a V_{EE} pin. In order to rectify the constant voltage value V_{EE}, there is a constant voltage compensation data port and voltage can be rectified per 20mV. Do not set it to this port by the program so that this port may decide the correction data when it ships it usually.

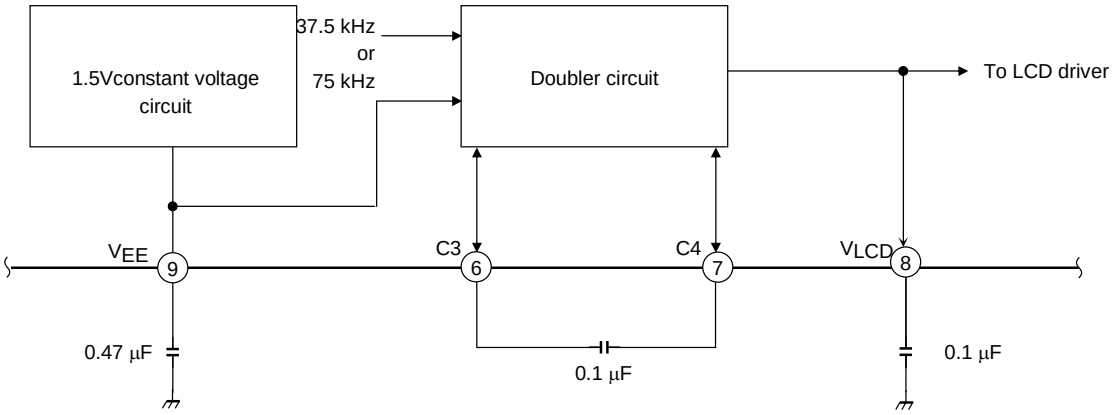


Note: After system reset, this port serves as data rectified so that it might be set to V_{EE} =1.5V at the time of shipment. For this reason, do not access this port.

Note: During reset or a clock stop, V_{EE} pin becomes high impedance.

○ LCD Driver Doubler Circuit (V_{LCD})

The doubler circuit for LCD drivers (V_{LCD}) is built in as for the power supplies of a LCD driver.
The doubler circuit for LCD drivers outputs the 3V constant voltage which doubled 1.5V constant voltage two by charge pump system doubler by the capacitor.



Note: During reset or a clock stop, V_{LCD} pin outputs V_{CPU} level.

Note: The V_{LCD} doubler potential is used also for the power supply in the I/O port etc.

Note: The doubler clock can use 37.5 kHz or 75 kHz. (OSC2 bit).

○ Back Up Mode

The backup mode decreases the operating current, holds a data memory and other register, etc. The backup mode can be backed up with hardware or the backup by the program.

The backup by the program can be changed to three kinds of backup modes by executing the CKSTP instruction or the WAIT instruction.

The backup on which hardware depends has two kinds of functions of the decrease detecting function and the power-off backup function. When V_{DD} pin power supply falls to decrease voltage detection setting (V_{DD} =0.85V to 1.225V) potential, a decrease voltage detection function stops CPU temporarily and prevents incorrect operation of CPU. At this time, the operation such as LCD driver, I/O ports, and PLL is held. If a V_{DD} pin level is set to about 0.5v or less, a power supply off-backup function will stop functions, such as a LCD driver, an I/O Port, and PLL, make the power supply only for CPU (V_{CPU} pin) low consumption current (0.5 or less uA), and hold the contents of a memory, and the state of the register of all others.

1. Clock Stop Mode

If the CKSTP instruction is executed, it becomes a clock stop mode.

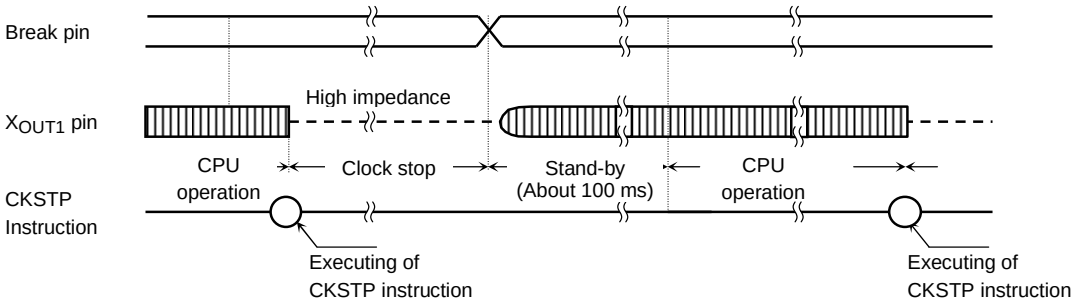
Clock stop mode is held in the state of an inside just before stopping operation of a system and stopping. At this time, V_{DD},V_{PLL} and V_{CPU} pin power supply becomes as low consumption current (10 or less uA), a crystal oscillation stops, the output pin for a LCD display and a CMOS output port are fixed to the "L" level, and Nch open drain pin is altogether fixed to OFF (high impedance) state automatically. The power supply of V_{DD} and V_{PLL} pin can be lowered to an OFF state, and V_{CPU} pin power supply can be lowered to 0.75V, respectively.

The clock stop is canceled on the following conditions.

1) I/O port which set as the break pin and input (I/O ports 3, 4, 6, and 8) pin state is changed. (Refer to I/O port functional item)
2) The V_{DD} power supply break is permitted (BRAEK ENA bit (ϕL11 (F)) ="1"), and when the power supply is turned on from off (about 0.5V or more), the V_{DD} power supply pin.

Release of clock stop mode performs the following address after the standby time progress for 100ms.

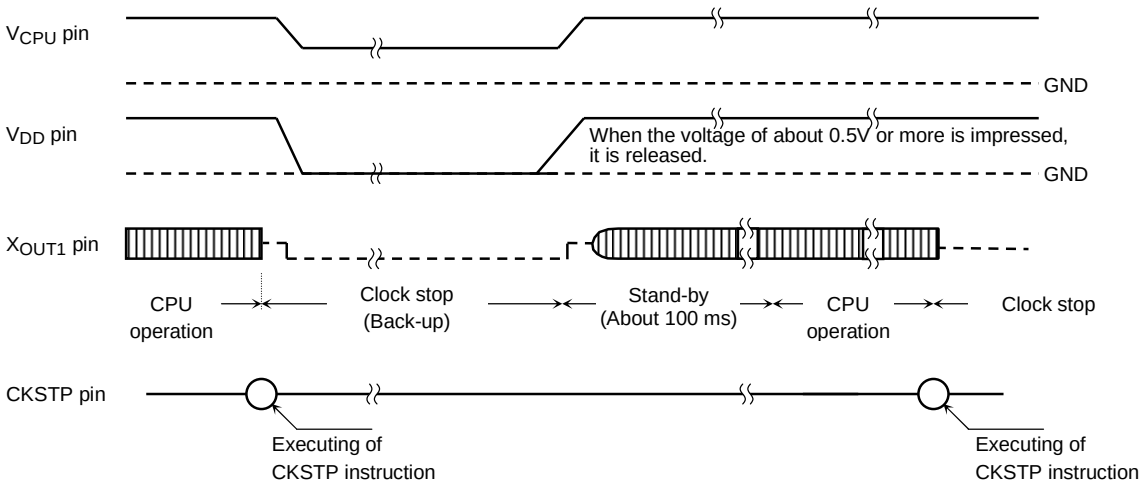
Note: During excuting CKSTP instruction, PLL becomes off state.



(Example for operating timing by Break pin)

Note: Whenever the CKSTP instruction is executed, it becomes a clock stop mode.

Note: When it is set as a break pin input, it is necessary to read this input state before CKSTP instruction execution.



(Example for operating timing by power supply pin)

Note: The release of the CKSTP instruction by on/off of the V_{DD} power supply pin should set "1" to BREAK ENA bit (ϕL11(F)). When this function is enabled, if voltage is impressed to the V_{DD} pin during CKSTP instruciton execution, it will consume about 10 μA with V_{CPU} pin. For this reason, when voltage is always impressed by the V_{DD} pin power supply, forbid this function.

Note: V_{CPU} pin needs to be potential held. Back up by the capacitor etc.

Note: It is reset that the V_{CPU} pin level decreases up to 0.75V (The typ.: 0.3V) and the voltage is impressed after that. (power-on reset)

2. Wait Mode

The wait mode suspends system operations, maintains the internal status immediately prior to suspension and decreases current consumption. In this mode, it stops at WAIT instruction execution Address at the time of hard and soft wait execution. The next address is executed immediately after the wait mode is cancelled without entering a stand-by status.

(1) SOFT WAIT mode

Only the CPU operations within the device are suspended when the WAIT instruction in which [P = 0H] has been specified in the operand is executed. The crystal resonator and other elements will continue to operate normally at this time. The SOFT WAIT mode is efficient in reducing current consumption during clock operations when used in programs that include clock functions.

The wait status is assumed whenever the WAIT instruction is executed and wait mode is canceled on the following conditions.

1) I/O port which set as the break pin and input (I/O ports 3, 4, 6, and 8) pin state is changed. (Refer to section in the I/O port functional item)
2) When the 2 Hz Timer F/F is set as “1”

Note: It enters the state of the backup when becoming off the V_{DD} power supply pin in the wait mode if set in the state of the V_{DD} power supply permission (BRAEK ENA bit (ϕL11(F)) = "1"). When the power supply is turned on (about 0.5V or more), it is released. At this time, CPU starts after standby time 100ms passes.

Note: Current consumption will differ in accordance with execution time of CPU operation.

(2) HARD WAIT mode

The operations of all elements, with the exception of the crystal resonator and doubler operating (V_{DB} / V_{LCD} pin) can be suspended by the execution of the WAIT instruction in which [P = 1H] has been specified in the operand. This enables even greater levels of current consumption reduction than the SOFT WAIT mode. It suspends the CPU operation.

During the hard wait mode, the state of output port is maintained and all the LCD output pins are fixed at the “L" level. The wait status is assumed whenever the WAIT instruction is executed and wait mode is canceled on the following conditions.

1) I/O port which set as the break pin and input (I/O ports 3, 4, 6, and 8) pin state is changed. (Refer to section in the I/O port functional item)
2) The V_{DD} power supply break is enabled (BRAEK ENA bit (ϕL11(F)) ="1" and when V_{DD} power supply pin is turned on from turn off status (about 0.5V or more).

Note: When the power supply is turned on from off (about 0.5V or more), the V_{DD} power supply pin is released in the wait mode when the V_{DD} power supply break has been enabled (BRAEK ENA bit (ϕL11(F)) ="1").

Note: The PLL OFF status will be assumed during the wait mode.

Note: During wait mode, the power supply doubler circuit (V_{DB} pin), the constant voltage supply circuit for LCD (V_{EE} pin) and the doubler circuit for LCD (V_{LCD} pin) are operating.

3. Back Up Mode by Hardware

The backup mode by hardware detects the power supply voltage level of a V_{DD} pin and makes it backup mode. The backup function by hardware has two kinds, a detected decrease voltage function and a power supply OFF detection function.

(1) Detected decrease voltage function

Detected decrease voltage function detects the V_{DD} pin level, makes CPU operation stop and prevents incorrect operation of CPU operation. If a V_{DD} pin level becomes below detected decrease voltage setting (V_{DD} = 0.85V to 1.225V) potential when the detected decrease voltage function is enabled, CPU operation will be stopped, and if it becomes again more than setting voltage, CPU will restart. Except that CPU stops, regular operation of the other functions is regular operation.

Decrease voltage operation performs detection operation to intermittence. The frequency of detection can be selected by the program and they are 1 time or 16 instructions to 2 instructions. It detects at a rate of 1 time. Selected a setup by the speed and consumption current of power supply change.

The detection voltage can set 25mV interval within the range of V_{DD} = 0.85V to 1.225V. Set it according to the specification. Since stop operation of CPU operation can be forbidden, the battery residual quantity level of 0.85V to 1.225V within the range is detected by carrying out variable of the detection setting voltage and detecting a detection flag. In this case, execute a backup instruction after detection of the minimum voltage level for incorrect operation prevention of CPU.

In case of permitting interruption, when VSTOP F/F bit is set to “1”, interruption will be published. If interruption is received, a program will branch to 0003H address.

It can be made PLL off-mode at the time of detected decrease voltage. For this reason, it is quickly at the time of a power supply fall. PLL can be stopped.

It is detectable to have become a stop or below detection voltage with VSTOP F/F bit. If this bit is detected, it will be set to "1" and will be reset by execution (STOP F/F Reset ="1") of flag reset.

Thus, when the V_{DD} potential (voltage of the battery) is decreased, various operation settings are possible by the program.

Note: Interruption of detected decrease voltage circuit is used both serial interface and timer port. When this interrupt is used, the interrupt function of the cereal interface and the timer port cannot be used.

(2) Detected power supply OFF function

Detected power supply OFF function detects the power supply OFF at the time of battery exchange etc., and CPU circuit (V_{CPU} pin) is changed into a backup state and holds it.

The detected power supply off function is enabled (BRAEK ENA bit (ϕL11(F)) ="1" and All the function stops when V_{DD} pin level is about 0.5V or less. At that time, V_{CPU} pin power supply becomes low current consumption (0.5uA or less), output pin for LCD and CMOS output port become "L" level , N channel Open drain pin becomes off (high impedance) status automatically fixed and become PLL off modes. If a power supply is switched on again, CPU will operate after the standby time for 100ms. It is detectable that the power supply was turned off with V_{DD} OFF F/F bit.

Note: Make V_{DD} pin level into a GND level at the time of power supply OFF. If V_{DD} level potential remains, current will be consumed with a V_{CPU} pin.

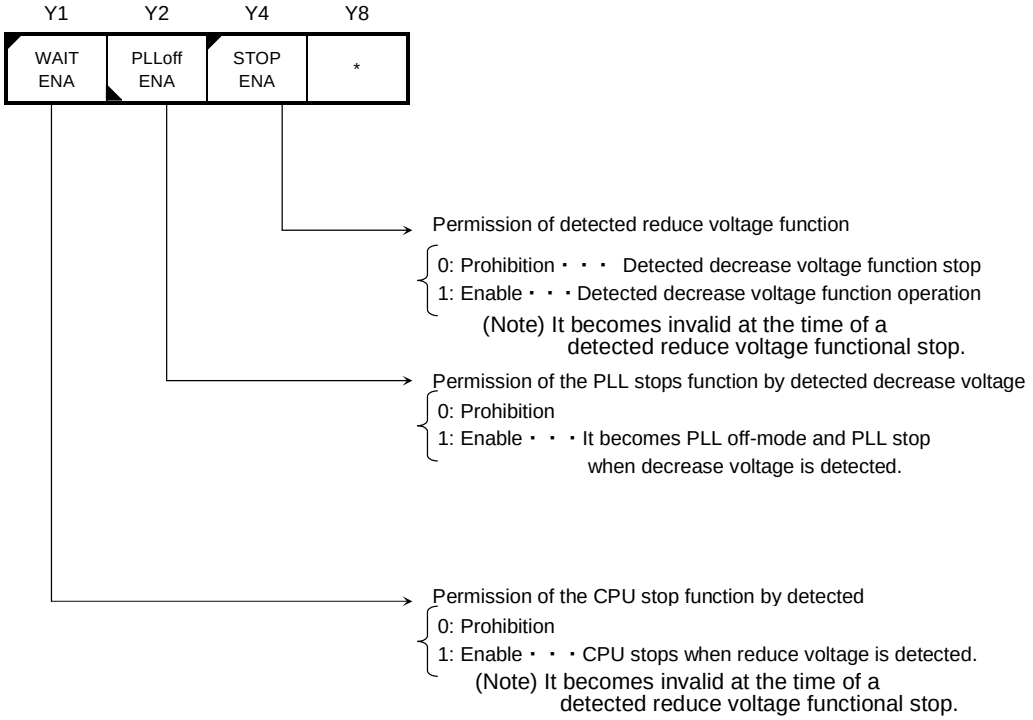
Note: BRAEK ENA bit (ϕL11(F)) permits VDD power supply break and power supply OFF detection function.

Note: Use this function using it together with the detected decrease voltage function.

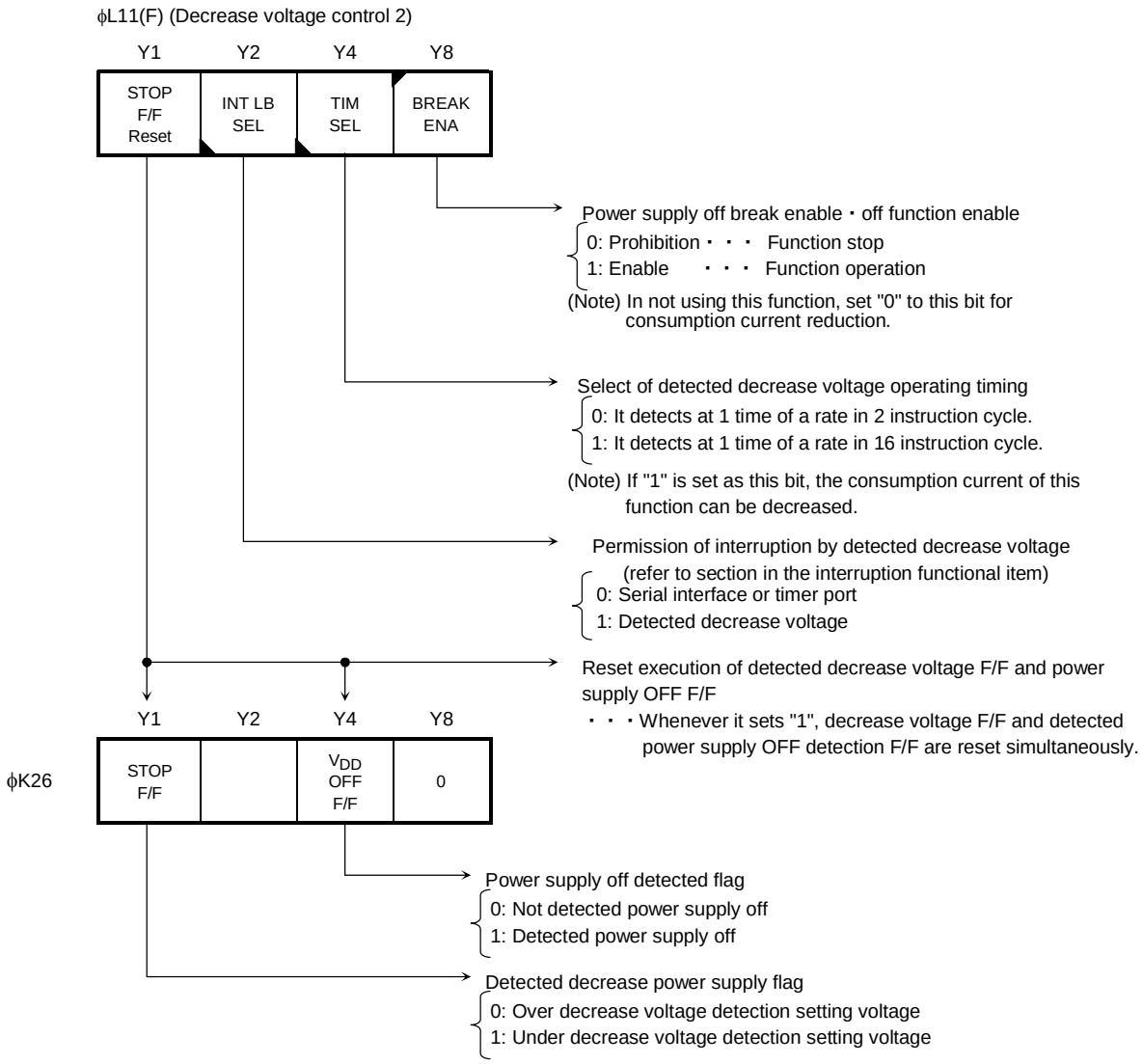
(3) Backup control register by hardware

Detected decrease voltage and a power supply OFF detection function control by access of decrease voltage control port (ϕL11 (E), ϕL11 (F)), detected decrease voltage setting data port (ϕL16(D), ϕK11(D)) and a flag register (ϕK26).

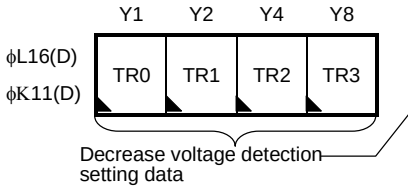
ϕL11(E) (Decrease voltage control 1)



Note: In not using decrease voltage detection function, please set "0" to a WAIT ENA bit for consumption current reduction.



Note: After ststem rtset, CKSTP instruciton release and detecting OFF by power supply off detedction circuit, STOP F/F becomes reset status during CPU standby time (100ms). V_{DD} OFF F/F is reset by "0" after system reset.



TR3	TR2	TR1	TR0	Data (HEX)	Decrease voltage detection voltage (V)
0	0	0	0	0	0.850
0	0	0	1	1	0.875
0	0	1	0	2	0.900
0	0	1	1	3	0.925
0	1	0	0	4	0.950
0	1	0	1	5	0.975
0	1	1	0	6	1.000
0	1	1	1	7	1.025
1	0	0	0	8	1.050
1	0	0	1	9	1.075
1	0	1	0	A	1.100
1	0	1	1	B	1.125
1	1	0	0	C	1.150
1	1	0	1	D	1.175
1	1	1	0	E	1.200
1	1	1	1	F	1.225

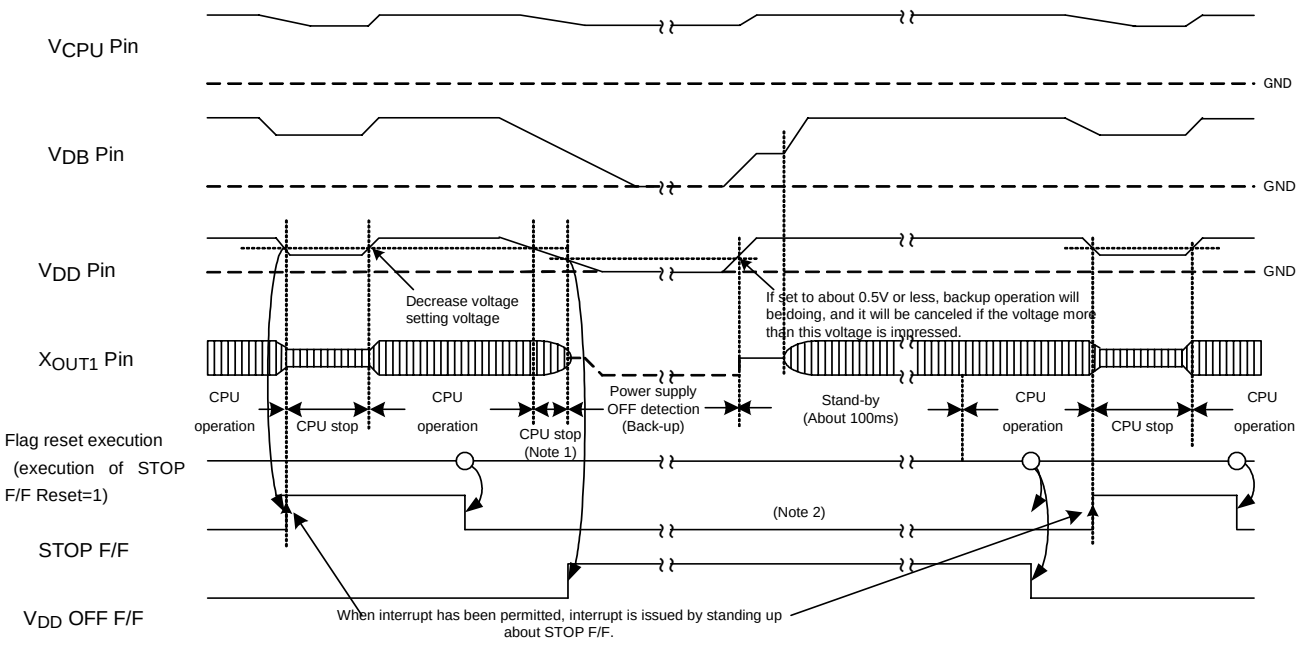
Note: Decrease voltage detection voltage detected V_{DD} pin level.

Note: If it becomes under decrease voltage detection voltage, STOP F/F will be set to "1" and CPU by decrease voltage detection will stop.

Note: Decrease voltage detection value is a standard value. The constant voltage of V_{EE} pin is used for the standard voltage of a decrease voltage detection circuit. Since variation produces this V_{EE} voltage with a product, a decrease voltage detection value also varies simultaneously.

Note: When a high-speed oscillator clock is used for a CPU clock, set up decrease voltage setting data between 0H to 6H (0.85V to 1.00V). Do not set excluding this.

(4) Decrease voltage detection, Power supply OFF detected timing

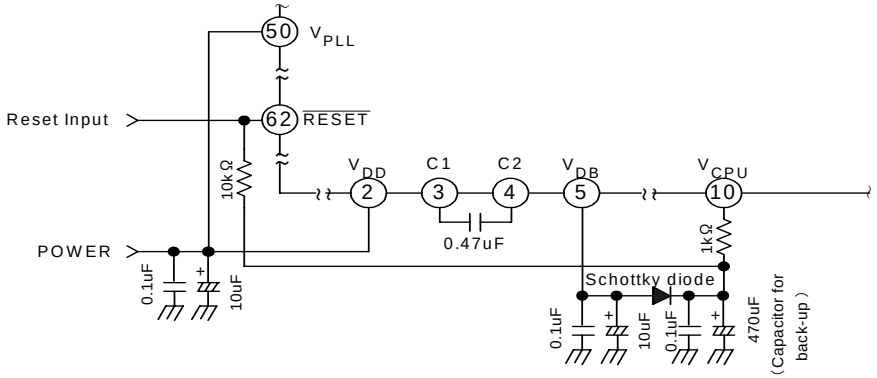


(Example for Timing operation)

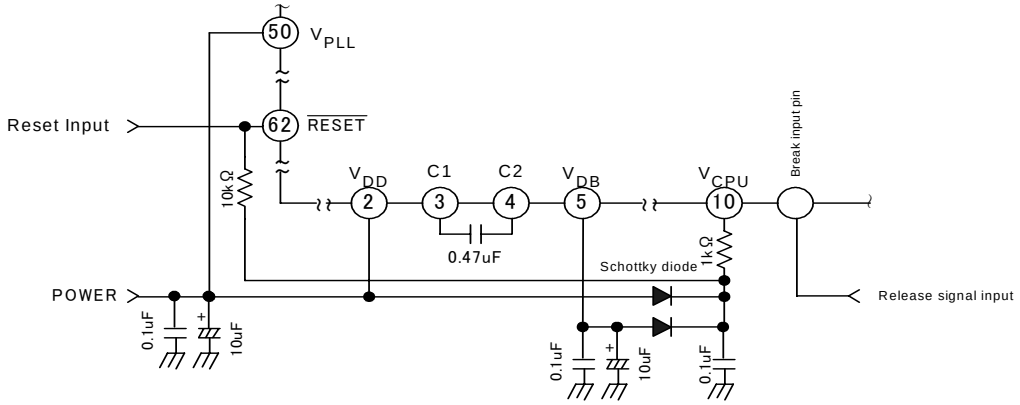
Note1: Decrease voltage detection voltage is detected and CPU operation is made to stop. Then, it is necessary to detect V_{DD} power supply voltage. For this reason, when you perform power supply OFF, please prepare the falling time more than decrease voltage detection operation timing time (two or 16 instructions) for the time from decrease voltage detection voltage to power supply detection (about 0.5 V). It becomes the cause of CPU incorrect operation.

Note2: STOP F/F is reset during standby time.

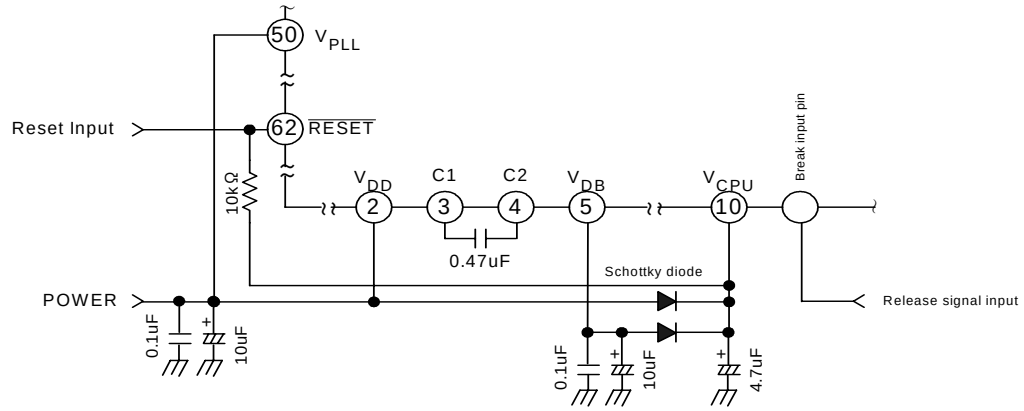
(5) Back up circuit



(Example of capacitor back-up circuit)



(Example of battery back-up circuit -1)



(Example of battery back-up circuit -2)

Note: When a CKSTP/WAIT instruction performs backup operation, please perform release operation by the release signal input if needed. Please remove the V_{CPU} pin resistance like example 2 of the above-mentioned circuit at the time of executing the CKSTP instruction.

Note: The diode use Schottky diode that VF is low, and the reverse-Leake current is small.
Recommended diode : 1SS357, 1SS393

Note: Set the capacity value to the capacitor for the backup according to the requested backup time.

Note: The "H" level of reset input needs to impress a V_{CPU} level. For this reason, make it into high impedance at the time of reset-off.

Note: The V_{CPU} pin power supply is logic power supply, such as timing circuit, ALU, data memory, and all registers. Usually, Hold V_{CPU} pin power supply at the time of backup.

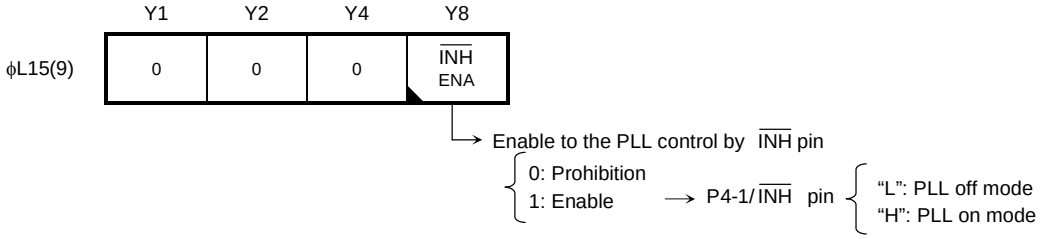
4. PLL OFF Mode

PLL can be turned on / turned off according to the contents of a reference selection port. If all the contents of a reference selection port are set as "1", it will become PLL off-mode.
(Refer to section in Reference frequency divider.)

When "1" is set to the $\overline{INH}$ ENA bit, PLL can be turned on/off with the $\overline{INH}$ pin. $\overline{INH}$ pin input serves as PLL off-mode on the "L" level, and serves as PLL on-mode on the "H" level. As a result, when the batteries are exchanged, it is possible to set it to PLL off mode quickly. It is accessed by the OUT1 instruction with which this data specified 9h to be a data selection port (ϕK/L1A) and specified [CN=5H] to be an operand part, respectively.

Moreover, it can be made PLL off-mode by decrease voltage detection.
(Refer to section in 3. Back up mode by hardware)

V_{PLL} pin serves as low consumption current at the time of PLL off-mode. Moreover, power supply for a V_{PLL} pin can be turned off at this time.



Note: At the time of clock stop mode, hard wait mode, and OFF by the power supply OFF detection function, it becomes PLL off-mode.

Note: V_{PLL} pin power supply is prescaler and programmable counter power supply. When only V_{PLL} pin power supply is turned off, the setting method of dividing frequency and the value of dividing frequency are maintained because the V_{CPU} power supply is used. Moreover, the V_{PLL} pin impression voltage level can impress the power supply to PLL regardless of V_{DD} pin or the potential of V_{CPU} pin when it is on.

Note: $\overline{INH}$ input pin is used also P4-1 pin. when $\overline{INH}$ input permission is carried out and an external interruption function (INTR2) and a break function are permitted, the function becomes effective. Moreover, input state can be judged by reading the P4-1 input data of an I/O Port 4 input port (ϕK33).

Note: I/O port control port of P4-1 pin becomes invalid and enters the state of the input compulsorily if $\overline{INH}$ input permission is done.

Note: Set "0" as the Y1/Y2/Y4 bit of the above-mentioned port.

○ Register Port

G-register, data register and DAL address register stated by explanation of CPU is arranged on the I/O map, and is treated with as one of the internal ports. Carry flag can also be accessed from an I/O map. (Refer to section in I/O access of stack register.)

G-register, carry flag, and data register have the 4-page interrupt stack register corresponding to four stack levels (four levels) among these registers. These contents interrupt with the contents of a data selection, at the time of interruption processing execution, are stored automatically, and return to a stack register automatically at it at the time of RNI instruction execution. (Refer to section in interrupt stack register.)

1. G-Register (ϕL/K18, ϕL/K19)

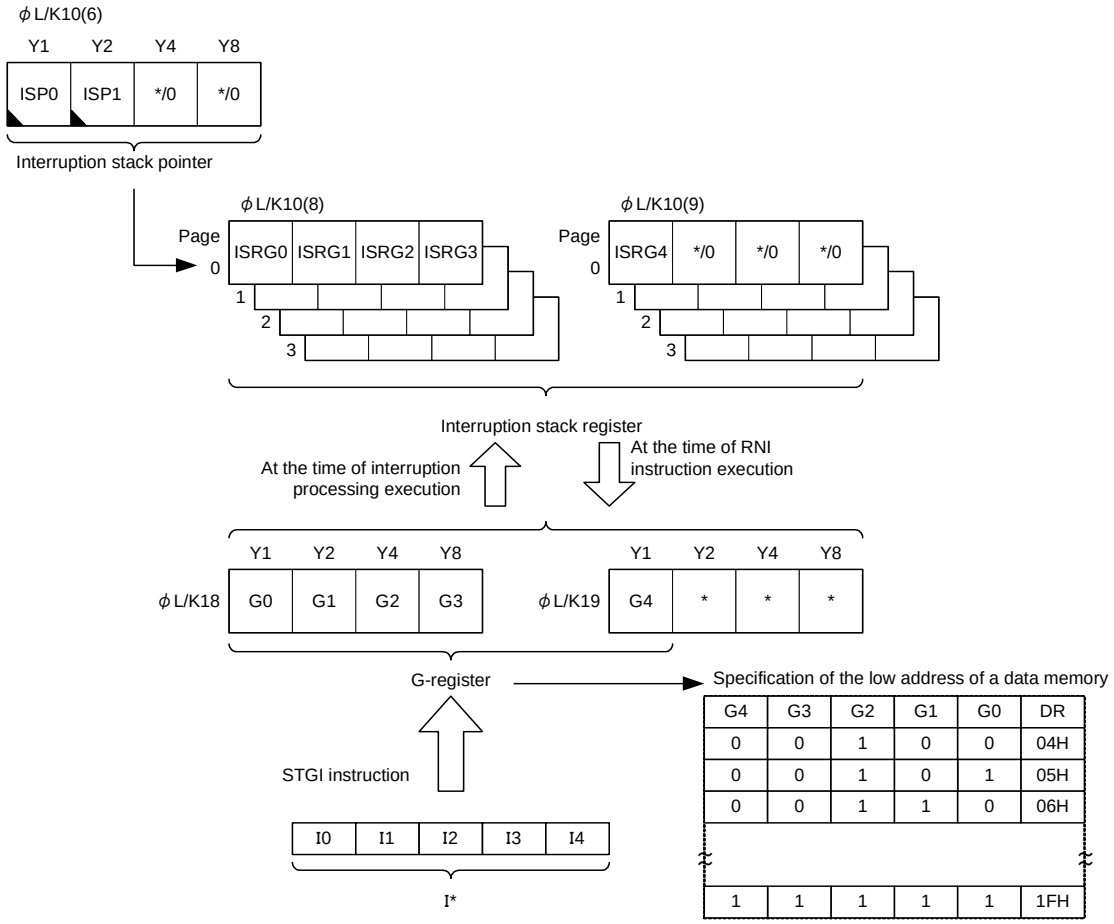
This register addresses the data memory's row addresses (DR = 04H to 1FH) during execution of the MVGD instruction and MVGS instruction. This register is accessed with the OUT1/IN1 instruction for which [CN = 8H to 9H] has been specified in the operand. Moreover, if STGI instruction is used, data can be set to this register by one instruction.

This register has the interruption stack register of four levels. It is evacuated to the interruption register which the contents of G-register interrupted at the time of interruption issue, and was specified to be it with the stack pointer, and returns by RNI instruction.

Note: The contents od this register are only valid when the MVGD instruction and MVGS instruction are executed and are ineffective when any other instruciton is executed. Moreover, it does not have the influence on this register by MVGD instruction and MVGS instruction.

Note: All of the data memory row addresses can be specified indirectly by setting data 00H to 1FH in the G-register. (DR = 00H to 1FH)

Note: Writing and reference are possible for the contents of the interruption stack registers ISRG0 to ISRG4 (ϕL/K10(8), ϕL/K10(9))at a program.

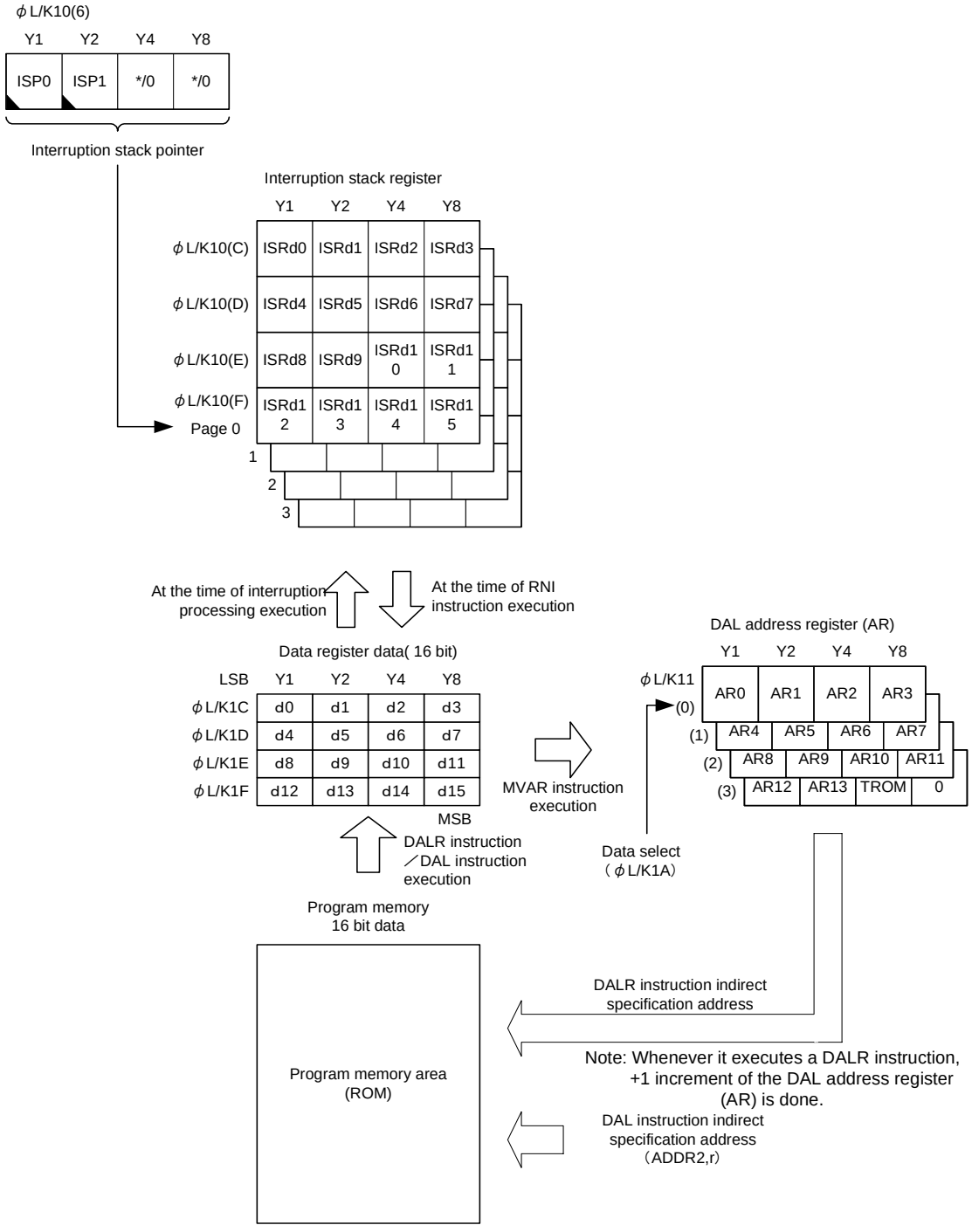


G4	G3	G2	G1	G0	DR
0	0	1	0	0	04H
0	0	1	0	1	05H
0	0	1	1	0	06H
1	1	1	1	1	1FH

1. Data Register (ϕL/K1C to ϕL/K1F), DAL Address Register (ϕL/K11(0) to ϕL/K11(3)) and Control Bit

The data register is 16-bit register for which load the program memory data when the DAL, DALR instruction is executed. The contents of this register are loaded into the data memory in 4-bit units with the execution of the OUT1/IN1 instructions for which [CN = CH to FH] has been specified in the operand. This register can be used for loading LCD segment decoding operations, radio band edge data and the data related to binary to BCD conversion.

The data register has the interruption stack register of four levels. It is evacuated to the interruption register which 16 bits of a data register interrupted at the time of interruption issue, and was specified to be it with the stack pointer, and returns by RNI instruction.



DAL address register (AR) is a register that specifies the program memory indirect when the DALR instruction is executed by the register in 16 bits.

There are two kinds of commands which load the data of a program memory, DAL instruction and DALR instruction. As for the DAL instruction, the content of ADDR2 (six bits) in the operand part and General register (r) becomes the reference address of the program memory. As for the DALR instruction, 14 bits of the DAL address register become the reference addresses. When the DAL instruction is executed, it becomes the reference area to program memory area (000H0 to 3FFH). All the areas in the program memory area can be referred to by executing the DALR instruction. Whenever the DALR instruction is executed, the content of the DAL address register is done by +1 increment. Therefore, data can continuously be loaded.

Moreover, the content of the data register can be transmitted to the DAL address register in 14 bits by one instruction by executing the MVAR instruction.

The content of the DAL address register can be accessed by executing the OUT1/IN1 instruction that specifies [CN=1H] for the operand part in four bits. DAL address register port is divided and indirect specified by the data selection port (ϕL1A) and set. The data of the specified port to set beforehand is set and the data port corresponding to it is accessed. Whenever this port (ϕL/K11) is accessed, the data selection port is done by +1 increment. For this reason, after setting up a data selection port, it can access continuously.

Note: The DAL address register becomes effective only the execution of the DALR instruction and becomes unrelated at the time of other instruction execution. There is no influence on the DAL address register by the DAL instruction.

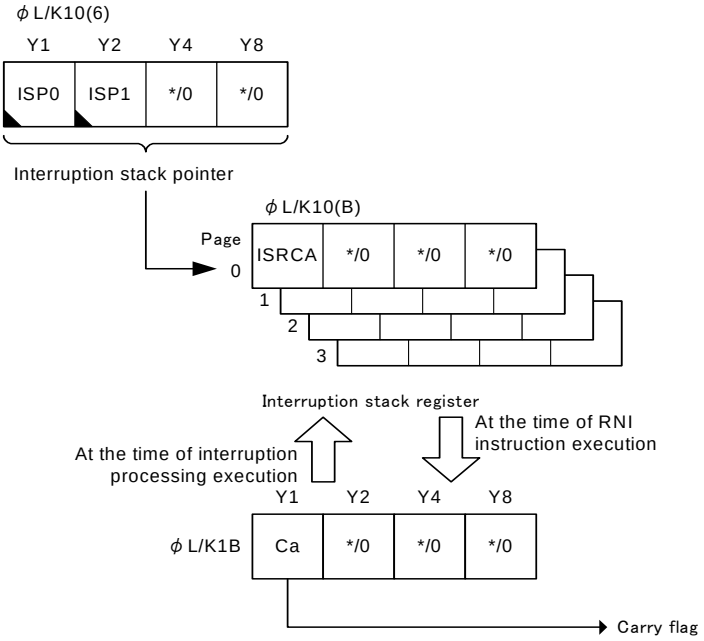
Note: For this product have 8k step of ROM capacity, if 2000H to 3FFFH is specified to be DALR instructionis executed, the contents of a data register wil become unfiexed.

Note: Rewriting and reference are possible for the contents of the interruption stack registers ISRd0 to ISRd15 (ϕL/K10(C to F)) at a program.

2. Carry Flag (ϕL/K1B)

This is set when either Carry or Borrow are issued in the result of calculation instruction execution and is reset if neither of these is issued. The carry flag is accessed with OUT1/IN1 instructions for which [CN=BH] have been specified.

There is an interruption stack register of four levels in a carry flag. At the time of interruption issue, it is evacuated to the interruption register specified with the interruption stack pointer, and this bit returns by RNI instruction.



○ Stack Register

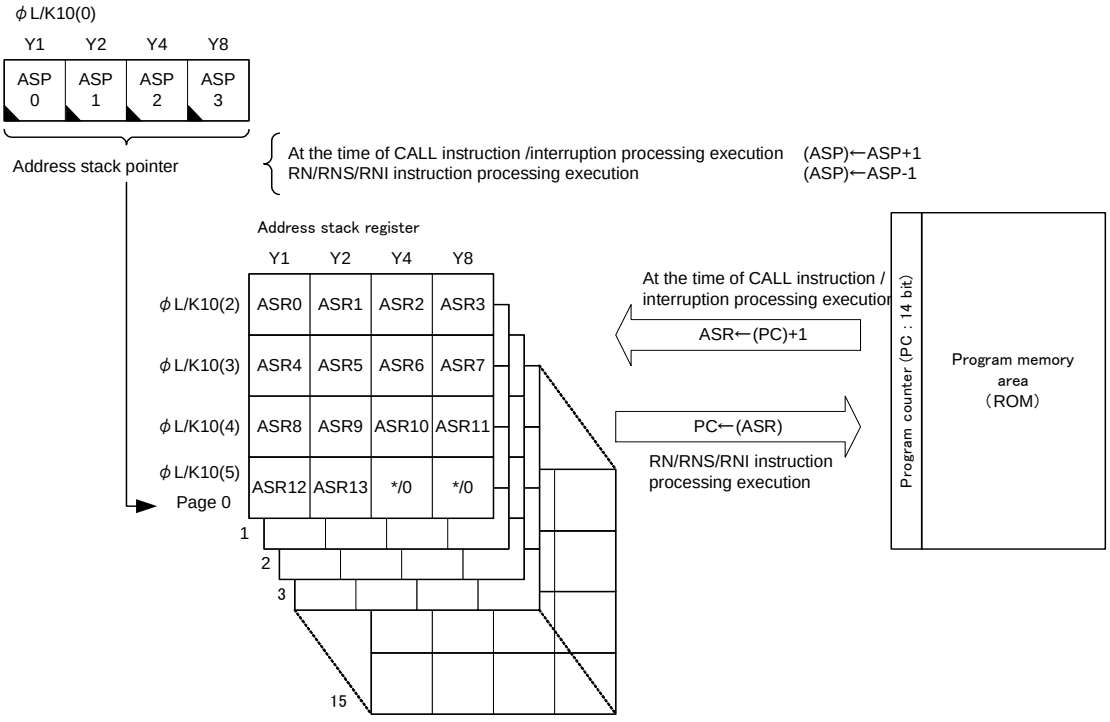
Stack register consists of address stack register (ASR) and interruption stack register (ISR). A stack register is used at the time of sub routine call instruction execution and interruption processing execution. Interruption stack register are 26 bits of the contents of G-register, data select, carry flag and data register as register port item and I/O port map mentions. Interruption stack register is 26 bits of a register port item, G-register stated on the I/O map, a data selection, a carry flag, and a data register. The address stuck register is arranged on I/O map and can do read-out / writing by input and-output instruction.

1. Address Stack Register (ASR)

Address stack register (ASR) is a register on 14 bits × page 16. When the subroutine call instruction and the interrupt processing are executed, +1 value that the content of the program counter did, that is, the return address is stored in the address stack register. At the time of interruption processing execution, the return address which is an interruption processing execution address is stored in an address stack register. This register consists of 16 pages and is specified by 4 bits of an address stack pointer (ASP). If transmitted to an address stack, an address stack pointer will be carried out -1. The subroutine or after interrupt is processed, the address stack pointer is done by +1 increment by the RN/RNS instruction or the RNI instruction, the content of the address stack register is transmitted to the program counter, and the program returns from the subroutine or the interrupt processing.

An address stack register is 16 pages and nesting serves as 16 levels.

The address stack register and the address stack pointer are arranged on the I/O map, and reference/rewriting is possible for them in these contents.



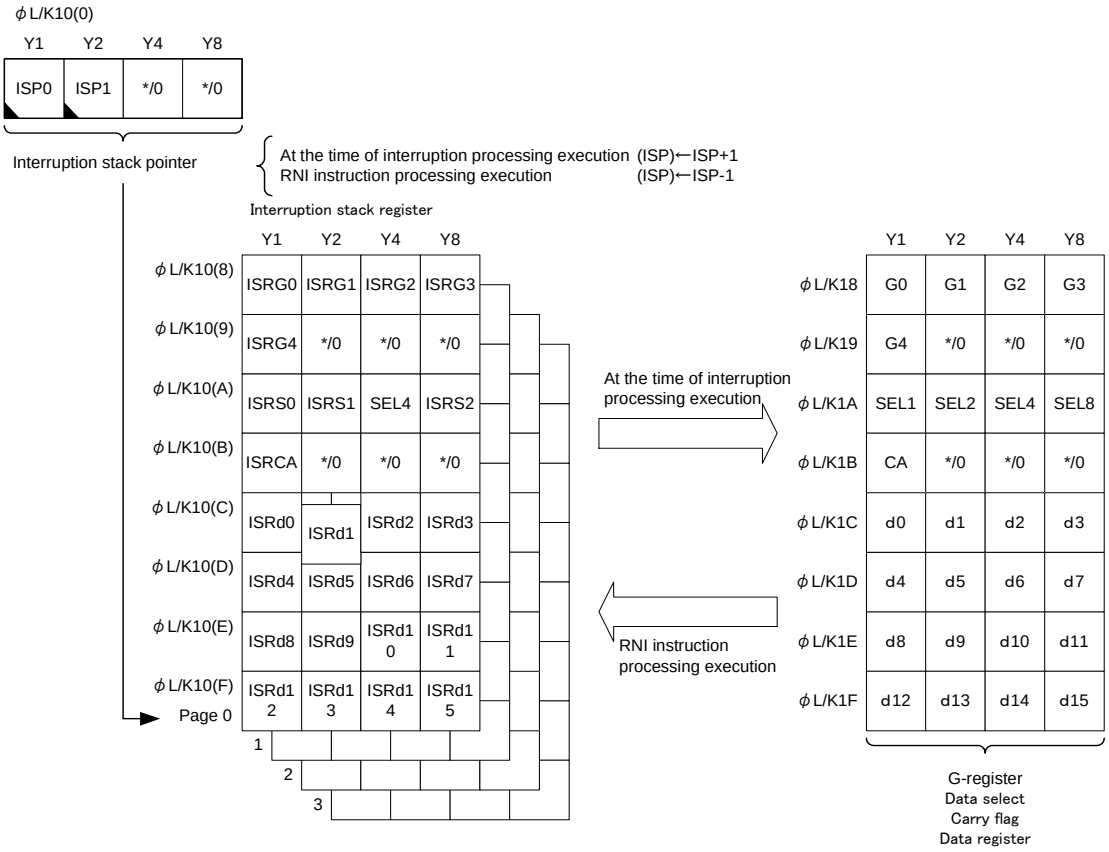
Note: The program memory area is 8k steps and 13 bits are used. Therefore, set the most significant bit (ASR13) to "0".

2. Interruption stack register (ISR)

Interruption stack register (ISR) is a register on 14 bits × page 16. When the interruption processing is executed, the content of 26 bits of G-register, the data selection, the carry flag, and the data register is automatically stored. This register consists of 4 pages and is specified by 2 bits of an interruption stack pointer (ISP). When interrupt is generated, the content of the register in 26 bits like G-register etc. is transmitted to the interrupt register. Simultaneously, an interruption stack pointer is done -1. When the RNI instruction is executed after the interrupt processing ends, the content of the register in 26 bits like G-register etc. is done, and it returns, and +1 is done as for the interrupt stack pointer. Thus, interrupt stack register (ISR) is used as a save register of interrupt.

Interrupt Stack register is page 4 and interrupt stack level becomes four levels.

The interruption stack register and the interruption stack pointer are arranged on the I/O map, and reference/rewriting is possible for them in these contents.

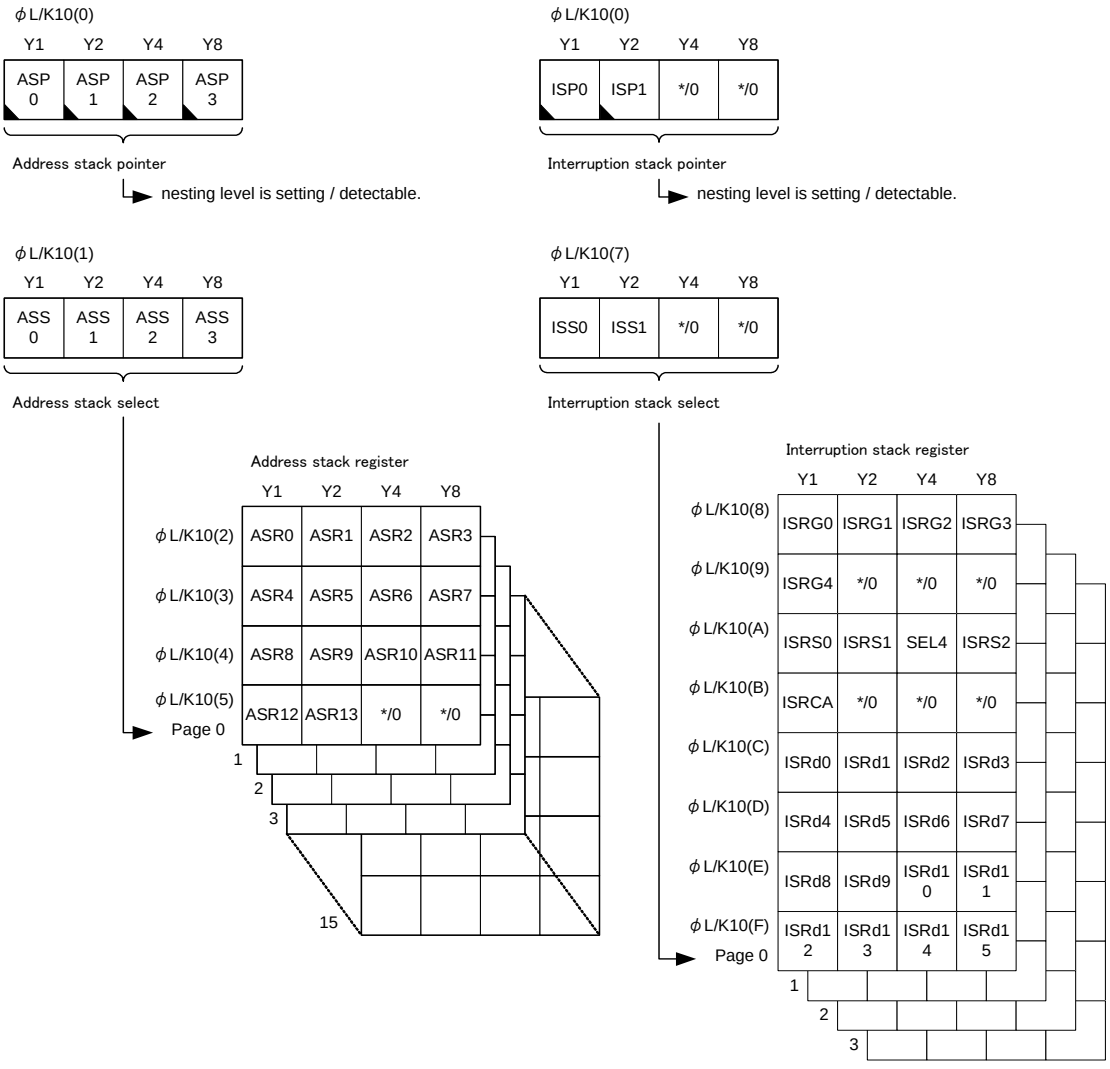


3. I/O Access of a Stack Register

The stack register is arranged in the I/O map. For this reason, reading of the state of a stack register and rewriting of data are possible. The contents of an address stack pointer (ASP) or an interruption stack pointer (ISP) can also be accessed. It is accessed by OUT1/IN1 instruction that specifies [CN = 0H] for the operand part, and these data is divided by the data selection and arranged.

There are an address stack register and each four and 16 page interrupt stack registers. When these ports are accessed by the I/O instruction, it accesses the stack register the specification of the page beforehand. The address stack selection specifies the page of the address stack register. The interrupt stack selection specifies the page of the interrupt stack register.

Rewriting of an address stack register is set up from a low rank bit, it is accessing a higher rank bit and 14 bits of address stack registers are updated. Therefore, it is necessary to note it to have to access higher rank bit when only the lower rank position bit changes.



Note: The program memory area is 8k steps and 13 bits are used. Therefore, it is necessary to set most significant bit (ASR13) of the address stack to "0".

○ Interruption Function

The circumference hardware which can use an interruption function has an INTR1 terminal, INTR2 terminal, timer port, serial interface, and timer counter and decrease voltage detection.

Such circumference hardware will publish an interruption demand signal if certain conditions are fulfilled. If interruption is received, the data of G-register, a data selection, a carry flag, and a data register will shunt to an interruption stack register, and a return address will shunt to an address stack register. Then, it branches to the vector address decided by each interruption factor, and each interruption processing routine is started.

It needs a pretreatment and post-processing of an interruption routine for returning to the same state as the time of interruption. G-register, data select, carry flag, data register return automatically from the interrupt stack register when return (RNI) instruction for shelter and interrupt to the interrupt stack register of interrupt is executed. The register used with other ALU and the data memory that cannot be destroyed should do shelter and the return to the data memory for interrupt by the program.

Interruption priority can be set by the program. During interruption processing, interruption processing of the priority below the interruption is forbidden.

The data of the interrupt stack register and the address stack register returns by executing return (RNI) instruction for interrupt, and the interrupt processing ends.

1. Interruption Control Circuit

Interrupt control circuit consists of interrupt permission flag, interrupt latch and interrupt priority circuit block. These controls are set and controlled by the OUT2/IN2 instruction.

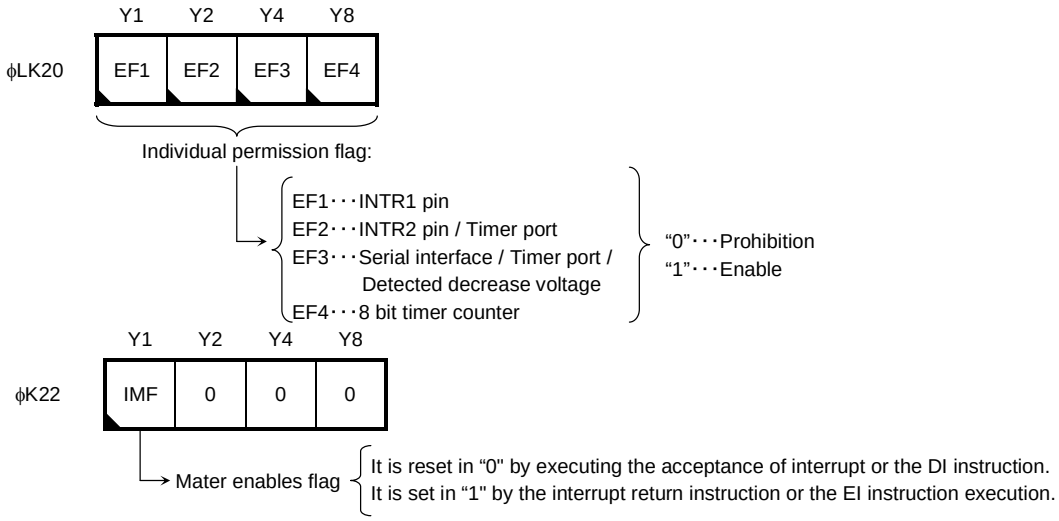
(1) Interruption enable flag

The interruption permission flag has an individual permission flag corresponding to four interruption factors, and the master permission flag which sets up permission and prohibition of the whole interruption processing. The individual permission flag sets the prohibition and the permission of interrupt corresponding to each interrupt factor. If these enable register is set “1”, it becomes enable and is set “0”, it becomes will be set prohibition.

An individual enable flag is accessed with OUT2 / IN2 instructions for which [CN=0H] has been specified to the operand.

The interrupt master permission flag sets the interrupt permission and the prohibition. By executing EI instruction, master permission flag is set to "1" and interruption changes into a permission state. By executing DI instruction, master permission flag is reset to "0" and interruption changes into a prohibition state. If the interruption demand permitted with the individual permission flag is published in the state of interruption permission, CPU will receive interruption, will branch to each vector address, and will perform an interruption routine. In receptionist processing and return processing of interruption, a master permission flag will be in a maintenance state. Therefore, when all interrupt is prohibited in interrupt, the DI instruction is executed and interrupt is prohibited.

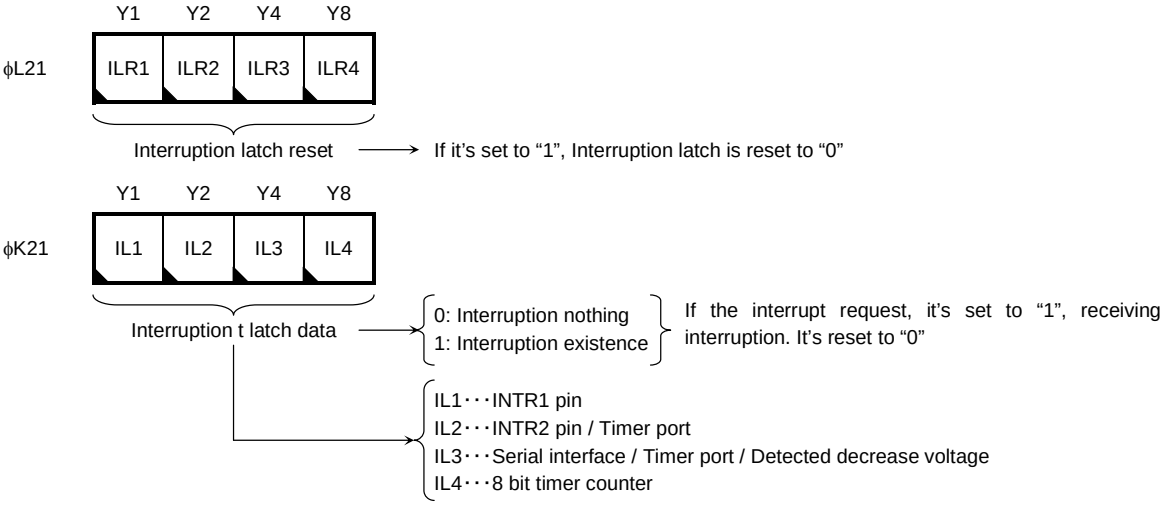
Interruption master flag can be read into a data memory by the IN2 instruction which specified [CN=2H] to be an operand part.



Note: Do not change the setting of the individual permission flag while processing interrupt.

(2) Interruption latch

The interrupt latch is set in "1" by the interrupt request issue from periphery hardware. If interruption is enabled, interruption receptionist will be required of CPU and it will branch to interruption routine. If Interrupt is received at this time, Interrupt latch is reset by data "0" automatically. Interrupt latch data can read by the program and judge individual existence or nothing of interrupt generating. By interrupt request, interrupt latch is reset from "1" from setting "0", it is able to cancel interrupt request or initialized.

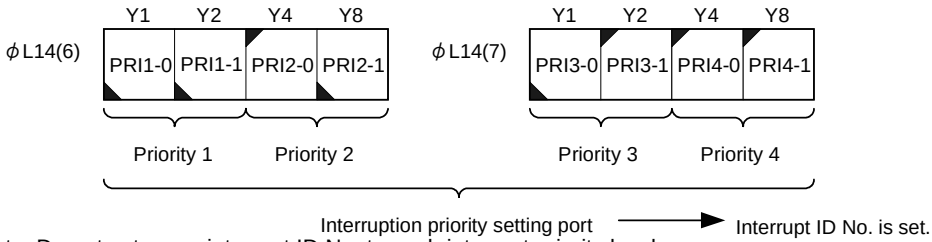


Note: Do not execute interrupt latch reset while processing interrupt.

(3) Interruption priority circuit block

Interruption priority circuit is a circuit of determined the ranking of the Interruption generating when Interruption occurs simultaneously or Interruption permit after two or more Interruptions had occurred. Vector address to Interruption routine is also generated by this block. The interruption priority level can be set by the program. The priority level is decided by setting interrupt ID No. corresponding to each interruption factor to the interrupt priority level setting port. The interrupt priority level setting port is composed of priority level 1 to 4 and sets interrupt ID No. to priority level 1 to 4 in order with high interrupt order. For instance, when the interrupt priority level is set in order of cereal interface (2), INTR1 pin (0), INTR2 pin (1) and timer counter (3), 2h, 0h, 1h, and 3h(ϕL14(6)=2h, ϕL14(7)=dh) are set to priority level 1 ~ 4. It can access by the OUT1 instruction with which these ports specified 6h and 7h to be data selection ports (ϕK/L1A) and specified [CN=4H] to be an operand part, respectively.

Interruption ID No.	Interruption factor	Vector Address
0	INTR1 pin	0001H
1	INTR2 pin / timer port	0002H
2	Serial interface / Timer port / Detected decrease voltage	0003H
3	Timer counter	0004H



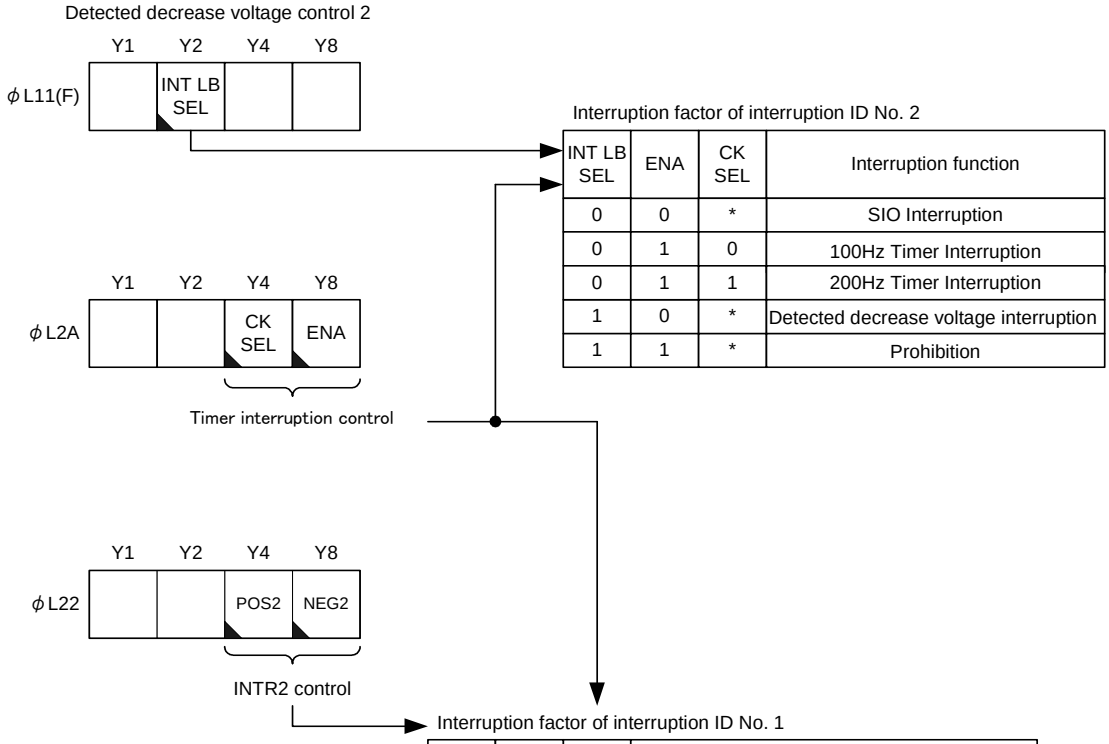
Note: Do not set same interrupt ID No. to each interrupt priority level.

Note: Do not change a setup of an interruption priority during interruption permission and interruption processing.

Note: The interruption priority after system reset serves as the same order as interruption ID No. order (ID No.0 → order 1).

(4) The change of an interruption factor

ID No.1 and 2 can respectively select INTR2 pin / timer port and serial interface / timer port / detected decrease voltage among interrupt ID No.. These changes are done in the control port in each block. It's possible to select by the following setting, and select it according to the specification. When usually initializing it, this setting is done. Do not perform the change under interruption permission and interruption processing. Change excluding these states when changing, and execute reset of the interrupt latch after the Change.



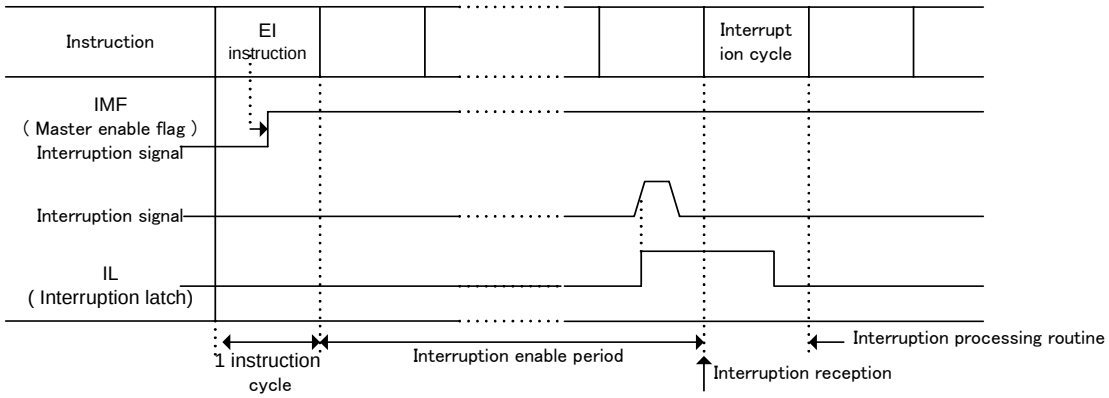
2. Interruption Receptionist Processing

Interruption request is maintenance until if it's receiving interrupt or reset "0" to interruption latch by system reset operation or by the program. Interruption reception operation is as shown below.

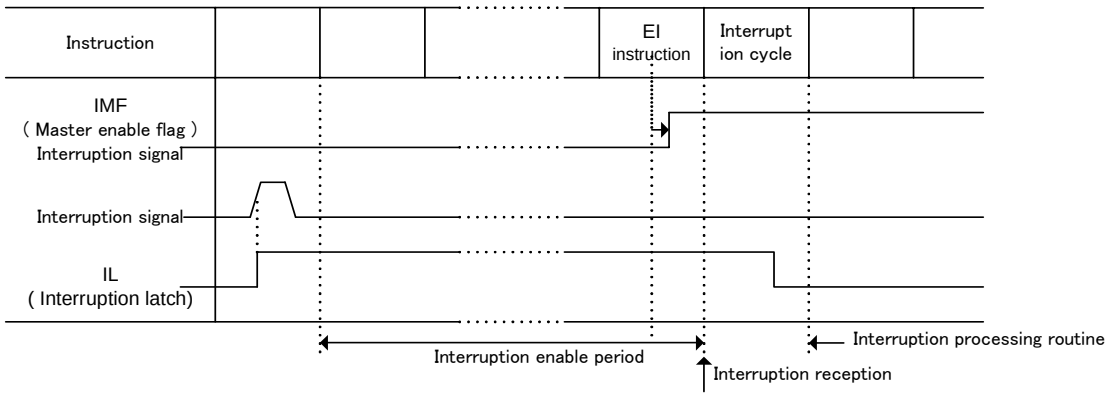
1) Each around hardware is output each interruption signal and set "1" to interruption latch if interruption conditions are fulfilled.
2) Interruption latch of Interrupt factor received resets to "0" if interruption enables flag and the master enable flag corresponding to each Interrupt factor set to "1"
3) The interrupt of the priority level below the accepted interrupt factor is prohibited.
4) The contents of address stack pointer (ASP) and interruption stack pointer (ISP) are done -1.
5) The contents of program counter (PC) are evacuated to address stack register. The contents of carry flag (Ca), G- register (G-REG), data select and data register (DATA) are evacuated to interruption stack register. At this time, the contents of a program become the following address, which permitted the next address or next interrupt at the time of interrupt being received.
6) The contents of vector address corresponding to received interrupt transfers to program counter.
7) Executing of the contents of vector address.

These execution 2) ~ 6) is executed during 1 instruction cycle. The instruction cycle is called "Interrupt cycle"

In case of interruption enable period



In case of interruption reservation period



3. Return Processing from Interrupt Processing Routine

In order to make it return to processing before receiving Interrupt from Interrupt processing routine, RNI instruction and that is an exclusive command is used.

Execution of RNI instruction does the following processing automatically one by one.

1) Interruption of the priority below the returning interruption factor is permitted.
2) The content of the specified interrupt stack register is returned in G-register, data selection, carry flag, and the data register in the interrupt stack pointer and it returns to the program counter respectively by the address stack pointer the content of the specified address stack register.
3) The contents of an address stack pointer (ASP) and an interruption stack pointer (ISP) are carried out +1.

RNI instruction of the above-mentioned processing is processed in 1 instruction cycle.

Note : Return from interrupt by executing the RNI instruction.

4. Interrupt Processing Routine

If interruption has been permitted, CPU accepts the interruption request regardless of the program executed at that time when the interruption request is issued. Therefore, after doing interrupt processing, when making it return to the program of a basis, it is necessary to return to the state where it is performed by interrupt processing. For this reason, it is necessary to perform shunting and return operation within an interruption processing routine about a register, a data memory, etc. which may be operated within an interruption processing routine at least.

(1) Evacuation processing

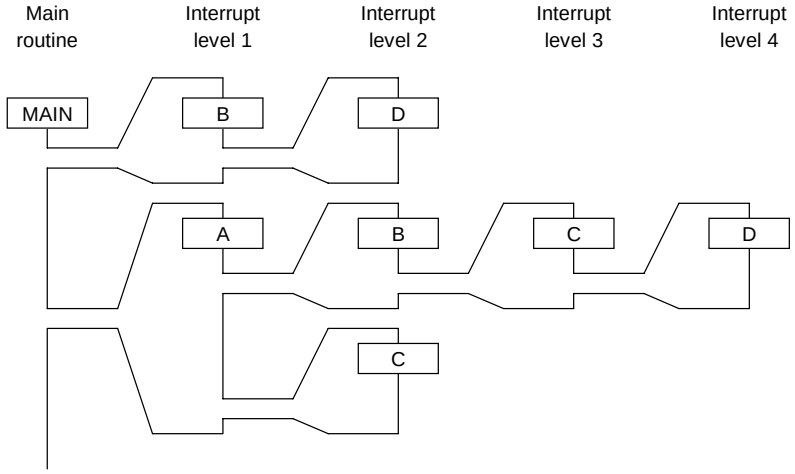
When CPU accepts interruption, it automatically takes evacuation to the interruption stack register the content of G-register, data select, carry flag and data register. The content of the area of the data memory and the General register used by the interrupt processing routine takes evacuation before it uses it by the program if necessary.

(2) Return processing

The content of G-register, data selection, carry flag, and data register returns automatically when RNI instruction is executed. And the return processing does operation opposite to the evacuation processing of the above-mentioned.

5. Multiplex Interrupt

Multiplex Interrupt is the method of processing another interrupt during interrupt processing. As shown in a figure, another interrupt factor C or D is processed during interrupt processing to a certain interrupt factor A and B. The depth of interrupt at this time is called interrupt level.



The example of multiplex interrupt

Cautions are required for the following points when using multiplex interrupt.

1) The priority of interrupt factor
2) Restriction of the Address stack level used at the time of interrupt request issue
3) Shunting processing of a carry flag, a data memory, etc.

(1) Priority of interrupt factor

The priority of multiplex Interrupt is A < B < C < D in a figure.

At the time of a priority, interrupt of C must be processed priority even if interrupt of A or B is under processing, and even if interrupt of C is under, priority must be given to Interrupt of D.

For example, there are interruption factors A and B, it assumed that the factor of A requests every 10 ms and the interrupt processing time is 4 ms and the factor of B requests every 2 ms and the interrupt processing time is 1 ms. When there is no priority of A and B, if an interrupt requests of A enters during interrupt processing of B interrupt, processing of A is done and it will stop doing interrupt processing of B. In such a case, it is necessary to program that give the priority of A < B and forbid interrupt of A during interrupt processing of B, and even if interrupt of B is received under processing of interrupt of A.

Such a priority level is set in interrupt priority level port (ϕL14 (6), ϕL14 (7)) explained by the item of the interrupt priority circuit block. When the setting of the interrupt priority level is set in order of factor A<B<C<D, the interrupt of the interrupt order less than it is prohibited while processing interrupt as the interrupt order is high. For example, all interruption is prohibited at the time of interruption of Factor D, and interruption of permission and factor A/B/C is prohibited for interruption of Factor D during interruption processing of Factor C. The change in the interruption order is prohibited while processing interruption. Please prohibit interruption in the program area that wants to be prohibited by using the DI/EI instruction to prohibit the acceptance of a high interruption factor when the interruption processing with low interruption order is being executed.

(2) Restriction of address stack level

As the item of Interrupt reception processing explained, return address is evacuated to an Address stack register and G-register, data select, carry flag and data register are evacuated to the interruption stack register automatically. The interruption stack level is four levels and the Address stack level is 16 levels. Because the content of the interrupt stack register and the address stack register is destroyed when the interrupt stack level and the address stack level are exceeded, it is necessary to use it so as not to exceed this. Since execution of a sub routine call command is also used, especially an address stack register needs to unite and take into consideration the address stack level by interruption and sub routine call.

(3) Evacuation processing

When using multiplex Interruption, it is necessary to secure the evacuation area of evacuation processing separately to each Interruption factor.

○ External Interruption and Timer Counter Function

External interruption has two types of INTR1 pin and INTR2 pin. Interruption request is done by the rising or falling edge of a signal added to these pins. The I/O port function, the break function when backing up, and the INTR2 pin use the $\overline{INH}$ input pin of PLL combined to the interruption input pin.

Timer counter is 8-bits binary counter and has the function of timer and external clock timer. In the pulse width measurement mode, the pulse width input from external interruption pin (INTR1) for is measured. It is possible to use it for the detection of the leader pulse of remote control etc.

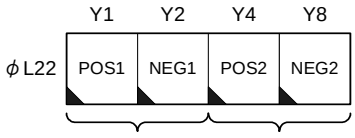
1. External Interruption Function

External interruption has two types of INTR1 pin and INTR2 pin and the edge of these inputs is detected and Interrupt request is done. Schmitt circuit and the noise cancellation are built into input, and the frequency of CPU clock (The low-speed oscillation clock: 75 kHz and high-speed oscillation clocks: 300 to 600 kHz) is used for the noise removal clock. The pulse of less than 1 to 3 clocks of a CPU clock is removed as a noise, and if the above at the time of a 75 kHz oscillation: 13.3 to 40 us pulse for 1 to 3 of a CPU clock (at the time of a 75 kHz oscillation: 13.3 to 40 us) is inputted, it will generate interruption. The rising / falling / both edges can choose input edge for every pin.

The external interruption function serves as a combination pin with I/O port. Interruption will be permitted if edge selection permission is done by the external interruption control port. Moreover, the external interruption input state can be read from the I/O port -4 input data port (ϕK33) used combined.

The INTR1 pin is used combined with the input pin of the pulse width measurement mode function of the timer counter. A logical of pulse setting etc. is controlled with the INTR1 control port. (Refer to section in Timer counter.)

External interruption of the INTR2 pin is a selection with the timer port interruption. When external interruption of the INTR2 pin is used, it is necessary to set the timer port. (Refer to section in timer port, the change of an interruption factor) If Interruption of INTR1 pin is received, the program will branch to 0001H address and a program will branch to 0002H address at the time of INTR2 pin.



INTR1 Control

INTR2 Control

INTR2 external interruption / Control of Timer port interruption

POS2	NEG2	Interruption function	Edge select
0	0	100/200Hz Timer interruption	I/O port function
1	0	External interruption of INTR2 pin	Rising edge
0	1		Falling edge
1	1		Both edge

Control of INTR1 external interruption

POS1	NEG1	Interruption function	Edge select
0	0	External interruption prohibition	I/O port function
1	0	External interruption of INTR1 pin	Rising edge
0	1		Falling edge
1	1		Both edge

Note : The function becomes effective when $\overline{INH}$ input function and break function are permitted at the time of external interruption functional setup.

Note : When interruption is permitted, I/O port -4 control port becomes invalid and becomes input port compulsorily.

2. Timer Counter Function

Timer counter are consists of 8-bit binary counter, counter coincidence register, digital comparator and controlled the control circuit.

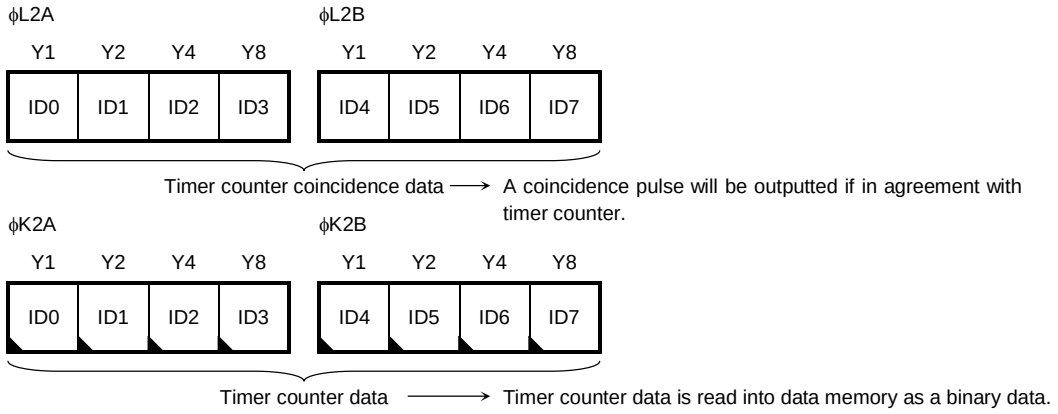
The timer counter function has the timer mode and the pulse width measurement mode.

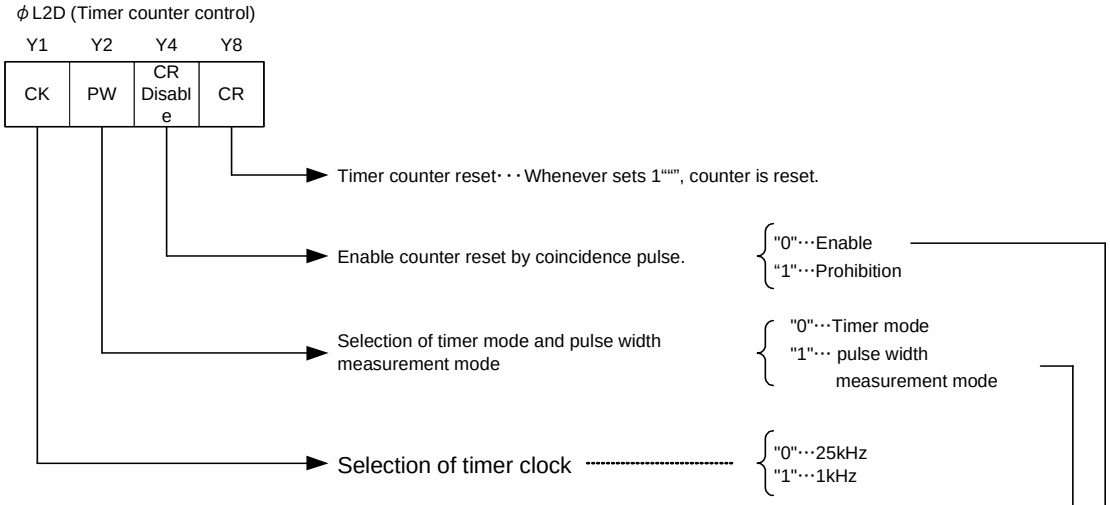
The timer mode is a mode that detects fixed time. The coincidence signal pulse is output and the interruption request is issued when the timer clock is input to the binary counter in eight bits, and it agrees to the content of the counter coincidence register. In pulse width measurement mode, measurement of pulse width and detection of pulse width are performed by carrying out calculation of the timer counter between "H" or "L" levels inputted from INTR1 pin. The pulse width detection can be used to detect the leader pulse of remote control etc.

Timer mode and pulse width measurement mode can use 25 kHz or 1 kHz as a timer clock.

(1) Timer counter register configuration

The register of timer counter is consisted of counter data, coincidence register and control register.





INTR1 control (ϕL22)		Clock enable logic of INTR1 input signal (It's effective only to set CR Disable=0.)	Reset condition of INTR1 input signal (It's effective only to set PW=1.)
POS1	NEG1		
0	0	It does not count.	—
1	0	count among "H" level	Falling edge
0	1	count among "L" level	Rising edge
1	1	Operation always	Both edge

Note : It becomes invalid at each CR Disable=1, PW=0 settings in the above-mentioned.

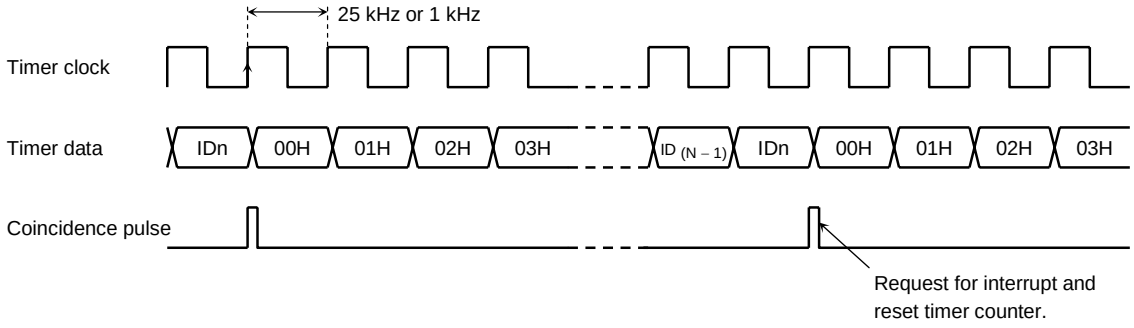
(2) Timer mode

Timer mode is detected fixed time. Interrupt request is done and reset to counter whenever it detects fixed time. At this time, control bit is set to 25 kHz, 1 kHz, "0" to PW bit and "0" to CR bit.

Timer coincidence data is

Timer time = IDn (coincidence data) × Timer clock cycle IDn ≧ 1 (HEX)

It sets up the data which corresponding to time.



(3) Pulse width measurement mode

In pulse width measurement mode, measurement and detection of "H" or "L" pulse width of INTR1 input can be performed.

The control bit at this time selects 1 kHz or 25 kHz as a timer clock, and sets "1" to the PW bit. The INTR1 input becomes the input permission signal of the counter clock if "1" is set to the PW bit, and the timer clock is input to the timer counter in permitting. And coincidence of a coincidence data value and a counter value publishes timer interruption.

The input logic is used combined with the external interrupt logic setting (POS1/NEG1 bit). If "1" and "0" are set as POS1 bit and NEG1 bit, timer counter count on the "H" level. If "0" and "1" are set as POS1 bit and NEG1 bit, timer counter count on the "L" level.

・Detection of pulse width

Detection of pulse width detects more than fixed pulse width. It is possible to use it for detection and the data detection of the leader pulse of remote control etc. The control bit at this time is set as CR Disable bit "0", and timer counter is set as automatic reset at the time of a pulse width measurement end. If it is set as automatic reset, timer interruption will not be published at the time of below the set-up pulse width. Only when the pulse more than detection pulse width is inputted, timer interruption is published and it becomes detectable. It is possible to use it by using external interrupt together as detection of the data of remote control.

The detection pulse width at this time is as follows.

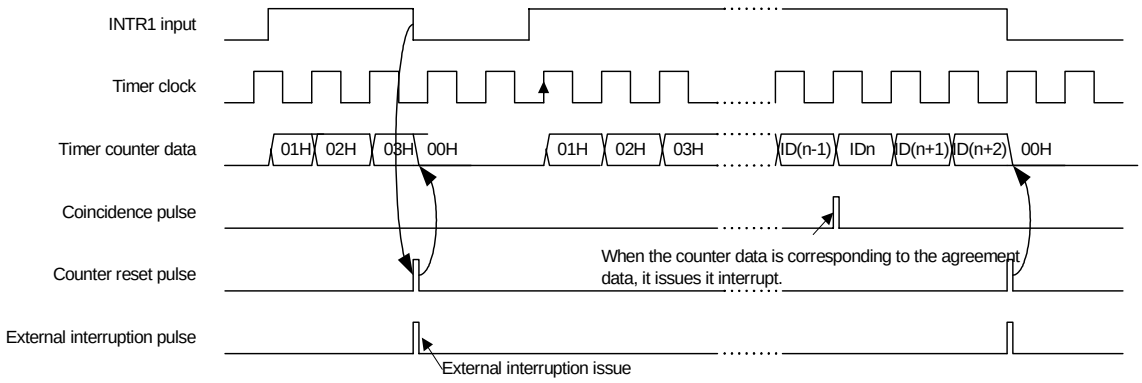
Detection pulse width = IDn(Coincidence data) × The cycle of timer clock IDn≧1(HEX)

・Measurement of pulse width

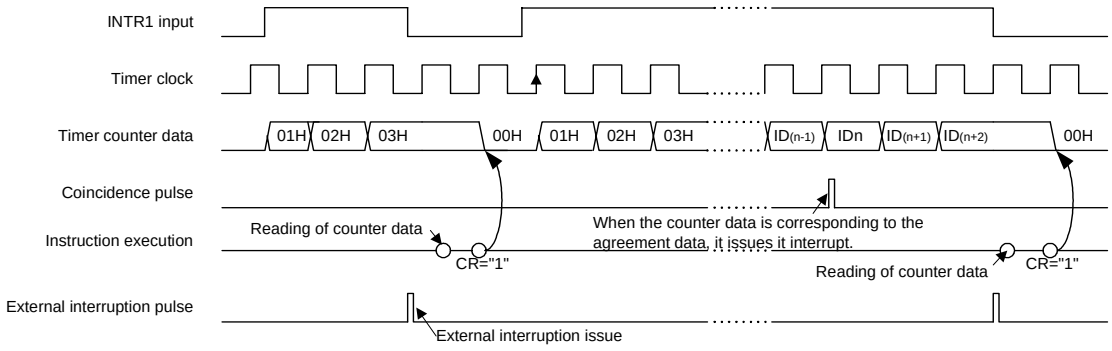
At the time of measurement of pulse width, it sets to the CR Disable bit of a control bit "1", and it sets the reset execution to the timer counter at the time of pulse width measurement end as prohibition state. The pulse width can be measured by referring to the timer counter value detecting the external interrupt issue when the pulse width measurement ends. The pulse width at this time is as follows.

Pulse width = CTn(Timer counter data) × The cycle of timer clock

The timer counter is reset after reading the timer counter data (CR="1") and it initializes it.



The example of pulse width detection operation timing in pulse width measurement mode (CR Disable = “0”)



The example of pulse width detection operation timing in pulse width measurement mode (CR Disable = “1”)

Note : Whenever "1" is set to the CR bit, the counter is reset. Execute reset if necessary.

Note : When external interruption is used together, the measurement end can be detected.

○ Internal Interruption and Interrupt Function

Interruption has four types of timer port, timer counter, serial interface and detected decrease voltage. Among these, timer port, serial interface, and decrease voltage detection is making other interruption factors serve a double purpose. Select and use a necessary interrupt factor.
(Refer to section in the change of an interruption factor.)

1. Interruption of Timer Port

The interruption of the timer port issues interruption by the rising edge of 100Hz or 200Hz timer. Refer to the item of timer port function in detail.

2. Interruption of Timer Counter

If timer counter value is same as coincidence register value, interruption of timer counter is occurred interruption. Refer to the item of timer counter function in detail.

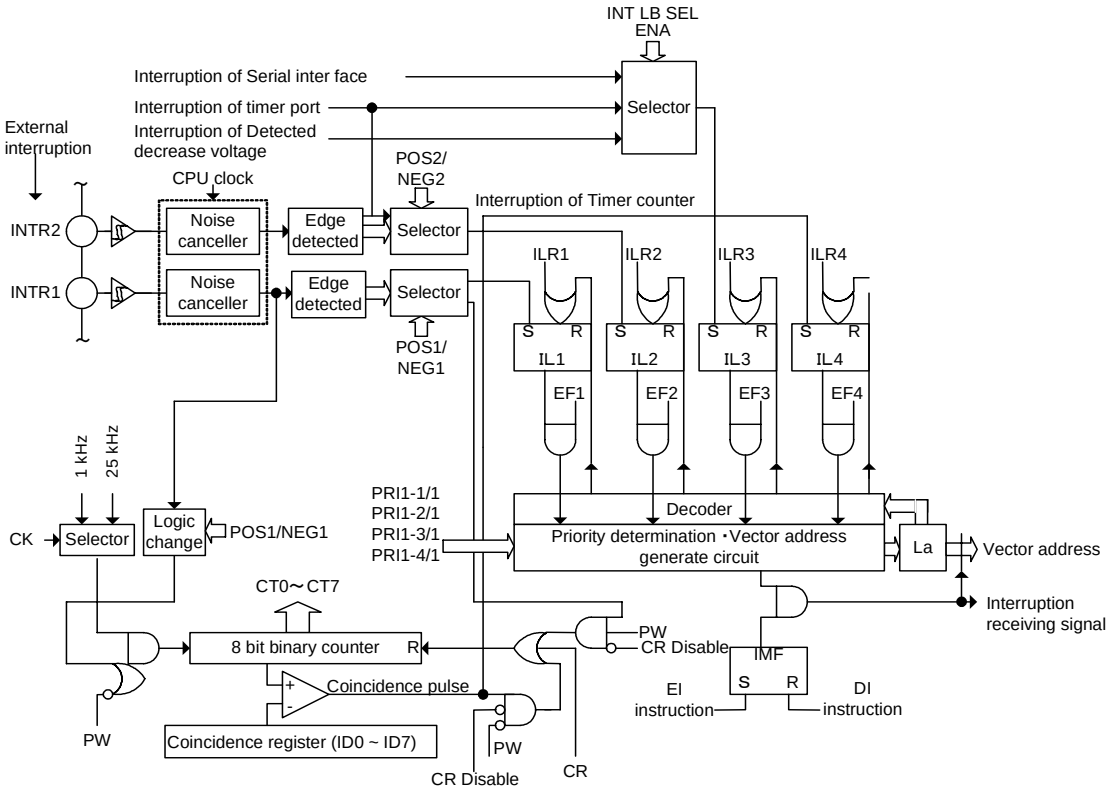
3. Interruption of Serial Interface

Interruption of serial interface is occurred interruption at the time of finishing operation of serial interface. Refer to the item of serial interface function in detail.

4. Interruption of detected decrease voltage

Interruption of detected decrease voltage will publish interruption if decrease voltage is detected. Refer to the item of detected decrease voltage function in detail.

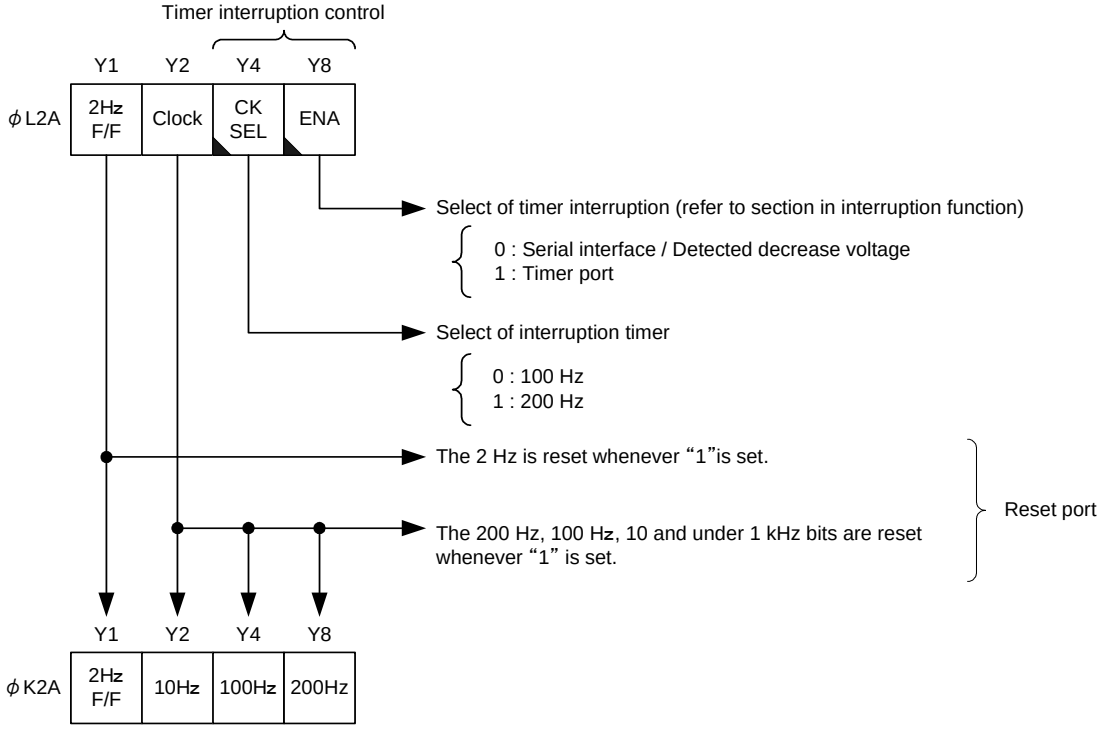
5. Interruption Block Configuration



○ Timer port

The timer us equipped with 100 Hz, 10 Hz and 2 Hz F/F bits and used for counting clock operations and tuning scan mode, etc. Interruption can be issued to interrupt by rising about 100Hz or 200Hz when selecting it in the timer port.

1. Timer port

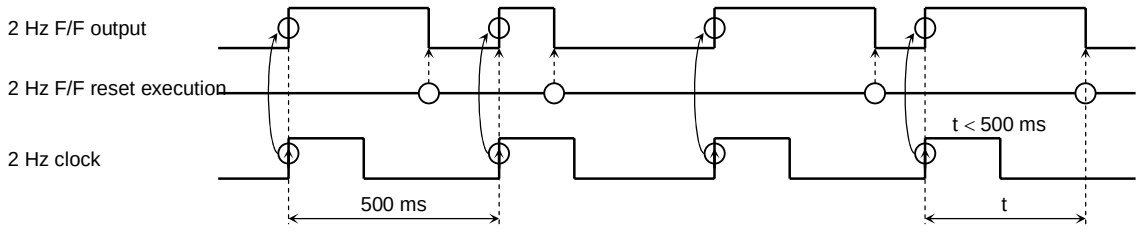


The timer ports are accessed with the OUT2 instruction for which [CN = AH] has been specified in the operand.

2. Timer port timing

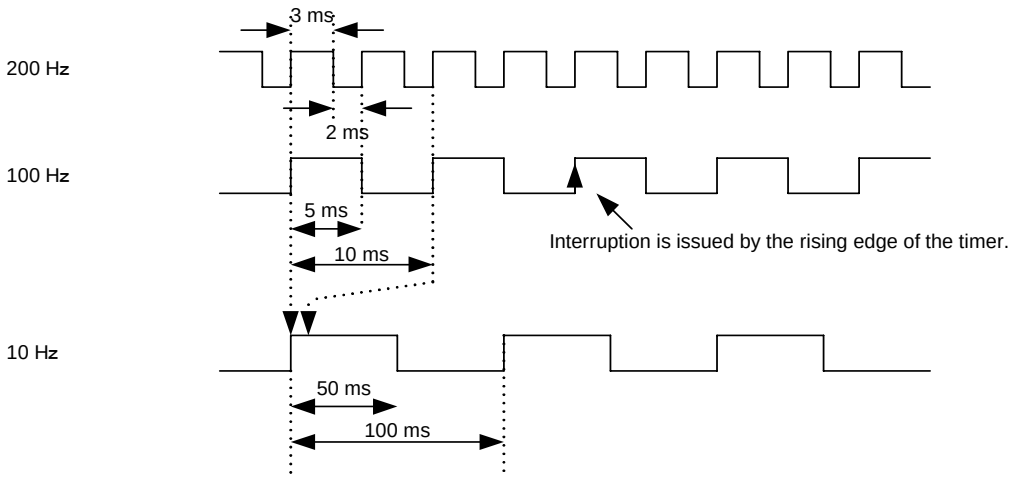
The 2 Hz timer F/F is set with the 2 Hz (500 ms) signal and is reset by setting "1" in the reset port's 2 Hz F/F. This bit is usually used as a clock counter.

The 2 Hz timer F/F can only by reset with the reset port's 2 Hz F/F, and incorrect counts will be output and correct timers not acquired if not reset within a 500 ms cycle.



The 10 Hz, 100 Hz and 200 Hz timers are output to 10 Hz, 100 Hz and 200 Hz bits will respective cycles of 100 ms, 10 ms and 5 ms and a pulse of duty 50%. The duty of 10Hz and 100Hz timer is outputted with 50% of cycle. 200Hz timer is outputted with 60% of cycle of the high level for 3ms, and the low level for 2ms. Counters at 1 kHz or below will be reset whenever the reset port's timer bit is set at "1".

100Hz or 200Hz timer can be selected as interruption. When timer interruption is permitted, interruption is published in rising of this pulse. If interruption is received, a program will branch to 0003H Address.



○ Input and Output Port

There are 45(max.) I/O ports available which are used to input and output control signals. Of these 45 I/O ports, 36 I/O ports are CMOS type and 9 I/O ports are Nch open drain type. The exclusive input port has maximum of two and maximum of two exclusive output ports.

I/O port 3 can set the pull-down or the pull-up. I/O port 3, 4, 6, and 8 can do the backup release (Break function) setting by the port pin and each I/O port becomes the terminal of using combined of peripherals. Please switch according to the specification and use it.

1. I/O port, Exclusive Input Port (IN/IN2), Exclusive Output Port (OT1 / OT2)

The combination function and the functional feature of each I/O port are as follows.

I/O port		Pin Number	Combination and Additional Function		Input impression tolerance	Structure	Break Function
			Pin name	Funciton			
I/O port 6	P6-0 ~ P6-3	11 ~ 14	ADin1 ~ ADin3	6 bit A/D converter analog input	0~VDB (VDD × 2)	Nch	○
I/O port 10	P10-0 ~ P10-3	15 ~ 18	COM1 ~ COM3	LCD driver common output	0~VLCD (3V)	CMOS	–
I/O port 12	P12-0 ~ P12-3	19 ~ 22	S1 ~ S4	LCD driver segment output			
I/O port 13	P13-0 ~ P13-3	23 ~ 26	S5 ~ S8				
I/O port 14	P14-0 ~ P14-3	27 ~ 30	S9 ~ S12				
I/O port 15	P15-0	31	S13				
	P15-1	32	S14				
I/O port 16	P16-0	33	S15				
	P16-1	34	S16				
	P16-2	35	S17/Xin2	LCD driver segment output / High speed oscilattoer			
	P16-3	36	S18/Xout2				
I/O port 3	P3-0	37	SCK1/RX1	Serial interface (CMOS input and output)			○
	P3-1	38	SDIO1 / TX1				
	P3-2	39	SI1				
	P3-3	40	PCTRin	Pulse counter input			
I/O port 4	P4-0	41	INTR1	External interruption input / PLL inhibit input			
	P4-1	42	INTR2/$\overline{\text{INH}}$				
	P4-2	43	BUZR	Buzzer output			
	P4-3	44	VRout1	Electrical volume			–
I/O port 5	P5-0	45	VRin1				
	P5-1	46	VRcom				
	P5-2	47	VRin2				
	P5-3	48	VRout2				
Exclusive input port	IN	49	IFin	IF input	0~VPLL		
Exclusive output port	OT1	53	DO1/P	Phase comparator output	0~VDB (VDD × 2)		
	OT2	54	DO2/N/Tin				
I/O port 9	P9-0	55	Tout		0~5.5V	Nch	
	P9-1	56	MUTE	Mute output	0~VLCD (3V)	CMOS	
	P9-2	57	DDCK2 / TEST	DC - DC converter clock output for VT / Test input			
I/O port 8	P8-0	58	VDET	DC - DC converter voltage detection input for VT	0~5.5V	Nch	○
	P8-1	59	DDCK1	The DC-DC converter clock output for VT			
			SI2	Serial interface (Nch open drain input and output)			
	P8-2	60	SCK2 / RX2				
	P8-3	61	SDIO2 / TX2				
Exclusive input port	IN2	4	C2	DC - DC converter pin for CPU	0~VDB	–	–

I/O port 3 is I/O port of CMOS structure. The P3-0 to 2 pins are used the serial interface combined and the P3-3 pin is used the pulse counter input pin combined. It can be set to pull-up / downs and the break function. (Refer to section in Serial interface and pulse counter)

I/O port 4 and 5 are I/O port of CMOS structure. The P4-0 and 1 pins are used the external interruption input pin combined, the P4-1 pin is used the Inhibit input pin combined, the P4-2 pin is use the buzzer output pin combined and the P4-3, P5-0 to 3 pins are used the electrical volume pin combined. The P4-0 to 3 pins can set the Break function. (Refer to section in Backup and Buzzer output)

I/O port 6 is I/O port of Nch open drain structure. The impression to the VDB pin level is possible. 6 bit A/D converter analog input is used combined. The Break function can be set.
(Refer to section in A/D converter)

I/O port 8 is I/O port of Nch open drain structure. Impression to 5.5 V is possible. The P8-0 pin is used the DC – DC converter dobuler voltage detection input for VT pin combined, the P8-1 pin is used the DC - DC converter clock output for VT pin combined and P8-1 to 3 pins are used the serial interface combined. These pins can set the Break function. (Refer to section in DC - DC converter and Serial interface)

I/O port 9 is I/O port of Nch open drain structure (P9-0) and CMOS structure (P9-1, P9-2). The P9-0 pin is used Tr. Output for LPF pin combined, the P9-1 pin is used Mute output pin combined, the P9-2 pin is used clock output for DC – DC converter pin combined. The P9-2 pin is pull-down and becomes test mode input pin during “L” level of $\overline{\text{RESET}}$ pin. It is necessary to make this pin into open or the "L" level during the test mode input. (Refer section in MUTE output, DC –DC converter for VT and Phase comparator)

I/O ports 10 to 16 are I/O port of CMOS structure. The LCD driver output pins are combined. P16-2 and 3 pins are used the high-speed oscillation terminal combined.
(Refer to section in LCD driver, System clock control circuit)

There are two exclusive input ports. They are IN input pin of IFin input combination, and IN2 input pin of the pin C2 combination input for doubler. IN input can be changed by the program. The IN2 input is Al option, and when the switching regulator type is selected, the IN2 input can be used for the DC-DC converter for CPU.

Two phase comparator output pins can be used as exclusive output port (OT1/OT2). These pins can output "H" level, "L" level and three values of high impedance. As for the "H" level, V_{DB} pin level is outputted.

The V_{LCD} (3V) power supply pin is used for the power supply of I/O Ports 3, 4, 5, 8, 9, 10 to 16 of I/O circuit. Therefore, when outputting it, the impressed voltage becomes possible impression up to 3V, and can obtain depend for the terminal V_{DD} power supply a small, steady output current. Moreover, the IN2 pin is possible the impression to the V_{DB} pin level. As for the IN pin, the impression to the V_{PLL} pin level is possible.

Note : Refer to each item of the function of using combinedly for the setting of each pin to the I/O port.

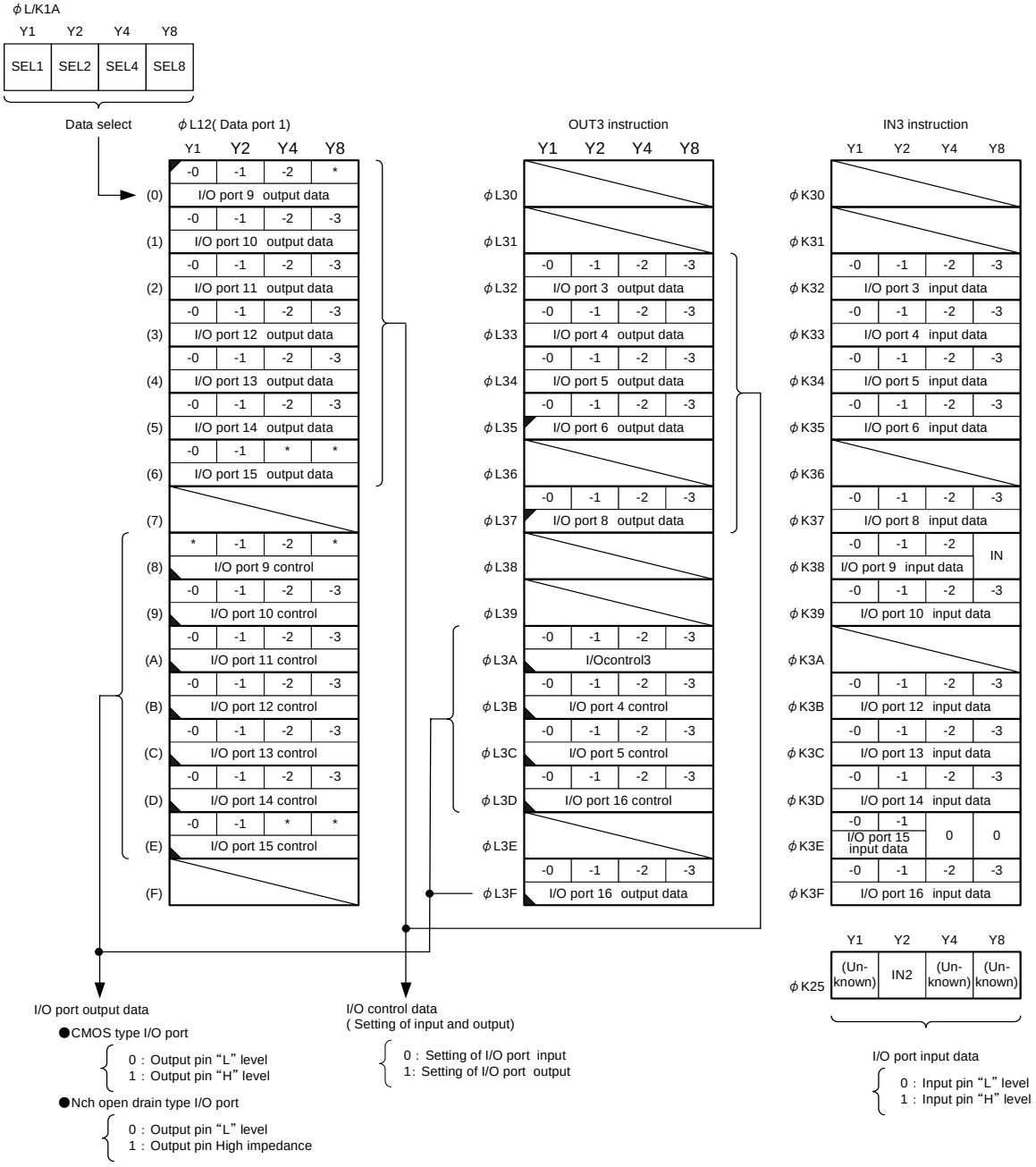
Note : As for "H" level of the OT1/OT2 output, the V_{DB} level is output. As for the I/O port of other CMOS forms, all the V_{DD} levels are output.

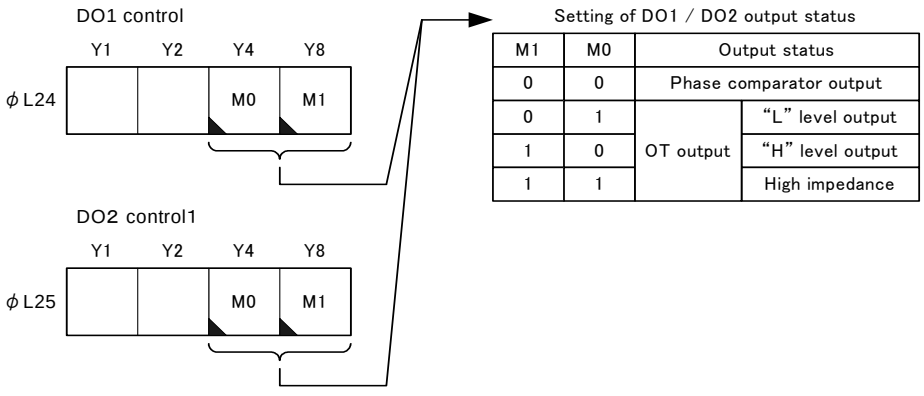
Note : The power supply of the exclusive input port IN is using the V_{PLL} power supply. For this reason, "H" and the "L" level are more than V_{PLL}x0.8 and less than V_{PLL}x0.2, respectively, and if they turn off a V_{PLL} power supply at the time of tuner-off, IN input become unfixed. All the input levels except this pin are "H" levels: V_{DD}×0.8 or more "L" level: It becomes V_{DD}×0.2 or less.

Note : After system reset, the MUTE / P9-1 pin is set in the MUTE output and all other I/O pins are set to an input or high impedance of the I/O port. The MUTE output becomes "L" level while resetting the system. After system reset is released, it becomes "H" level.

Note : All pins set to the output of the I/O port is outputted "L" level while executing the clock stop instruction. The former state is outputted after clock stop release.

2. Control Port of Input and Output Port





The setting of input and output of I/O port is set with I/O control data port. ”0” is set in the I/O control data port bit which corresponds to the relevant port when setting the input port, and “1 is set when setting the output port.

The output port is output by setting the I/O port output data port. ”1” is set in the output data port bit which corresponds to the relevant port when setting the “H” level, and “0 is set when setting the “L” level.

I/O control data and I/O Port output data perform setup and control by data port - 3 of OUT1 instruction, and OUT3 instruction. The state of the pin is read to the data memory by executing the IN3 instruction. The output latch is not influenced to the content by executing the IN3 instruction.

The OT1 / OT2 output is set by the content of the DO control port. (Refer to section in Phase Comparator)

Note : The I/O control port (I/O port 6,8,9-0) of the Nch open drain form doesn't exist. Set "1" to output data when setting it to the input and make it to high impedance.

Note : I/O port 1, I/O port 2 …correspond to P1-0 to 3, P2-0 to 3 … of the pin name.

Note : After system reset, the contents of output port becomes unknown. Therefore, we will recommend output data to be fixed before the output is set.

Note : When ϕL1 to ϕL15, ϕK10 and ϕK11 of the I/O map is accessed, the data select port is automatically done by +1 increment.

Note : When setting it to the output, the state of the pin is re A/D by executing the IN3 instruction.

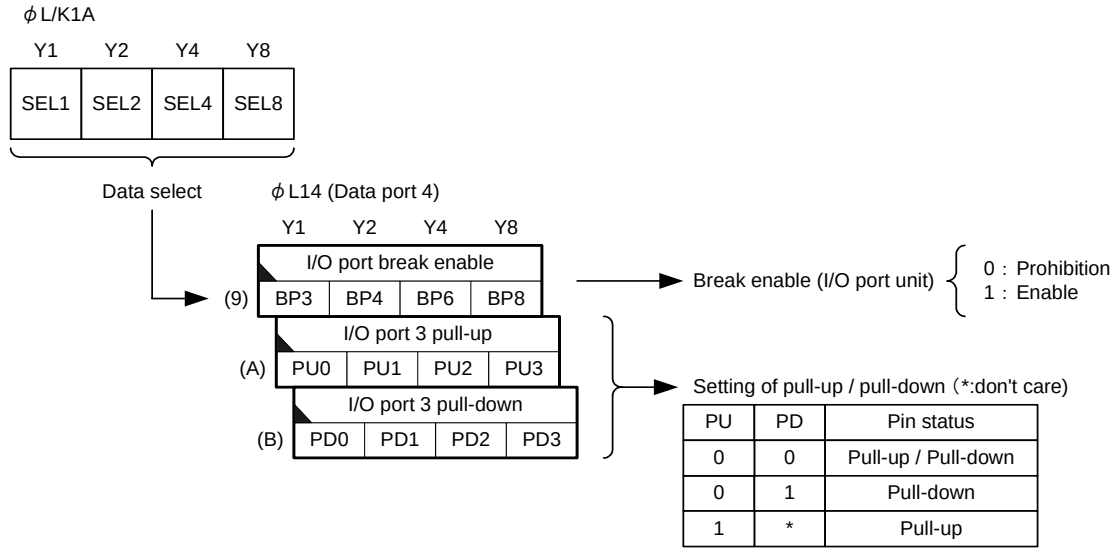
Note : All the input circuits are the AND structures, the gate of AND is turned on only at the time of reading (IN instruction) execution of data. An input has almost no influence of consumption current also with a floating state or middle potential. Therefore, a pull-up in potential that is lower than the V_{DD} potential and 3 value output at the output level can be used. However, it is necessary to note it so that current consumption may increase rapidly when it sets to the break pin, serial interface setup, the interruption input, etc. and the input is middle potential,

Note : Y1/Y4/Y8 bits other than IN2 bit of the exclusive input port (ϕK25) become unfixed.

3. Break Setting, Pull-Up / Pull-Down Setting

16 of I/O Ports 3, 4, 6, and 8 can be set as a back up release pin (Break pin) for every I/O Port. The break pin releases the execution of WAIT and CKSTP instruction when the input of the I/O port set to the input changes, and reactivates CPU operation. When the Break bit of the MUTE port is "1", the MUTE bit is compulsorily set in "1" by change of an input state. (Refer to section in MUTE output)

I/O port 3 can be set by pull-up/down control port with 50kΩ (standard) in the pull-down or the state of the pull-up every one pin. Set it to pull-up/down control port corresponding to the I/O port 3.



PU	PD	Pin status
0	0	Pull-up / Pull-down
0	1	Pull-down
1	*	Pull-up

Note : BP3, BP4, BP6, and BP8 correspond to I/O Port 3, 4, 6, and 8, respectively.PU0/PD0, PU1/PD1, PU2/PD2 and PU3/PD3 correspond to P3-0, P3-1, P3-2, and P3-3 pin, respectively.

Note : Break enable is carried out only when it is made an input setup of an I/O Port. Do not do the use that becomes the middle level to the input pin where the break setting.

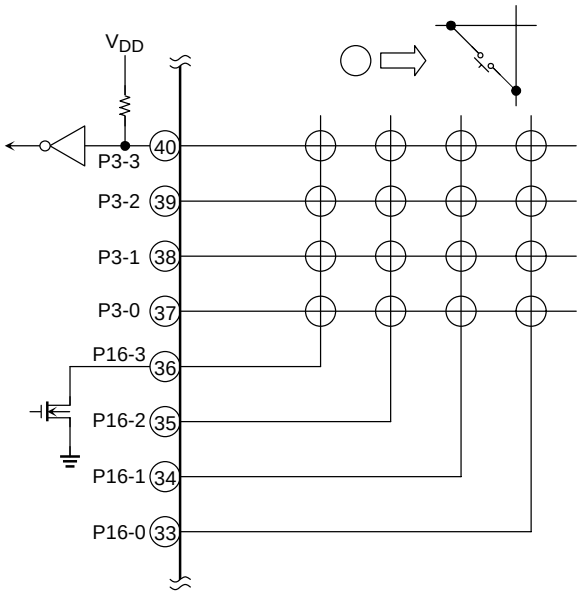
Note : It is necessary to read the input of the released I/O port before the wait instruction or clock stop instruction is executed.

Note : If serial interface function, plse counter function or break permission of the interruption input is carried out at the time of use, wait instruction and clock stop instruction are released by input change of these pins. However, it is necessary to read the input of the I/O port according to the I/O port control before the instruction is executed of the input setting doing.

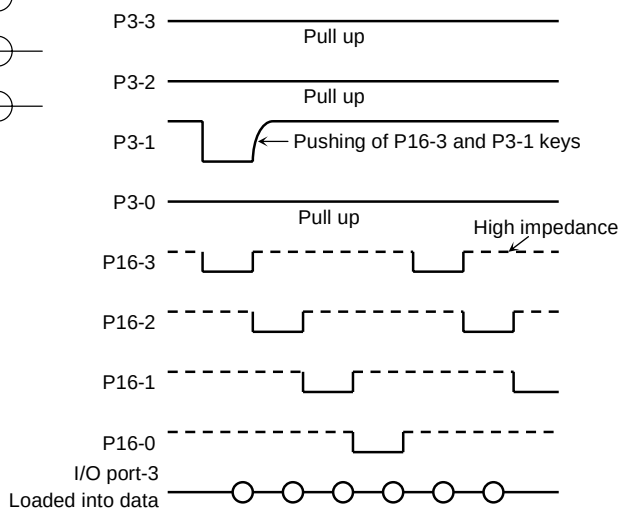
Note : The pull-up / pull down setup of I/O Port 3 can be set at the time of serial interface function and pulse counter function use.

Set up the pull-up and pull-down is used for key matrix configuration. I/O Port -3 with a pull down or a pull-up is considered for a usual I/O Port output as an input as an output of key matrix and key matrix is constituted. During executing of CKSTP instruction and WAIT instruction, the existence of this key input can also be judged and re-started when the key input is set in the break.

The following is an example of key input matrix circuit configuration.



Example for key input matrix circuit

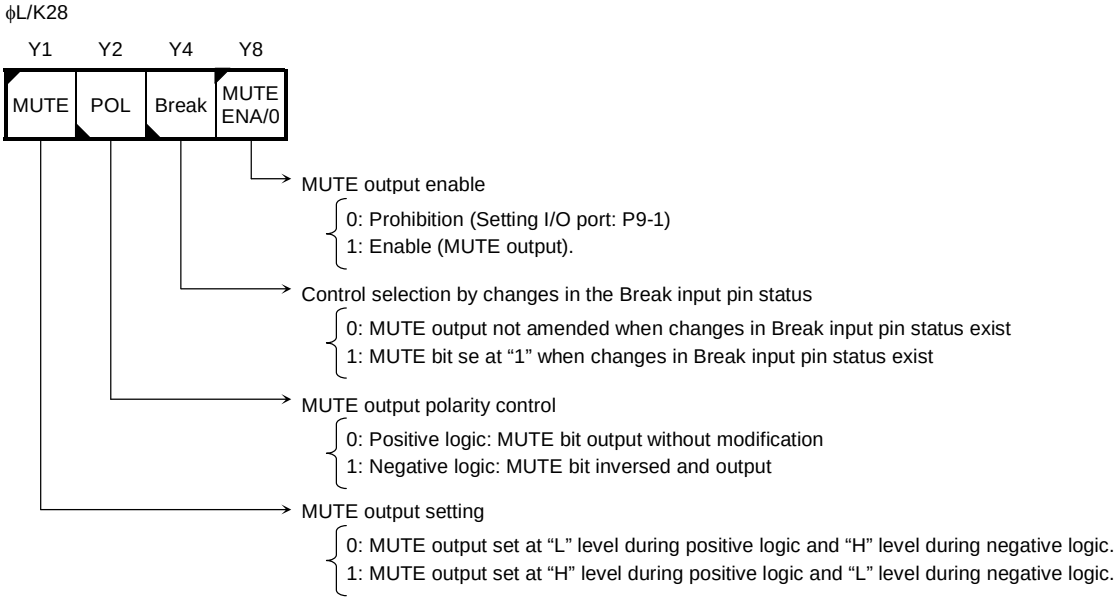


Note : When the CKSTP instruction is released by the key input, since the standby time of about 100 ms occurs as time lag after being canceled of a clock stop.

○ MUTE output

This is a dedicated 1-bit CMOS output port fro muting control purposes. It uses it combined with P9-1 of the I/O port. The MUTE output can reverse the MUTE output by outputting logical set and changing of the I/O port.

1. MUTE port



The MUTE output is usually used for the Muting control.

The MUTE output uses combined with I/O port function pin (P9-1) and switches the I/O port and the MUTE output pin by the MUTE ENA bit. After reset, this bit is set in "1" and becomes MUTE output.

MUTE bit outputs the data set as this bit to a MUTE output pin in right logic or negative logic. If the break function of the I/O port is permitted (Refer to section in the I/O port item) and "1" is set to the Break bit,, whenever the input of the I/O port changes, the MUTE bit can be set in "1". It can change into muting state quickly at the time of the band change or radio-off etc., and the pop sound generated in a linear circuit can be prevented. IPOL bit sets up the logic of MUTE output. Set up according to specification.

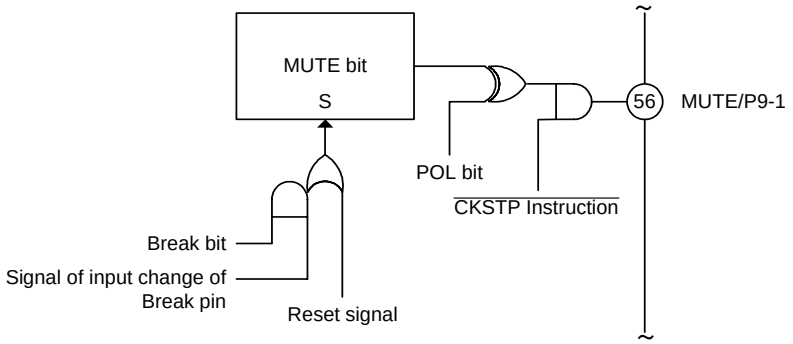
This port is accessed with the OUT2/IN2 instruction for which [CN = 8H] has been specified in the operand.

Note : As for a MUTE output, the "L" level is outputted during system reset. After reset is released, "H" level is output. It becomes "L" level while executing the clock stop instruction, and after it releases it, the state before is output.

Note : When MUTE by the break function is controlled, the MUTE bit is set in "1" with the break pin. The state of the MUTE bit can be referred to by MUTE bit (ϕK28). The state of a MUTE pin can be referred to in the I/O Port 9 input data port (ϕK38) of P9-1.

Note : When a MUTE bit sets it as "1", electronic volume can be set as -∞dB. (Refer to section in electronic volume)

2. Circuit Composition of MUTE Output



○ Serial Interface

Serial interfaces are two channels and one serial interface. There are three kinds of functions of the UART function of 3 line type, 2 line type serial interface, and the full duplex are provided.

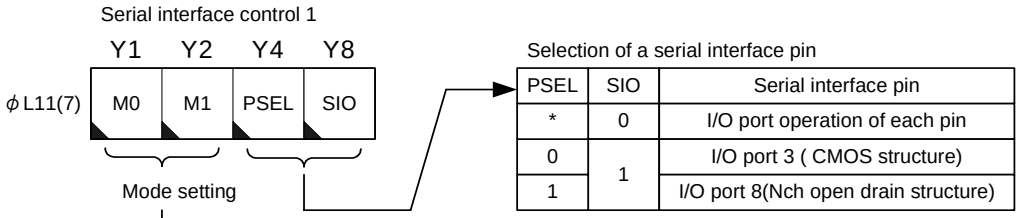
SCK1/TX1(P3-0), SDIO1(P3-1),SI1(P3-2) pins of the serial interface of CMOS form or SCK2/TX2(P8-2), SDIO2(P8-3),SI2(P8-1) pins of Nch open drain type (it approves to impression voltage 5.5V) perform transmission and reception with LSI or microcomputer for extension. When the operation of the serial interface ends, interrupt is issued.

The serial interface consists of control circuits which control 4 bits input-and-output serial counter, 12 bits serious output latch, a 12-bit serial input latch, and these.

The basic operation of a serial interface is as follows. In serial output operation, the serial data output bit data specified at the serial output counter is outputted, and data is outputted to a serial output pin at the order specified when a serial counter was risen or downed with a serial clock. In serial input, the serial input data is sequentially taken into the serial latch specified with the serial input counter like a serial output.

1. The Serial Interface's Control Port, Data port

The serial interface performs control and data transfer by the control port and the data port. These ports are arranged in data port 2 of the I/O map, and accessed by the OUT1/IN1 instruction.



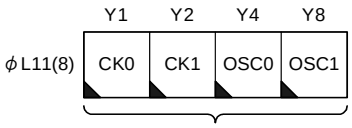
Selection of a serial interface pin

PSEL	SIO	Serial interface pin
*	0	I/O port operation of each pin
0	1	I/O port 3 (CMOS structure)
1		I/O port 8(Nch open drain structure)

Serial interface mode setting

M1	M0	Serial interface mode
0	0	Operation stop
0	1	2 line type interface
1	0	3 line type interface
1	1	UART

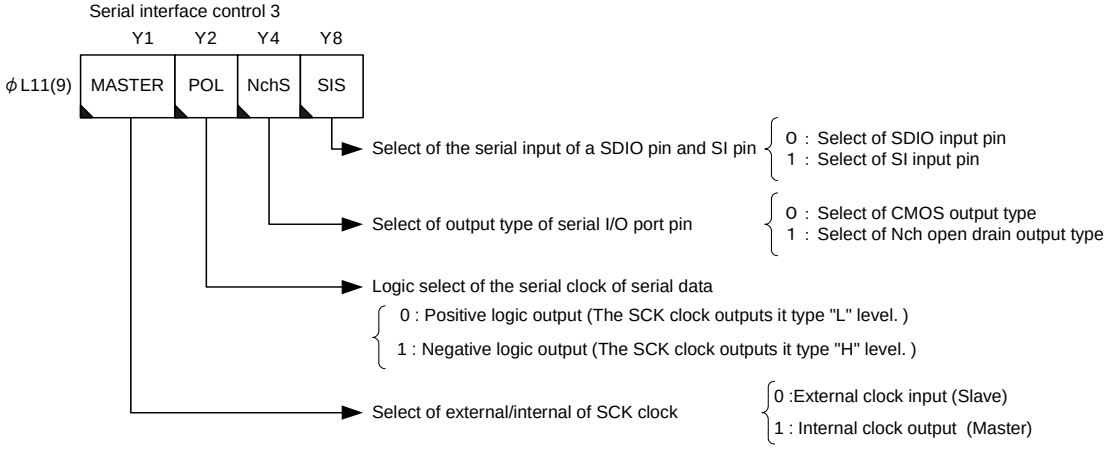
Serial interface control 2



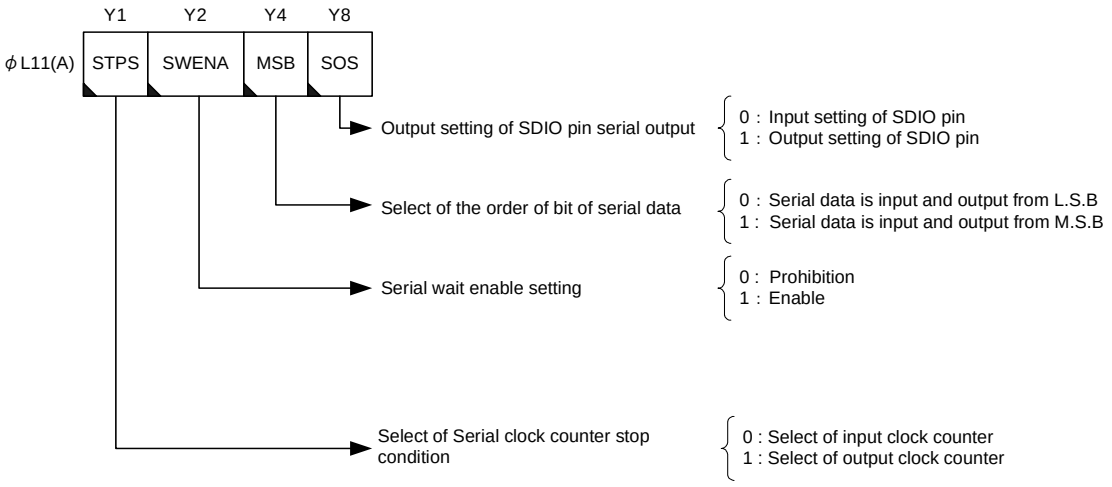
Serial clock (transmission rate) frequency setting

OSC1	OSC0	Setting of oscillator	CK1	CK0	At 2/3 line setting of type Clock frequency (fSCK)		UART transceiver transmission rate (fSCK)		
0	0	Low-speed oscillator (75 kHz)	0	0	fosc/2	37.5kHz	-		
			0	1	fosc/4	18.75kHz	fosc/8bps	9375bps	9600bps mode
			1	0	fosc/8	9.375kHz	fosc/32bps	2344bps	2400bps mode
			1	1	fosc/16	4.6875kHz	fosc/64bps	1172bps	1200bps mode
0	1	High-speed oscillator (300 kHz)	0	0	fosc/2	150kHz	fosc/16bps	18750bps	19200bps mode
			0	1	fosc/4	75kHz	fosc/32bps	9375bps	9600bps mode
			1	0	fosc/8	37.5kHz	fosc/128bps	2344bps	2400bps mode
			1	1	fosc/16	18.75kHz	fosc/256bps	1172bps	1200bps mode
1	0	High-speed oscillator (450 kHz)	0	0	fosc/2	225kHz	fosc/24bps	18750bps	19200bps mode
			0	1	fosc/4	112.5kHz	fosc/48bps	9375bps	9600bps mode
			1	0	fosc/8	56.25kHz	fosc/192bps	2344bps	2400bps mode
			1	1	fosc/16	28.125kHz	fosc/384bps	1172bps	1200bps mode
1	1	High-speed oscillator (600 kHz)	0	0	fosc/2	300kHz	fosc/32bps	18750bps	19200bps mode
			0	1	fosc/4	150kHz	fosc/64bps	9375bps	9600bps mode
			1	0	fosc/8	75kHz	fosc/256bps	2344bps	2400bps mode
			1	1	fosc/16	37.5kHz	fosc/512bps	1172bps	1200bps mode

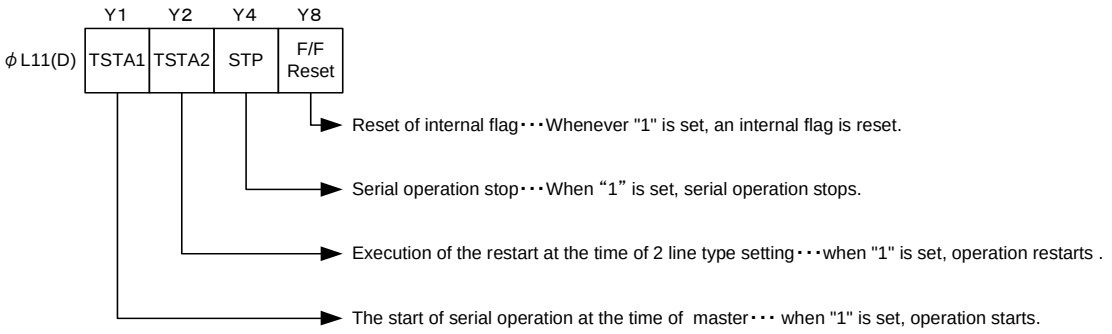
Serial interface control 3

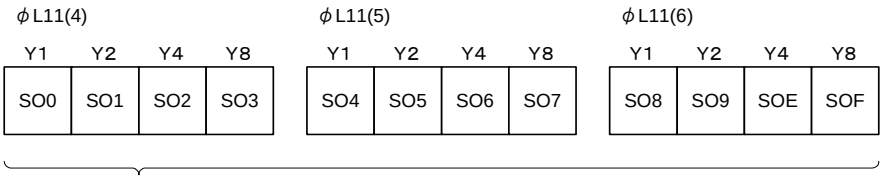


Serial interface control 4



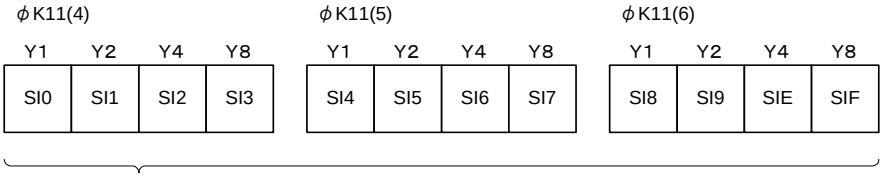
Serial interface control 7





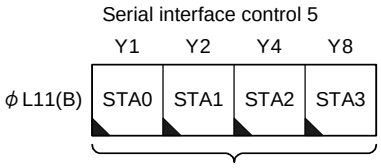
Serial output data → The set data outputs output data corresponding to the output counter number to the serial output pin.

0 : Serial output "L"
1 : Serial output "H"

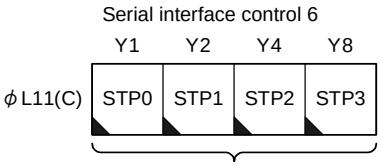


Serial input data → The state of the serial input pin is input to input data corresponding to the input counter number by the edge of the shift clock.

0 : Serial input "L"
1 : Serial input "H"

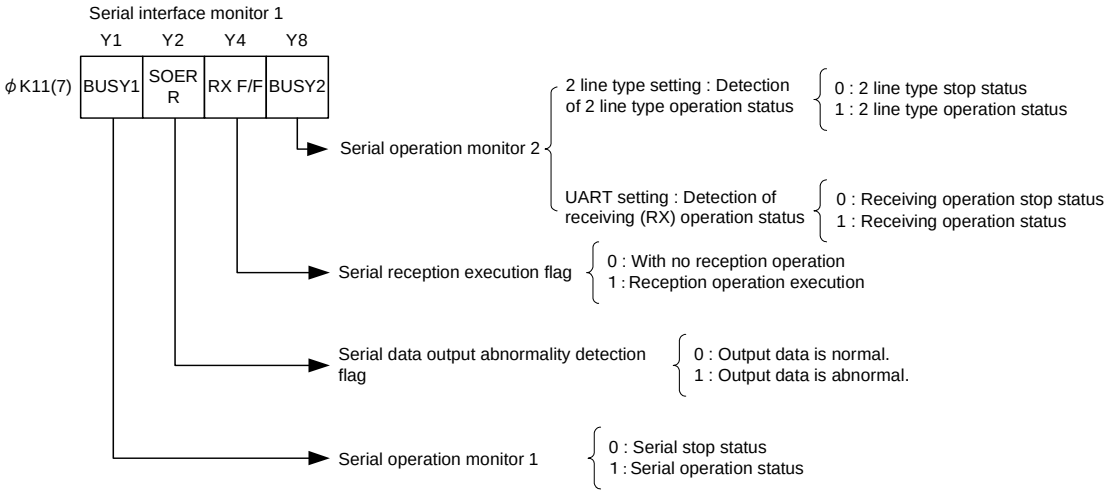


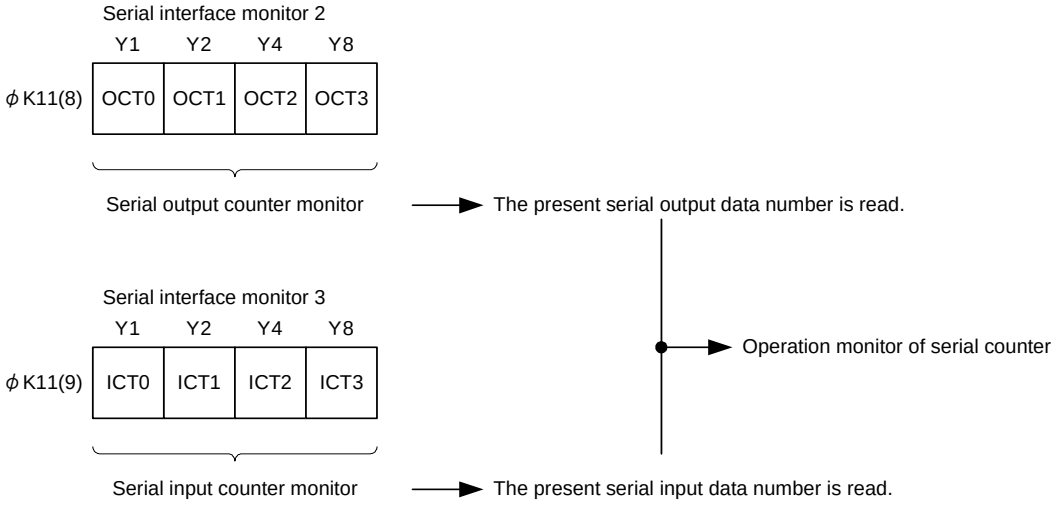
Start data of serial counter → When the serial operation starts, the set counter number is set in the cereal counter.



Setting of start and stop of a serial counter.

Stop data of serial conter → The serial counter stops by the set counter number.


Serial interface monitor 1
Y1 Y2 Y4 Y8
ϕK11(7)
BUSY1
SOER R
RX F/F
BUSY2
Serial operation monitor 2
2 line type setting : Detection of 2 line type operation status
0 : 2 line type stop status
1 : 2 line type operation status
UART setting : Detection of receiving (RX) operation status
0 : Receiving operation stop status
1 : Receiving operation status
Serial reception execution flag
0 : With no reception operation
1 : Reception operation execution
Serial data output abnormality detection flag
0 : Output data is normal.
1 : Output data is abnormal.
Serial operation monitor 1
0 : Serial stop status
1 : Serial operation status


Serial interface monitor 2
Y1 Y2 Y4 Y8
ϕK11(8)
OCT0 OCT1 OCT2 OCT3
Serial output counter monitor
The present serial output data number is read.
Serial interface monitor 3
Y1 Y2 Y4 Y8
ϕK11(9)
ICT0 ICT1 ICT2 ICT3
Operation monitor of serial counter
Serial input counter monitor
The present serial input data number is read.

1-1. Serial Interface Setting, Control Bit

(1) Setting of serial pin (PSEL, SIO bit)

I/O port 3 or I/O Port 8 can be used for serial input-and-output pins. I/O Port 3 is CMOS structure and I/O Port 8 is Nch open drain structure. Since impression to 5.5V is possible for I/O Port 8, it can do an interface with LSI of 5V system easily.

I/O port 3 is usually used to communicate with LSI of the VDD power supply drive of the same power supply system. This port can be used as Nch Open drain, and the impressed voltage can be used below the terminal V_{LCD} (3V) power supply. Therefore, it is possible to use it as an interface with system LSI power supply of 3V or less.

Set "0" to this control bit when the serial interface unused.

SIO	PSEL	Serial interface pin	Pin structure	Pin type	Maximum impression voltage
0	*	Each pin I/O Port operation	-	-	-
1	0	I/O port3	CMOS	CMOS or Nch open drain	~VLCD(3V)
1	1	I/O port8	Nch open drain	Nch open drain	~5.5V

Note : After the system is reset, these bits are reset in "0".

(2) Form of serial operation (M0, M1 bit)

Serial operation form can select three kinds of serial interface modes of 3 line type, 2 line type, and UART. Set "0" to this control bit for serial interface at the time of intact. It changes into the following function pin when the mode is selected.

M1	M0	Serial interface mode	Used pin and name					
			I/O port 3 select			I/O port 8 select		
0	0	Operation stop	P3-0	P3-1	P3-2	P8-1	P8-2	P8-3
0	1	2 line type interface	SCK1	SDIO1	P3-2	P8-1	SCK2	SDIO2
1	0	3 line type interface	SCK1	SDIO1	SI1(P3-2)	SI2(P8-1)	SCK2	SDIO2
1	1	UART	RX1	TX1	P3-2	P8-1	RX2	TX2

Note : After the system is reset, these bits are reset in "0".

(3) Clock Selection of Serial Operation (CK0, CK1, OSC0, OSC1 bit)

The serial operation clock sets the operation speed in the serial interface. At the time of 2 / 3 line type master setup, four kinds of speed (fosc/2, fosc/4, fosc/8, and fosc/16) of operation can be selected. Three kinds (9600/2400/1200bps) can be selected at the time of UART setup. The operation speed of 2/3 line type can speed up to 300 kHz or less, and can use transfer rate 19200bps of UART by using a high-speed oscillator. Select the operation clock referring to the next table.

These bits become don't care at the slave of 2/3 line type setting, and the serial clock up to 200 kHz can work at operation speed.

Note : When the type is set 2/3 lines, duty of the clock frequency is all 50%.

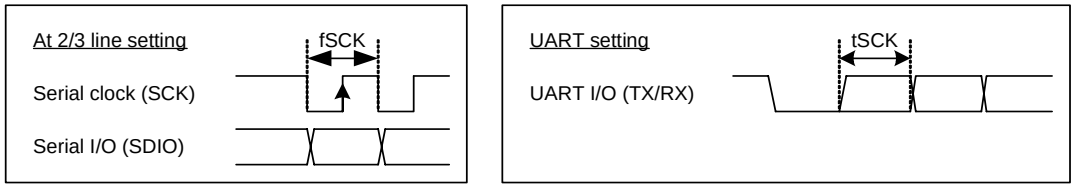
Note : OSC0 and the OSC1 bit become don't care in a prohibition state in high-speed ociloator.

Note : Set all these bits to "0" at the slave of 2/3 line type setting.

Note : After the system is reset, these bits are reset in "0".

Setting of frequency of serial clock (transfer rate)

OSC1	OSC0	Setting of ocillator	CK1	CK0	At 2/3 line setting of type Clock frequency (fSCK)		UART transceiver transmission rate (fSCK)		
0	0	Low-speed oscillator (75 kHz)	0	0	fosc/2	37.5kHz	-		
			0	1	fosc/4	18.75kHz	fosc/8bps	9375bps	9600bps mode
			1	0	fosc/8	9.375kHz	fosc/32bps	2344bps	2400bps mode
			1	1	fosc/16	4.6875kHz	fosc/64bps	1172bps	1200bps mode
0	1	High-speed oscillator (300 kHz)	0	0	fosc/2	150kHz	fosc/16bps	18750bps	19200bps mode
			0	1	fosc/4	75kHz	fosc/32bps	9375bps	9600bps mode
			1	0	fosc/8	37.5kHz	fosc/128bps	2344bps	2400bps mode
			1	1	fosc/16	18.75kHz	fosc/256bps	1172bps	1200bps mode
1	0	High-speed oscillator (450 kHz)	0	0	fosc/2	225kHz	fosc/24bps	18750bps	19200bps mode
			0	1	fosc/4	112.5kHz	fosc/48bps	9375bps	9600bps mode
			1	0	fosc/8	56.25kHz	fosc/192bps	2344bps	2400bps mode
			1	1	fosc/16	28.125kHz	fosc/384bps	1172bps	1200bps mode
1	1	High-speed oscillator (600 kHz)	0	0	fosc/2	300kHz	fosc/32bps	18750bps	19200bps mode
			0	1	fosc/4	150kHz	fosc/64bps	9375bps	9600bps mode
			1	0	fosc/8	75kHz	fosc/256bps	2344bps	2400bps mode
			1	1	fosc/16	37.5kHz	fosc/512bps	1172bps	1200bps mode



(4) Condition setting of serial operation

● MASTER bit (Selection of external/internal of SCK clock)

The master and the slave are set. It becomes master if a serial clock (SCK) is selected as internal clock. It will become a slave if it is selected as external clock.

At the time of master setup, if start setup is carried out to a serial start bit (TSTA1, TSTA 2 bit), serial operation will be started and serial clock will be outputted. And it stops by the condition precedent of a serial counter. The serial clock with which the serial clock was selected in the clock selection bit (CK0, CK1 bit) is outputted.

When the clock is input from the outside as for the slave setting, serial operation will be started automatically. An external clock can input the frequency below 200 kHz (fSCK) in 2 / 3 line type.

Selection of external/internal of SCK clock(Master bit)
- 0: External clock (Slave)
- 1: Internal clock (Master)

Note : Change to the slave setting when you set UART.

Note : After the system is reset, these bits are reset in "0".

● POL Bit (Logic selection of the serial clock of serial data)

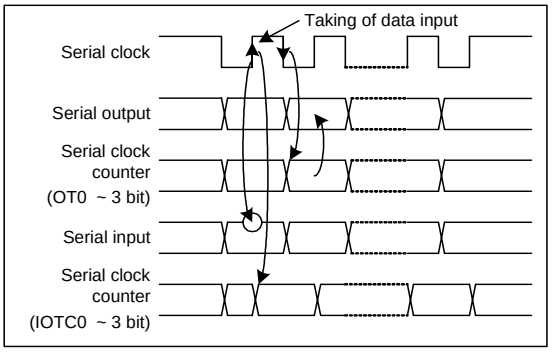
The logic of shift clock input and output of serial clock is selected.

If "1" is set as master bit and POL bit, serial operation will be stopped and a serial clock will stop on the "H" level. If serial operation is started, serial clock will output from the "H" level and it will stop on the "H" level. If "0" is set as a POL bit, it will become reverse logic and will become the above with operation from the "L" level.

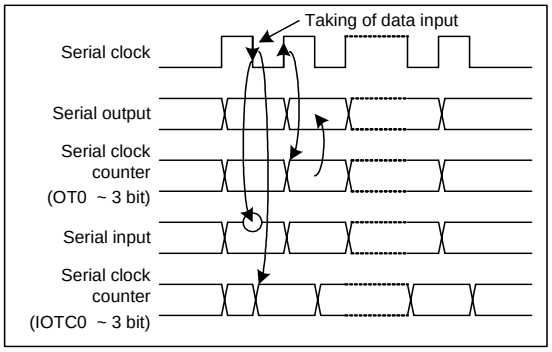
POL bit controls the operation edge of the serial counter by the serial clock I/O and the taking edge of serial input simultaneously with the output logic. P The timing operation by POL bit is as follows.

Logic selection of the serial clock of serial data (POL bit)
- 0: Positive logic output (SCK clock outputs it from "L" level.)
- 1: Negative logic output (SCK clock outputs it from "H" level.)

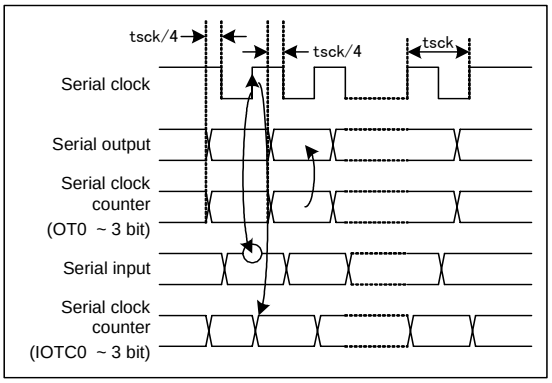
(A) At the time of 2 line type master slave and 3 line type slave setup (POL="1")



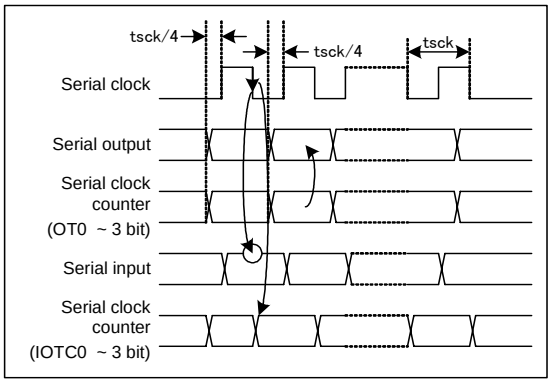
(B) At the time of 2 line type master slave and 3 line type slave setup (POL="0")



(C) At 3 line type master setting type (POL="1")



(D) At 3 line type master setting type (POL="0")



Note : The serial output at the time of 3 line type master setting (serial output counter) changes to the timing shifted tsck/4.

Note : The serial clock at the time of 2 line type master setting inputs and carries out serial operation of the clock of SCK pin. For this reason, serial operation is not started unless waveform is outputted for SCK pin by a certain cause.

Note : Change in "POL = 0 " at the time of UART setting.

Note : After the system is reset, these bits are reset in "0".

● NchS Bit (Selection of output form of serial I/O port pin)

The serial interface I/O circuit form is set. If "0" is set to this bit, the circuit type becomes CMOS type and if "1" is set, it becomes Nch Open drain type.

Select of output type of serial I/O port t pin (NchSL bit)
- 0: Select of CMOS output type
- 1: Select of Nch open drain output type

Nch	I/O port－1	I/O port－7
0	CMOS type	Prohibition of setting
1	Nch open drain type	

Note : Change to the Nch Open drain setting at the time of 2 line type setting.

Note : It becomes effective also at the time of UART setting.

Note : After the system is reset, these bits are reset in "0".

● SIS bit (Selection of the serial input of SDIO pin and SI pin)

The serial input pin is set. If "0" is set to this bit, serial input becomes it for the SDIO input pin. If "1" is set, it becomes SI pin.

The function as I/O Port of SI pin is also effective. Therefore, when SI input pin is used for serial input, it is necessary to set the I/O port corresponding to this pin to the input port. Moreover, when the SDIO pin is used for serial input, SI pi can be used as I/O port.

Select of serial input of pin SDIO and SI pin (SIS bit)
- 0: Select of SDIO intput pin
- 1: Select of SI input pin

Note : Change the I/O port corresponding to this pin to the input setting at the time of SI pin setting.

Note : SI pin can be used as usual I/O Port at the time of SDIO input setting.

Note : Change the SDIO input setting at the time of UART setting.

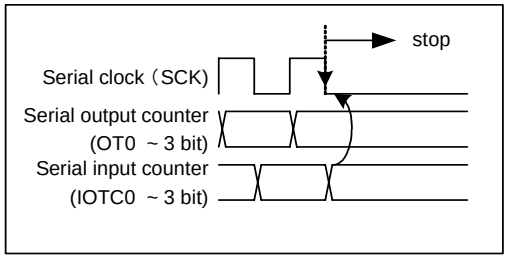
Note : After the system is reset, these bits are reset in "0".

● STPS Bit (Selection of serial clock counter stop condition)

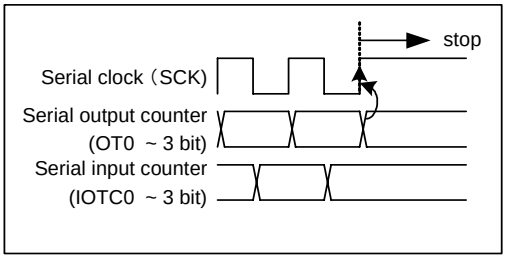
The serial operation stops when it becomes a position where the serial counter is stopped. In the serial counter, there are two systems of the serial output counter and serial input. This bit performs the change of an output or an input counter for stop condition.

Select of a serial clock counter stop condition (STPS bit)
- 0: Select of intput clock counter
- 1: Select of output clock counter

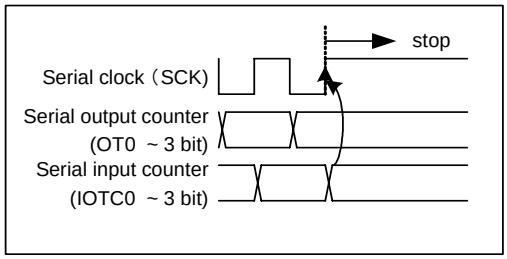
(A) At 2/3 line setting of type (POL="0", STP="0")



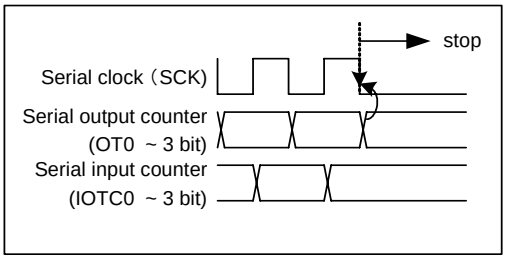
(B) At 2/3 line setting of type (POL="0", STP="1")



(C) At 2/3 line setting of type (POL="1", STP="0")



(D) At 2/3 line setting of type (POL="1", STP="1")



Note : Set it as STPS="1" (clock output counter selection) at the time of 2 line type and UART setting. It is m A/De setting of the above (B).

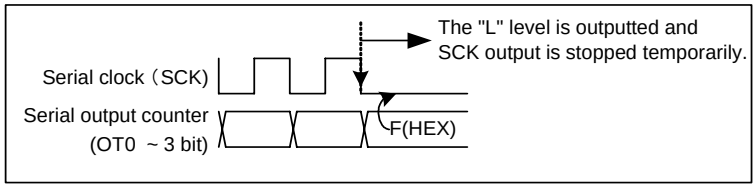
Note : After the system is reset, these bits are reset in "0".

● SWENA bit (Serial wait enable)

This control bit becomes effective only at the time of 2 line type setting. Usually, set up "1" at the time of 2 line type setting. When this bit is set as enable status at the time of 2 line type setting, if serial output counter (OCT0 to 3) is set to "F" (HEX), the "L" level will be outputted, SCK output will be in clock wait status and serial clock will stop.

Serial wait enable setting (SWENA bit)
- 0: Prohibition
- 1: Enable (Set up "1" at the time of 2 line type setting)

At 2 line setting of type (POL="1", STP="0", SWENA="1")



Note : Set it as SWENA ="0" at the time of 3 line type and UART setting.

Note : After the system is reset, these bits are reset in "0".

● SOS Bit (Output setting of SDIO pin serial output)

This control bit changes the data output and input of a serial data input and output pin (SDIO pin). "0" is set up at the time of serial data input, and "1" is set up at the time of a serial data output.

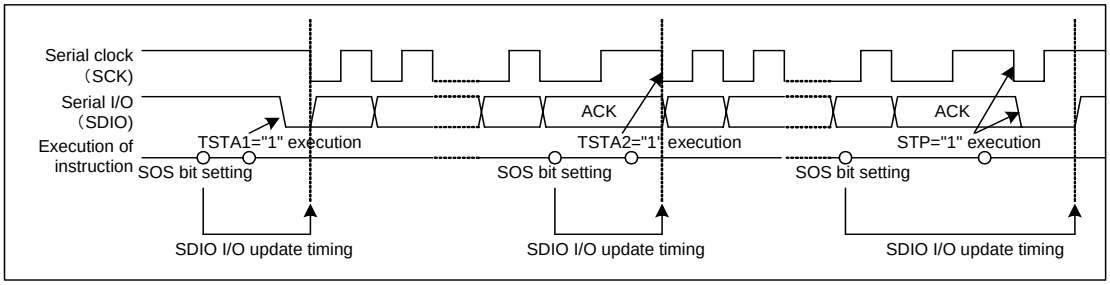
In the time of 3 line type setting, the change of input and output is changed at the time of the instruction execution to this bit. However, at the time of 2 line type setup, it is updated and set up on the following conditions after setting it as this bit.

Output setting of SDIO pin serial output (SOS bit)
- 0: Setting of SDIO pin input
- 1: Setting of SDIO pin output

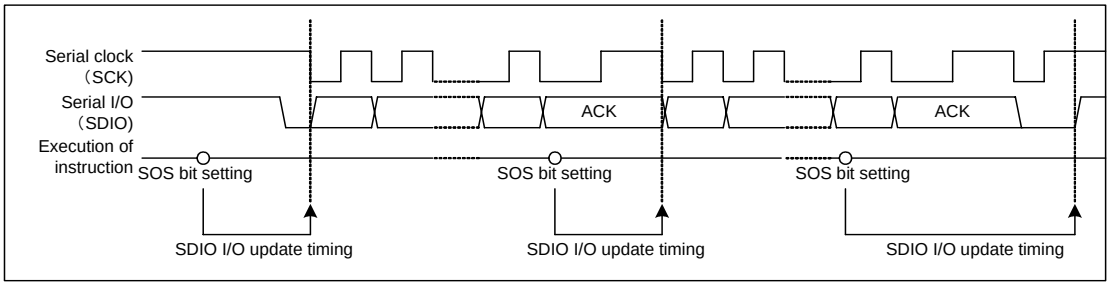
Update timing of terminal SDIO I/O switch at 2 line type

- Stop condition conditions
- Falling of the shift clock at the time of communication start
- Falling of the serial clock after ACK input and output

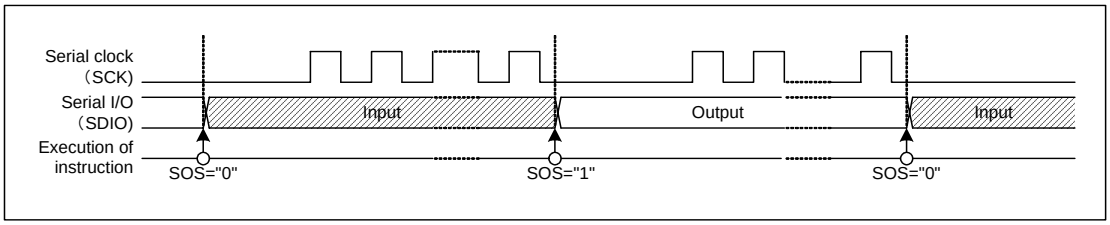
SDIO input and output change timing at the time of 2 line type setting (at the time of master setting)



SDIO input and output change timing at the time of 2 line type setting (at the time of slave setting)



SDIO input and output change timing at the time of 3 line type



Note : If it is set as an SOS bit, input and output of SDIO pin will be updated at the time of instruction execution at the time of 3 line type setting.

Note : At the time of UART setting, "1" is always set to SOS bit.

Note : After the system is reset, these bits are reset in "0".

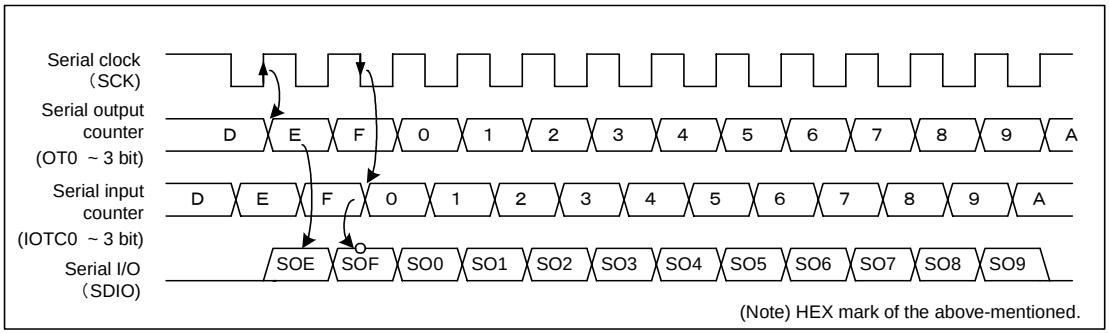
● MSB Bit (Selection of the bit order of serial data)

This control bit controls the arrangement of the serial data I/O data. Data input and output are selected from the MSB or LSB.

The serial data which designated the serial interface at the serial counter is outputted and inputted. Up or down of serial counter is controlled by the MSB bit. When "0" is set to the MSB bit, the serial counter does the up count. When "1" is set, the down count is done.

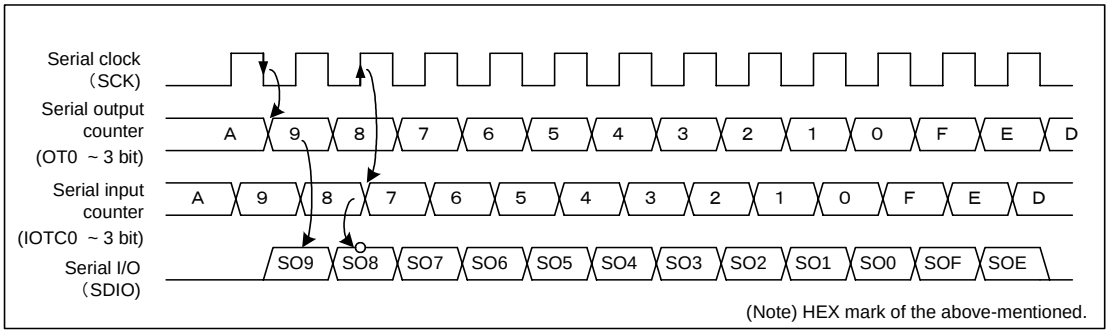
Selection of the bit order of serial data (MSB bit)
- 0: Setting of SDIO pin input
- 1: Setting of SDIO pin output

Serial counter and serial I/O timing (MSB="0", POL = "0" setting)



(Note) HEX mark of the above-mentioned.

Serial counter and serial I/O timing (MSB="1", POL = "1" setting)



(Note) HEX mark of the above-mentioned.

Note : The serial data corresponding to the serial output counter is output to the serial output pin, and the state of the serial input pin corresponding to the serial input counter is stored in the serial input data by the edge.

Note : As for the serial counter, the input counter and the output counter make the edge of the up or the down opposite.

Note : If the serial input and output data which does not exist at serial counter is specified, as for an output, "L" will be outputted and an input will serve as don't care.

Note : After the system is reset, these bits are reset in "0".

● Serial Counter, Serial Data
(STA0 to 3, STP0 to3, OCT0 to3, ICT0 to3 bit, SO0 to SO9/SOE/SOF, SI0 to SI9/SIE/SIF)

The serial counter consists of a serial input counter (CT0 to 3) which counts a serial input clock, and a serial output counter (OCT0 to 3) which counts a serial output clock. These serial counters are presetted to stop data (STP0 to 3) if stop is executed (STP="1"). When execution (TSTA1="1", TSTA2="1") of the start and the serial clock from the outside are input, serial counter starting data (STA0 to 3) is presetted to these serial counters. The serial counter is counted with the serial clock. The serial counter stops when the serial counter is corresponding to cereal stop data (STP0 to 3), and interrupt is issued.

The status of operation can be judged by the serial counter monitor (ICT0 to 3, OCT0 to 3).

- Start data of serial counter (STA0 to 3 bit)
  → When the serial operation is begun, the beginning data is set in the serial counter.
- Stop data of serial counter (STP0 to 3 bit)
  → Stop data will be set to a serial counter if stop execution (STP="1"). Moreover, after serial counter operation, serial operation stops in stop data position, and interruption is issued.
- Operating monitor of serial output counter (OCT0 to 3 bit)
  → The operation status of serial output side counter can be detected.
- Operating monitor of serial input counter (ICT0 to 3 bit)
  →The operation status of serial input side counter can be detected.

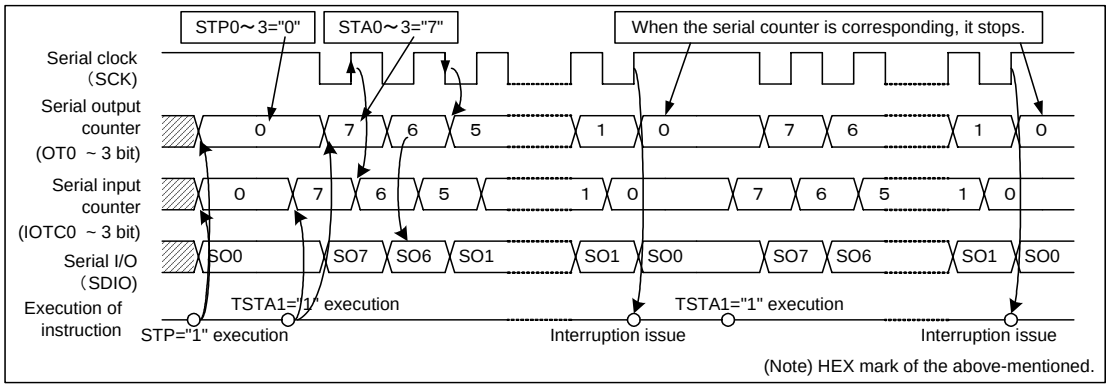
Serial data consists of 12 bits each of serial output data (SO0to SO9/SOE/SOF) and serial input data (SI0 to SI9/SIE/SIF). The serial data corresponding to the serial output counter number in serial output data is outputted to a serial output pin. The serial input data reads the state of the serial data input pin by the edge of the serial clock corresponding to the serial input counter number.

The SOE/SOF bit of the serial output data is automatically set in "1" by stop execution (STP="1") when mastering of the serial operation is set beginning at the time of setting two line type. Usually, the SO0/SI1 to SO7/SI7 bit is used in the serial I/O data, the SOE bit used in the output bit of the serial stop condition and the SOF/SIF bit is used for as I/O data of ACK.

The SO0/SI1 toSO7/SI7 bit is used in the UART I/O data, the SO8/SI8 bit is used for the parity bit and the S09 bit is used as a stop output data output respectively when UART is setting.

At the time of 3 line type setup, a maximum of 14-bit serial data input and output are possible. Set up a serial data start and stop data according to the number of bits and set up the number of bits.

The example of serial operating timing at the time of 3 line type setting (MSB="0", POL="0", STPS="1" setting)



(5) Start and Stop of Serial operation

● TSTA1, TATA2 bit (Start of serial operation)

The TSTA1 bit controls starting of the serial operation by the master setting. The serial clock is output when "1" is set to this bit and the serial interface operation is started.

The data of starting data (STA0 to 3) of the serial counter is presetted to the serial I/O counter. The serial output data corresponding to the starting data is output to the serial output data when the start is executed by 3 line type setting. Then, according to a serial clock (SCK), serial data (SO0 to SO9, SOE, and SOF) is outputted in order.

When starting execution is done by 2 line type setting, the start condition pulse is outputted to a serial data output, a start judgment is m A/De by this start condition, and serial operation is started. Moreover, when the starting execution is done by the UART setting, the start pulse is output from the TX pin. Afterwards, operation similar to 3 line type is done.

The start of operation by slave setup does not need to use this control bit and it is started with the serial clock from the outside.

The TSTA2 bit controls the restart of the serial operation at the time of 2 line type master. If beginning is executed by the TSTA1 bit, the start condition is output, the 8-bit serial clock operates, and it becomes the serial wait status after that. After ACK is input, the serial operation is restarted and input and output when "1" is set to the TSAT2 bit.

- Starting of serial operation at the time of a master (TSTA1 bit).
  → The serial operation starts when "1" is set at the time of master setting.
  The start condition is automatically output at the time of 2 line type setting.
  The start pulse is output at the time of UART setting.
- Execution of the restart at the time of 2 line type setting (TWTA2 bit).
  → Operation restarts at the time of "1" setting.

Note: If "0" is set to these bits, it becomes don 't care.

Note: Put the wait time more than one cycle of the serial operation clock during stop execution (STP="1") and start execution (TSTA="1").

● STP bit (The stop of serial operation)

STP bit controls the compulsive stop of serial operation under serial operation, initialization of an internal status and the output of stop condition.

If "1" is set as an STP bit (stop execution), serial counter is initialized, and serial counter stop data (STP0 to 3) is presetted and an internal status is initialized. The serial clock output stops when the stop execution is done while the serial is operating by the master setting.

When stop execution is done by 2 line type setup of a master, in addition to the above-mentioned operation, stop condition is automatically outputted from serial data output and serial clock.

- The stop and initialization of serial operation at the time of a master(STP bit)
  → Operation stops when "1" is set and it is initialized.
  The stop condition is automatically output at the time of 2 line type setting.

Note: If "0" is set to this bit, it becomes don 't care.

Note: Execute the stop for internal initialization after setting the condition (STP="1").

(6) Serial operation monitor

● BUSY1/BUSY2 bit (Operation monitor)

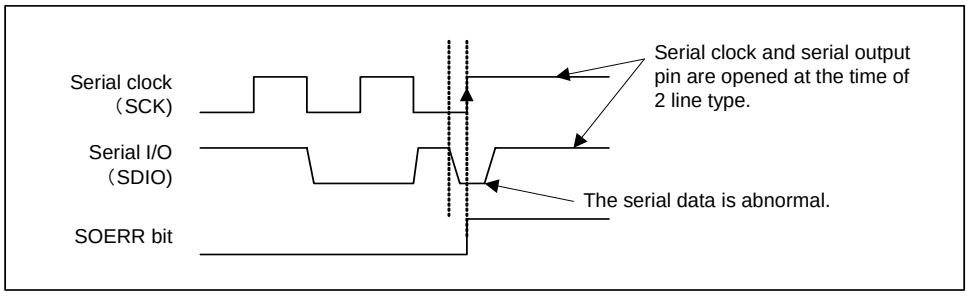
The BUSY1/BUSY2 bit detects a serial operation status. The serial clock operation can be detected in the BUSY1 bit. BUSY2 bit can detected the state of 2 line type of operation or the reception operation state of UART. Interrupt is issued by the falling the BUSY1 bit when interrupt has been enabled and the program branch to 0001H address.

● SOERR bit (2 line type serial output error flag)

The SOERR bit is used for detection of the Arbitration in 2 line type multi-master specification. Internal output data and the output are compared when the serial data of the master is output, the serial operation stops automatically for the disagreement, and the SOERR bit is set in "1".The serial clock and the serial data are opened and operation enters the state of continuance if this state is detected. In the detection of a usual arbitration, the clock from other masters is supplied and the serial operation finished. After 2 line type operation finished, FF Reset="1" is set up and flag is reset.

This detection does the detection operation regardless of master-slave because it is done when the serial output is set. For this reason, program processing is required when output data becomes disagreement by the noise etc. detect this bit and initialize by setting "1" as an STP bit and carrying out stop execution in the state of "1". Detect this bit when the interrupt issue or the BUSY1 signal doesn't become "L" even if certain fixed time passes usually. Set "1" to the STP bit, do the stop execution, and initialize it when this bit is "1".

When modes other than 2o line type are set, this bit becomes don 't care.



● RX F/F bit (Receiving flag)

The RX F/F bit detects UART or 3 line type slave's reception. This bit is effective only that the slave is set. When the serial clock receives the input or UART by the slave setting, this bit is set in "1". Refer to the serial receive data after the reception ends. When "1" is set to the FF Reset bit, this bit is reset in "0".

● F/F Reset bit (Reset of internal flag)

The internal flag is initialized. Whenever "1" is set, the internal flag is reset.

serial reception execution flag (RX F/F), serial data output abnormality detection flag (SOERR) at the time of 2 line type setting and the serial wait are reset and released.

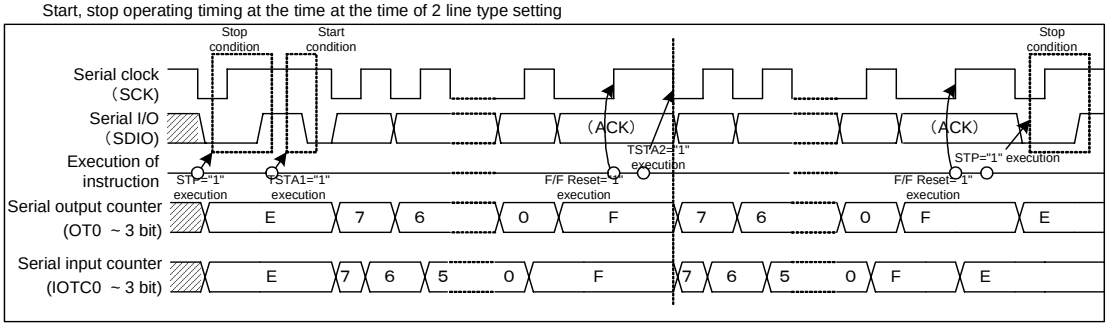
Moreover, at the time of 2 line type setting, it becomes in wait status after a serial output data SOF bit output. The SOF/SIF bit is used as acknowledge (ACK) bit usually. When the cereal operation is restarted, it restarts by the F/F Reset bit execution after reading the ACK bit I/O.

・Reset of internal flag (F/F Reset bit)

→An internal flag is reset whenever it sets ″1.″

The wait status at the time of 2 line type setting is released.

Start, stop operating timing at the time at the time of 2 line type setting



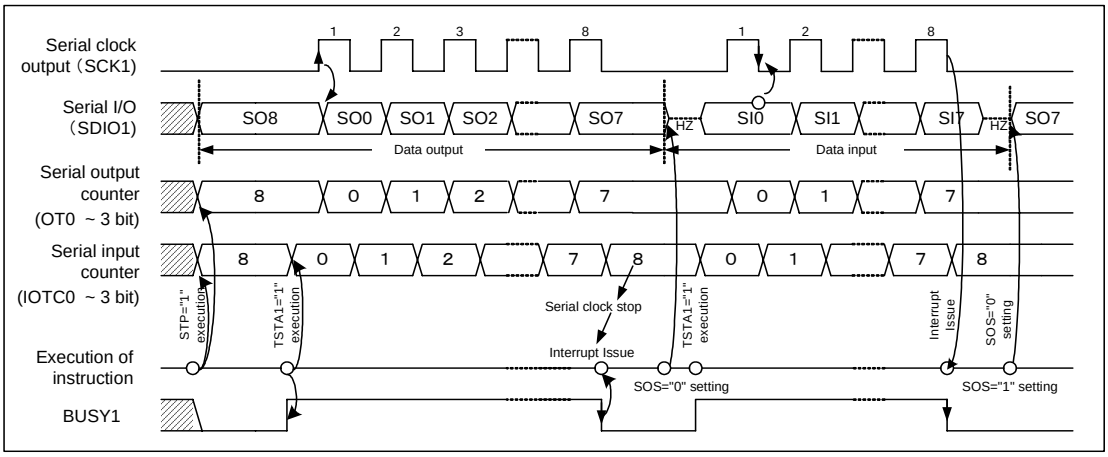
1-2. Example of Setting Serial Mode

The example of setting 3 line type, 2 line type, and UART is shown below. Set it according to the requested specification.

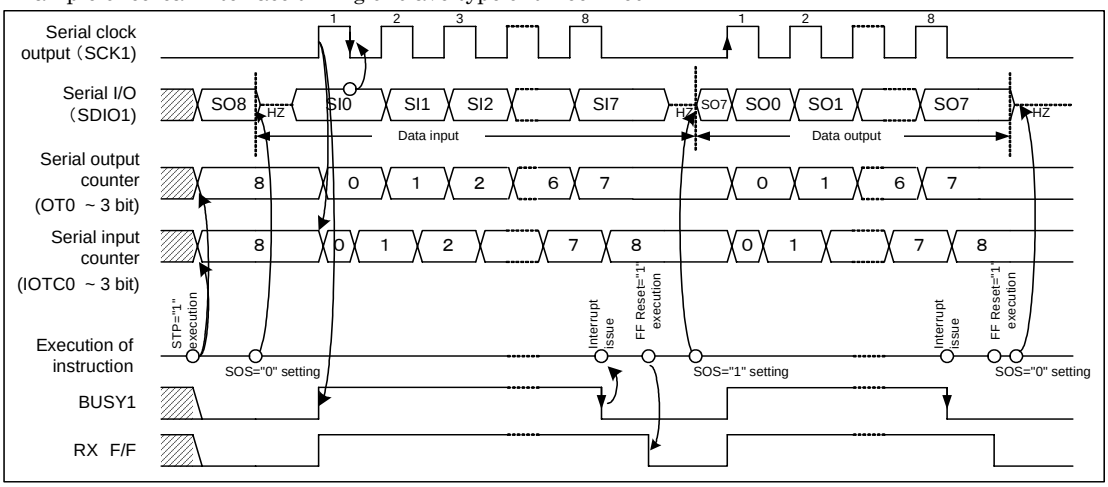
(1) Example of setting of 3 line serial mode

Setting bit	Condition setting data
M0,M1	3 line type setting (M0=0, M1=1)
CK0,CK1,OSC0,OSC1	Serial clock frequency setting
MASTER	Master setting (MASTER=1) : Refer to the example of master operating timing Slave setting (MASTER=0) : Refer to the example of slave operating timing
POL	Serial clock stop status =L Data output in rising, data output in falling (POL=0)
NchS	CMOS type setting NchS=0）
SIS	The SDIO pin is set to serial input. (SIS=0)
STPS	The stop condition is set to the input counter. (STOPS=0)
SWENA	Stop wait prohibition (SWENA=0)
MSB	Output from the LSB (MSB=0)
SOS	At data output: SOS=1, At data input: SOS=0
STA0～3	Serial I/O starting data: 0h
STP0to3	Serial I/O stop data: 8h
PSEL,SIO	Select (PSEL=0, SIO=1) of CMOS structure pin (SDIO1, SCK1).

・Example of cereal interface timing of master type of three lines

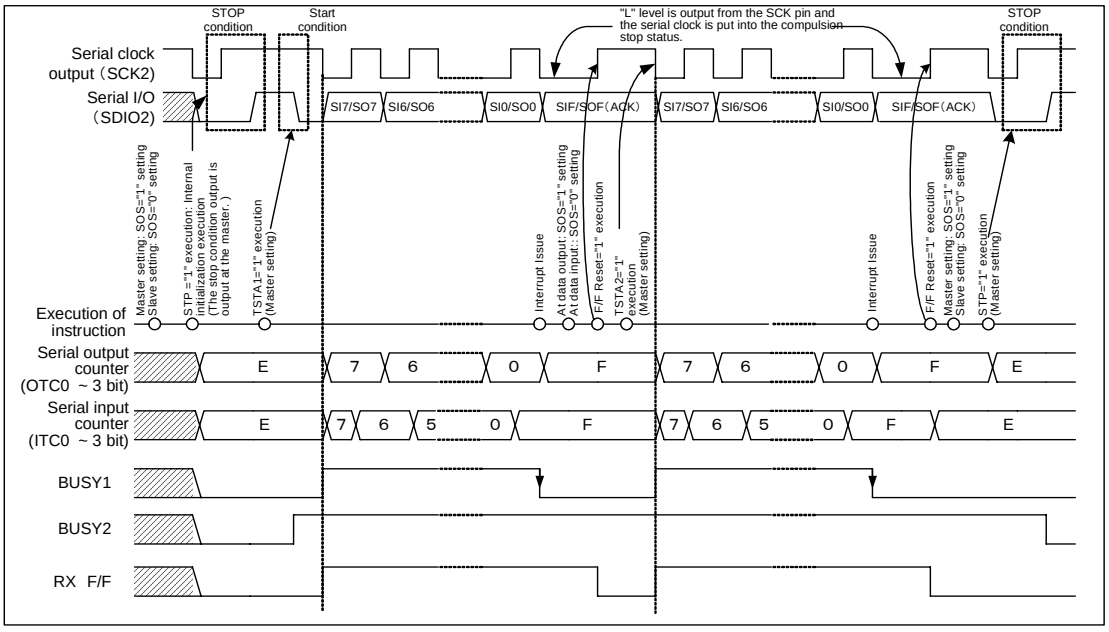


・Example of cereal interface timing of slave type of three lines



(2) Example of setting of 2 line serial mode

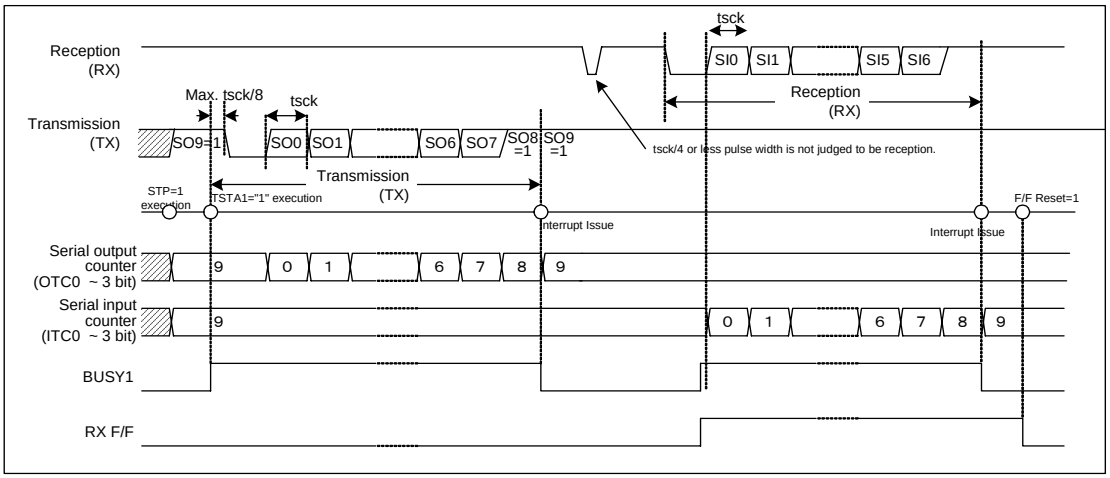
Setting bit	Condition setting data
M0,M1	2 line type setting (M0=1, M1=0)
CK0,CK1,OSC0,OSC1	Serial clock frequency setting
MASTER	Master setting (MASTER=1) : Refer to the example of master operating timing Slave setting (MASTER=0) : Refer to the example of slave operating timing
POL	Serial clock stop status =H Data output in falling, data intput in raising (POL=1)
NchS	Nch open drain type setting (NchS=1)
SIS	The SDIO pin is set to serial input. (SIS=0)
STPS	The stop condition is set to the input counter. (STPS=1)
SWENA	Stop wait enable (SWENA=1)
MSB	Output from the MSB (MSB=1)
SOS	At the time of data output: SOS=1, At the time of data input: SOS=0
STA0～3	Serial I/O starting data: 7h
STP0to3	Serial I/O stop data: 8E
PSEL,SIO	Select (PSEL=1, SIO=1) of Nch open drain structure pin (SDIO2, SCK2)



Note: In the master setting, start condition (STA1="1") cannot be output according to the ACK I/O timing under 2 line type operation (BUSY2="1"). Output the start condition after outputting the stop condition once.

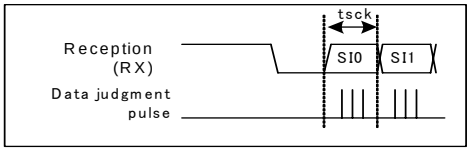
(3) UART モードの設定例

Setting bit	Condition setting data
M0,M1	UART setting (M0=1, M1=1)
CK0,CK1,OSC0,OSC1	Transceiver rate setting
MASTER	Master setting (MASTER=0)
POL	Serial clock stop status =H Data output in falling, data input in raising (POL=0)
NchS	Nch open drain type setting (NchS=1)
SIS	The serial data pin is set to the RX pin. (SIS=0)
STPS	The stop condition is set to the input counter. (STPS=1)
SWENA	Stop wait prohibition (SWENA=0)
MSB	Output from the LSB (MSB=0)
SOS	Data output setting (SOS=1)
STA0～3	Serial I/O starting data: 0h
STP0to3	Serial I/O stop data: 9E
PSEL,SIO	Select (PSEL=1, SIO=1) of Nch open drain structure pin (TX2, RX2)



Note: The start of reception is canceled when tsck/4 or less pulse width is inputted at the time of reception (RX).

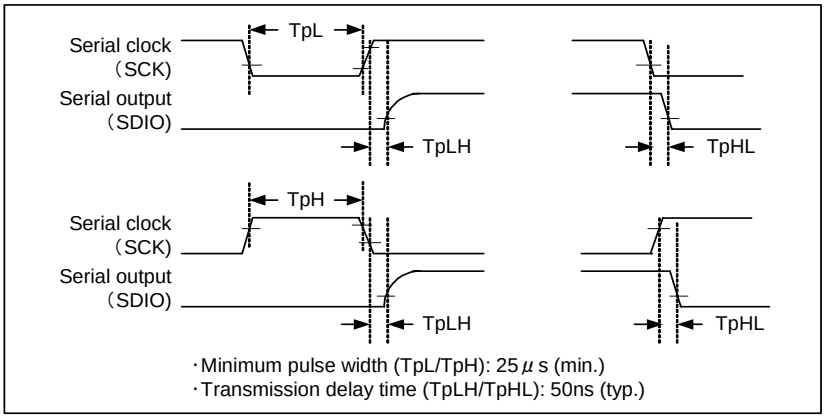
Note: The UART circuit has the data judgment circuit. If reception is started, data judging circuit will output the data judging pulse of three pulses in a data position, and judge RX pin status. When two pulses or more are the same data among these pulses, receive data is read as a serial data input. That is, it is normally receivable even if the noise of one pulse etc. occurs among pulse output positions.



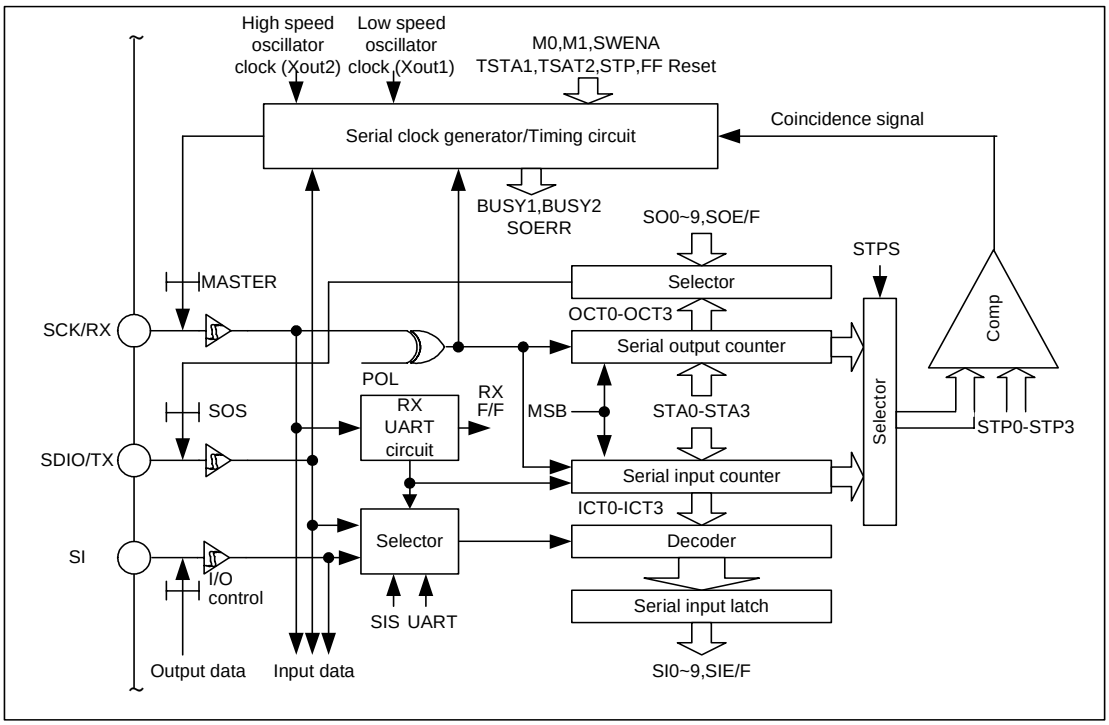
Note: The above-mentioned example is a transceiver example without parity. The SO8 bit output is output as stop bit. In the case of specification with a parity bit, 8 bits of SO8/SI can be assigned at parity. However, when transmission (TX) starts at once after interrupt issues it, the width of the stop bit cannot be secured. In this case, after interrupt is issued, execute the transmission after wait doing more than the width of the stop bit .

Note: UART of this product corresponds to a full duplex specification. Even if the transmission and the reception are executed at the same time, it is possible to send and receive it normally. However, the BUSY1 bit becomes "0" when either operation ends, and interrupt is issued. Therefore, judge the reception by the RX F/F bit.

1-3. Serial Clock Timing



2. Serial Interface configuration



Note: The pin only for sSerial input can be used as I/O port while the serial interface function is operating. It is necessary to make the I/O port to the input setting when using it as SI pin.

Note: All the pinls for serial interfaces are the Schmidt inputs.

Note: When the break of the I/O port input is enabled, the wait instruction and the clock stop instruction are released by the input change in serial input at the time of using theserial interface function. However, it is necessary to read the input of the I/O port according to the I/O port control before the instruction is executed of the input setting doing. After 100ms standby passes, the execution of CPU is started when the clock stop is released.

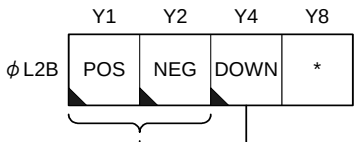
Note: When the serial interface function is used, the pull-up / pull-down of I/O port 3 can be set.

○ Pulse Counter

The pulse counter is 8-bit up/down counter and detection of the number of clocks can be performed with PCTRin pin (P3-3). It can use for the count and detection of a tape run.

1. Pulse Counter Control Port, Data Port

Pulse counter control 1



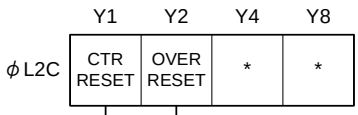
Setting 8 bit up/down counter

0: Up count operation
1: Down count operation

Setting input pin (PCTRin pin) counter input edge

POS	NEG	P3-3/PCTRin	Input edge
0	0	P3-3	-
1	0	PCTRin	Rising edge
0	1		Falling
1	1		Both edge

Pulse counter control 2

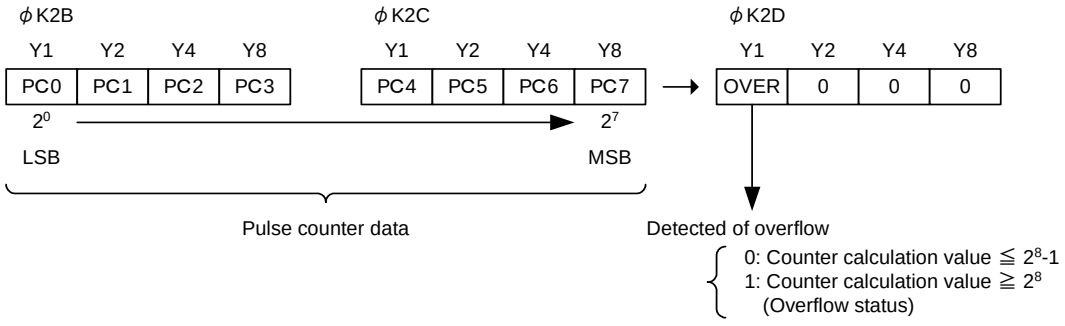


Reset of overflow detection F/F

Whenever it sets "1", OVER F/F is reset.

Reset of pulse counter reset

Whenever it sets "1", 8-bit rise down counter is reset.



0: Counter calculation value ≦ 2^8-1
1: Counter calculation value ≧ 2^8
(Overflow status)

The pulse counter measures pulse number of PCTRin (P3-3) pin.

POS and NEG bit set up the clock edge of input pin. The rising edge, the falling edge, and both edges can be selected. Usually, this bit is used fixed.

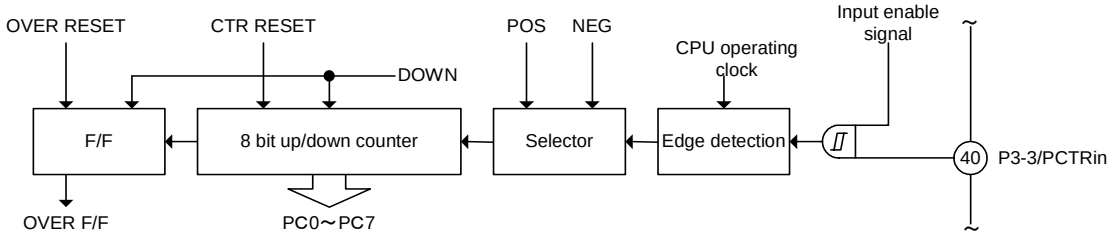
DOWN bit sets up an up/down of 8-bit counter. If it sets to "0" and it will set to rise count operation and "1", down count operation will be done. A change of a rise/down can be performed freely. However, if a clock pulse is inputted during change command execution, since it is canceled, be careful of this count.

When 2^8 or more pulses are inputted, OVER F/F bit is set to "1". When performing count operation of 8-bits or more, this OVER F/F are detected, and on a data memory, only the number of times of overflow is added and subtracted, and can correspond. After detection by this bit, and OVER RESET bit is set "1" and OVER F/F is reset. CTR RESET bit resets only 8-bit counter. The counter is reset whenever it sets "1".

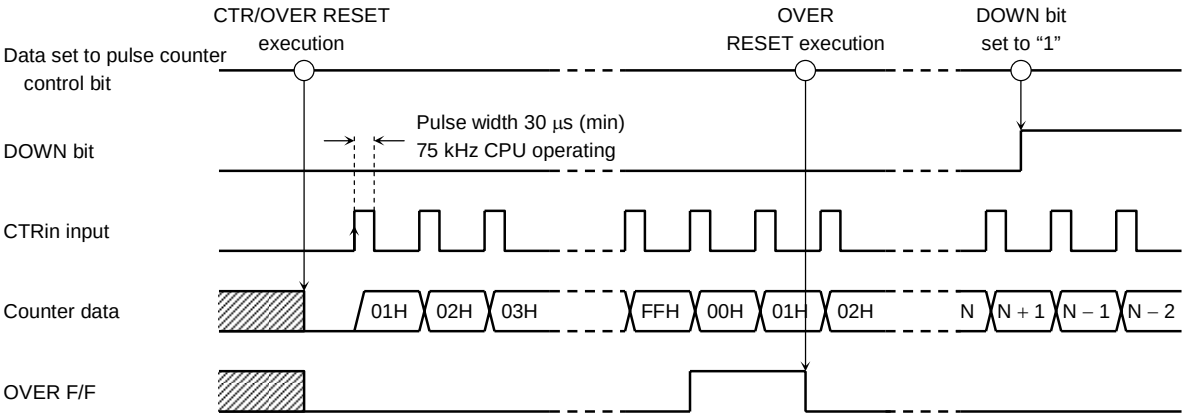
Counter data loaded data in a data memory by the binary.

The control of pulse counter and data loading is accessed with the OUT2/IN2 instructions for which [CN = BH to DH] have been specified in the operand.

2. Pulse Counter Circuit Configuration



3. Example for Pulse Counter Timing



Note: The CTRin input pin is Schmidt input.

Note: The pulse counter samples and judges of edge with a CPU operation clock (at the time of a low-speed clock 75kHz). For this reason, The pulse counter samples and judges of edge with CPU operation clock (at the time of low-speed clock 75kHz). Therefore, input the pulse width twice or more CPU operation clock.

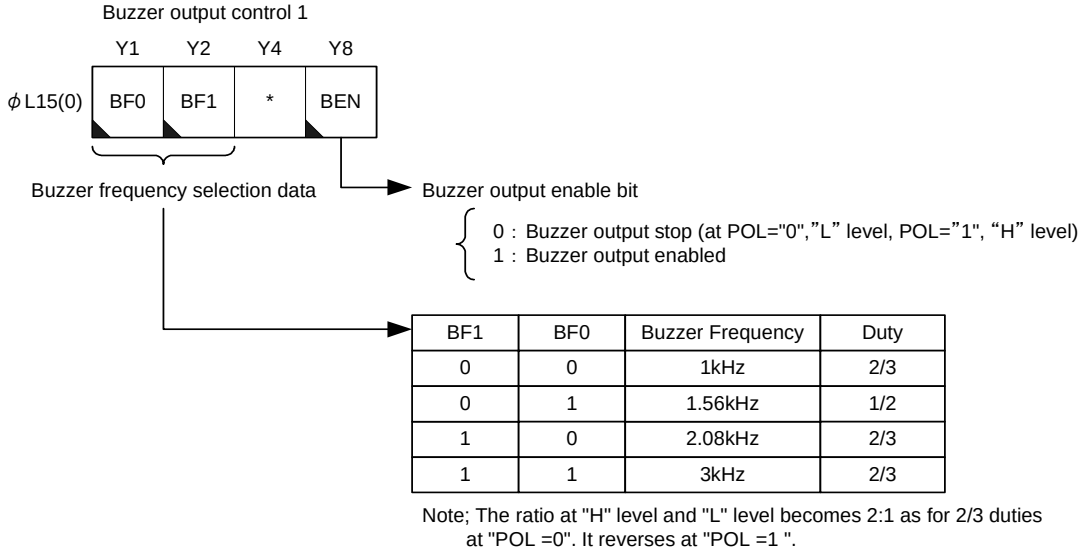
Note: When the break of the I/O port input is enabled, the wait instruction and the clock stop instruction are released by the input change in serial input at the time of using pulse counter function. However, re A/Ding the input of the I/O port is necessary before the instruction is executed of the input setting doing, and the first pulse is not counted by the I/O port control. After 100ms standby passes, the execution of CPU is started at the time of clock stop release.

Note: The pull-up / pull down setup of I/O Port 3 can be set at the time of using the pulse counter function.

○ Buzzer Output

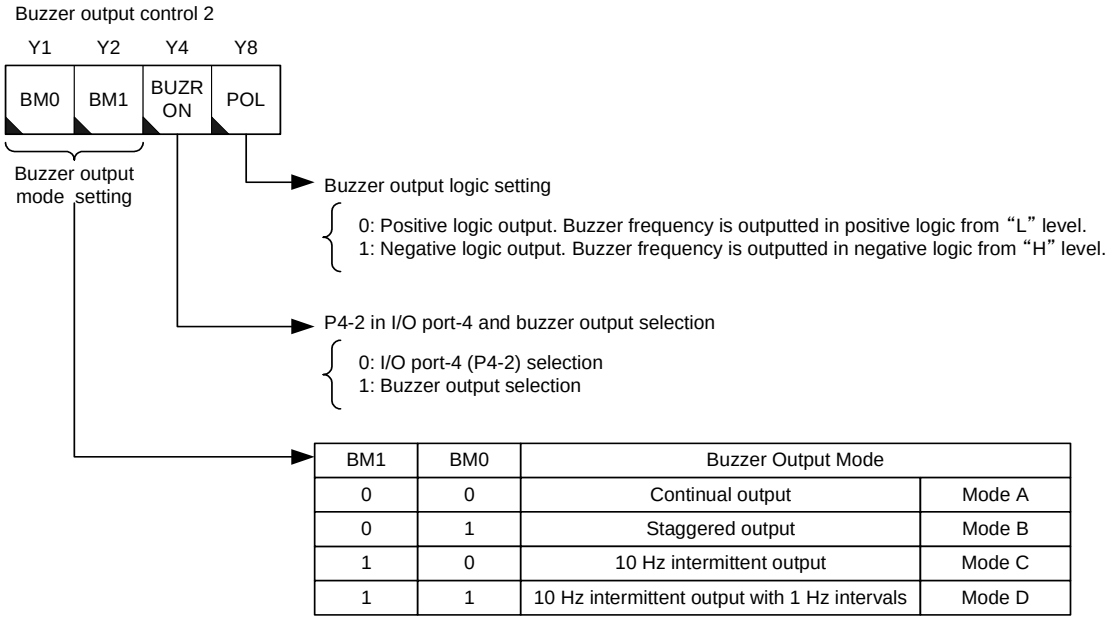
The buzzer output can be used to output tones and alarm tones to confirm key operations and the tuning scan mode. Buzzer type scan be selected from a combination of four output modes and eight different frequencies.

1. Buzzer Control Port

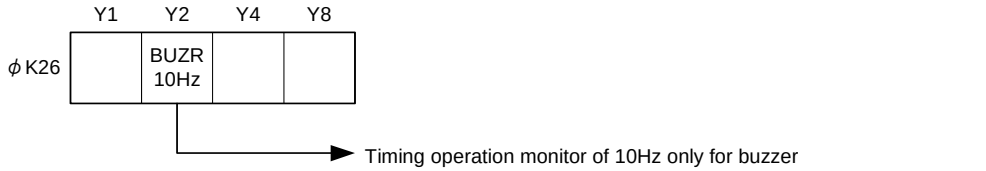


BF1	BF0	Buzzer Frequency	Duty
0	0	1kHz	2/3
0	1	1.56kHz	1/2
1	0	2.08kHz	2/3
1	1	3kHz	2/3

Note; The ratio at "H" level and "L" level becomes 2:1 as for 2/3 duties at "POL =0". It reverses at "POL =1 ".



BM1	BM0	Buzzer Output Mode	
0	0	Continual output	Mode A
0	1	Staggered output	Mode B
1	0	10 Hz intermittent output	Mode C
1	1	10 Hz intermittent output with 1 Hz intervals	Mode D



Note: 10 Hz operates by the base clock 100 Hz when "1" is set to the BEN bit. However, please refer to 10 Hz timer at the time of a Mode D setting.

The buzzer output is used also P4-2 I/O Port. In order to set it as a buzzer output, BUZR ON bit is set up "1" and it changes to a buzzer output by setting it as an output by the P4-2 I/O control port. After logic setting up of buzzer frequency, mode setup and a logic setup, buzzer enable bit is set up "1", it outputs buzzer. At the time of condition setup, buzzer enable bit is setup "0".

In Continuation output mode (mode A), if buzzer enable bit is set "1", buzzer frequency will be outputted continuously, and if "0" is set, a buzzer output will stop. In staggered output mode, whenever buzzer enable bit is set "1", buzzer is outputted and stopped between 50 ms.

Under a buzzer output (50 ms), if buzzer enable bit is set "1"again, 50 ms extension is carried out and the buzzer of 100 ms can be made to output.

Since it will be extended with 150 ms if it sets again between extended 50 ms, buzzer output time can be set up easily.

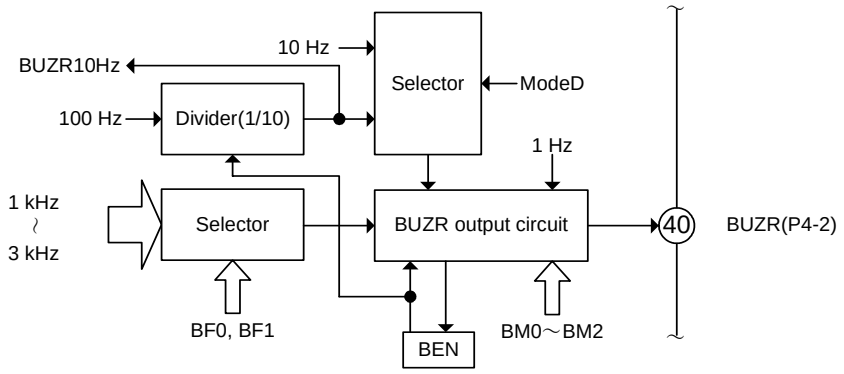
10 Hz intermittence output mode (mode C), if buzzer enable bit is set of "1", 50 ms buzzer output and 50 ms buzzer pause is carried out continuously. And a set of "0" stops a buzzer output.

10 Hz intermittent output with 1 Hz intervals mode (mode D), if buzzer enable bit is set "1", 50 ms buzzer output and 50 ms buzzer pause will carry out 500 ms output, after that 500 ms pause output of 50 ms buzzer output and the 50 ms buzzer pause is carried out again, and this operation is repeated. A set of "0" stops a buzzer output.

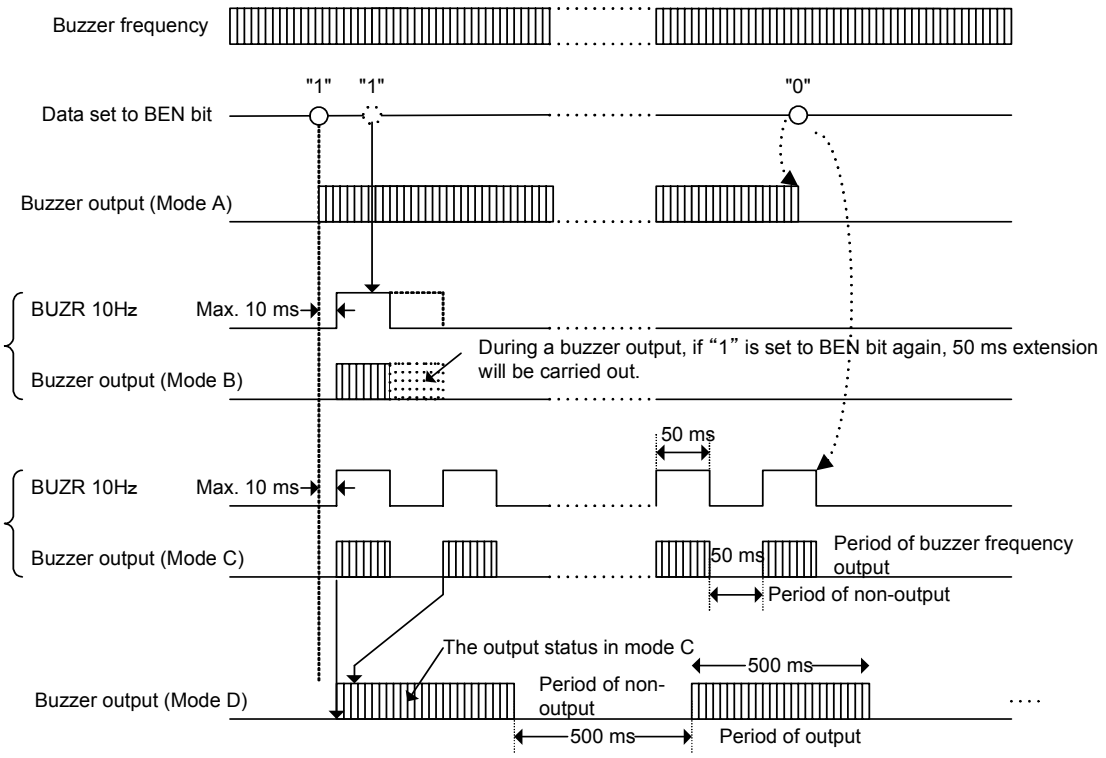
At mode B, C, and D, a buzzer is in an output state, even if it sets "0" to buzzer enable bit and it makes it stop, the buzzer of 50 ms is outputted and stops. In addition, a buzzer output state can be judged according to the contents of BUZR10Hz bit. The BUZR10Hz bit is "0", buzzer is an output state and it is in a pause state at the time of "1". However, refer to 10Hz timer at mode D.

The control of the buzzer is accessed in data port 6 of the OUT1 instruction.

2. Buzzer Circuit Configuration



3. Buzzer Output Timing



Note: When making a buzzer output, it sets up an output state about P 4-2 (set "1" to I/O control port).

Note: It stops compulsorily when setting it to BEN=0.

Note: When the frequency setting is changed while outputting the buzzer, it is updated and it is changed by the change in 10Hz timing at the time of mode B setting.

○ LCD Driver

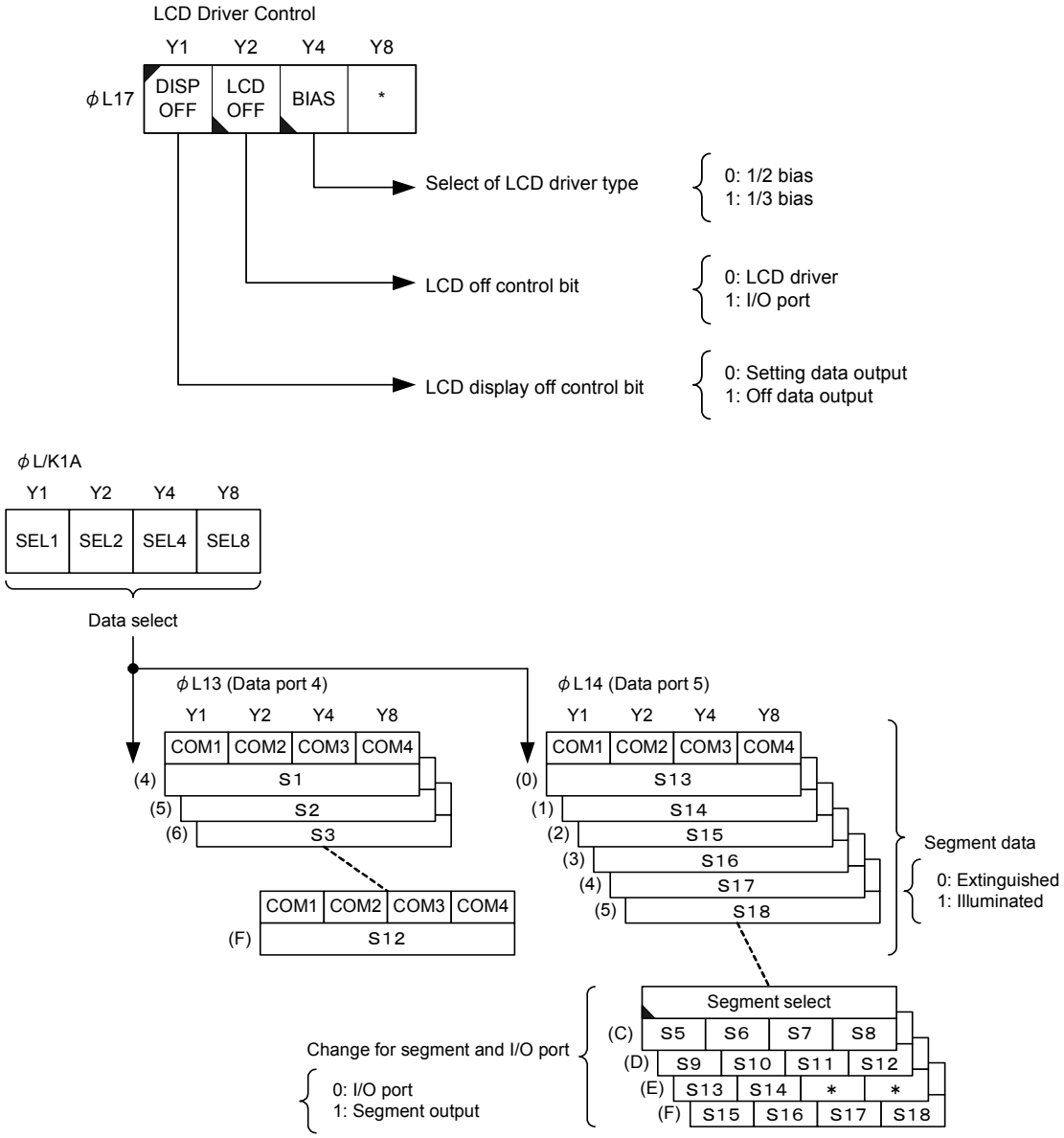
The LCD driver is using also I/O port and can make a maximum of 72 segments turn on. When LCD driver is permitted, I/O port 10 changes to COM1 to COM4 pin, I/O port 12 change to S1 to S4 pin and setting can do 14 of I/O port 13/14/15/16 to a segment pin output for every pin.

1/4 duty 1/2 biases (the frequency of the frame 62.5Hz) or 1/3 bias drives (the frequency of the frame 125Hz) can be selected LCD driver's drive system.

The LCD driver is built-in a constant voltage circuit (V_{EE} = 1.5 V) for display purposes and a voltage doubler circuit (V_{LCD} = 3.0 V)For this reason, the LCD display stabilized even if it changed power supply voltage can be performed. (Refer to section in LCD driver doubler circuit.)

The common output is output three potential (V_{LCD}, V_{LCD} ×1/2, and GND) and the segment output is output two potential (V_{LCD} and GND) when 1/2 biases are set the LCD driver output. The common and segment output is output four potential (V_{LCD}, V_{LCD} ×2/3, V_{LCD} ×1/3 and GND) when 1/3 biases are set the LCD driver output.

1. LCD Driver Port



Note : The segment data controls lighting/turning off the segment corresponding to common output and the segment output.

The LCD driver control port is arranged in the data ports 4 and 5 selected in the selection port. These ports are accessed by the OUT1 instruction that specified [CN=3H, 4H] to be operand parts.

● Segment data of a LCD driver

The segment data of a LCD driver is set by data port 4 and 5(ϕL13, ϕL14). The LCD display is turned off when "0" is set to the segment data port and the LCD display is lights when "1" is set in the segment data port.

● LCD OFF bit

The LCD OFF bit controls the switch of the LCD output pin and the I/O port. After reset, I/O port and LCD driver's pins of using combined are I/O ports. When the LCD driver function is used, "0" is set to this bit. When the LCD driver function becomes enable, four I/O port P10-0 to P10-3 pins change in the COM1 to COM4 output pin and four P12-0 to P12-3 changes into the S1 to S4 output pin.

Note: After system reset, this bit is set to "1."

● DISP OFF bit

The DISP OFF bit is able not to set the segment data and to turn off all the LCD display. When "1" is set in this bit, the LCD display is turned off all. At this time, the segment data is maintained, and when "0" is set in the DISP OFF bit, a former display will be displayed on LCD.

Note: Rewriting the segment data is possible while the DISP OFF.

Note: After the CKSTP instruction is executed, the DISP OFF bit is set to "1". For this reason, set "0" as DISP OFF bit after CKSTP instruction release if needed.

Note: After system reset, this bit is set to "1."

● BIAS bit

The BIAS bit selects the liquid crystal driver system. If "0" is set as this bit and it becomes 1 / 2 bias system (frame frequency of 62.5Hz) and "1" will be set up, it becomes 1 / 3 bias system (frame frequency of 125Hz).

Note: About about 100μA current consumption increases compared with 1/2 bias setting it when 1/3 bias is set.

Note: After system reset, this bit is reset to "0."

● Segment select port

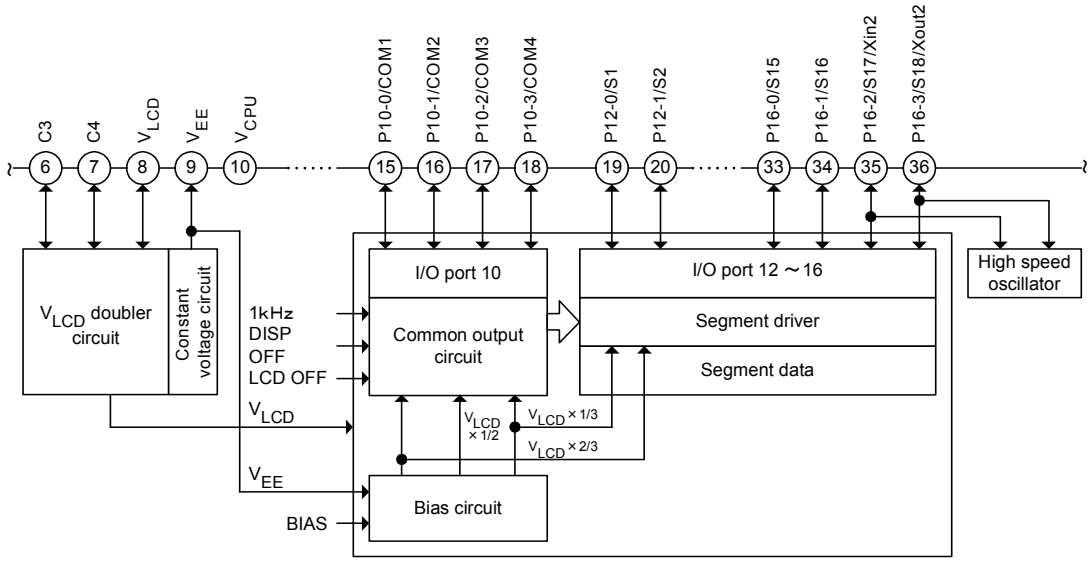
14 of I/O ports 13 to16 can be switched to the pin segment every one pin. If "1" is set in the bit corresponding to each segment, it becomes a segment output. If "0" is set, it becomes I/O port. The S5 to S8, S9 to S12, S13 to S14 and S15 to S18 bit correspond to the P13-0 to P13-3, P14-0 to P14-3, P15-0 to P15-1 and P16-0 to P16-3 pin.

Note: The segment output and I/O port can be set regardless of LCD off control bit (LCD OFF). If LCD OFF control bit is not set as LCD driver, the segment is not output to set to the segment output pin.

Note: S21 and S22 pin are used combinedly with the high-speed oscillation pin. The high-speed oscillation function is given to priority over the high-speed when it is selected as the high-speed oscillation pin and this port becomes don't care.

Note: After system reset, this bit is reset to "0."

2. LCD Driver Configuration



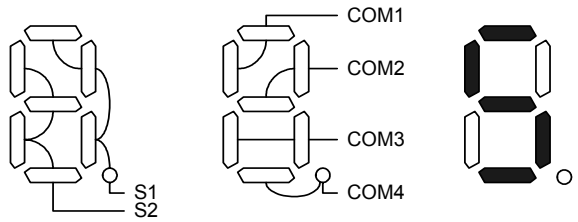
Note: After system reset, all LCD driver combination pins become the input status of the I/O Port.

Note: The LCD driver pin uses the I/O port and the high-speed oscillation pin combinedly.

3. LCD Driver Operating Timing

- LCD output waveform at the time of 1 / 2 bias setting (BIAS bit ="0")

  The potential of the LCD driver wave form outputs potential the V_{LCD} , V_{EE} and GND level by the frequency of the frame 62.5Hz at 1/2 biases.

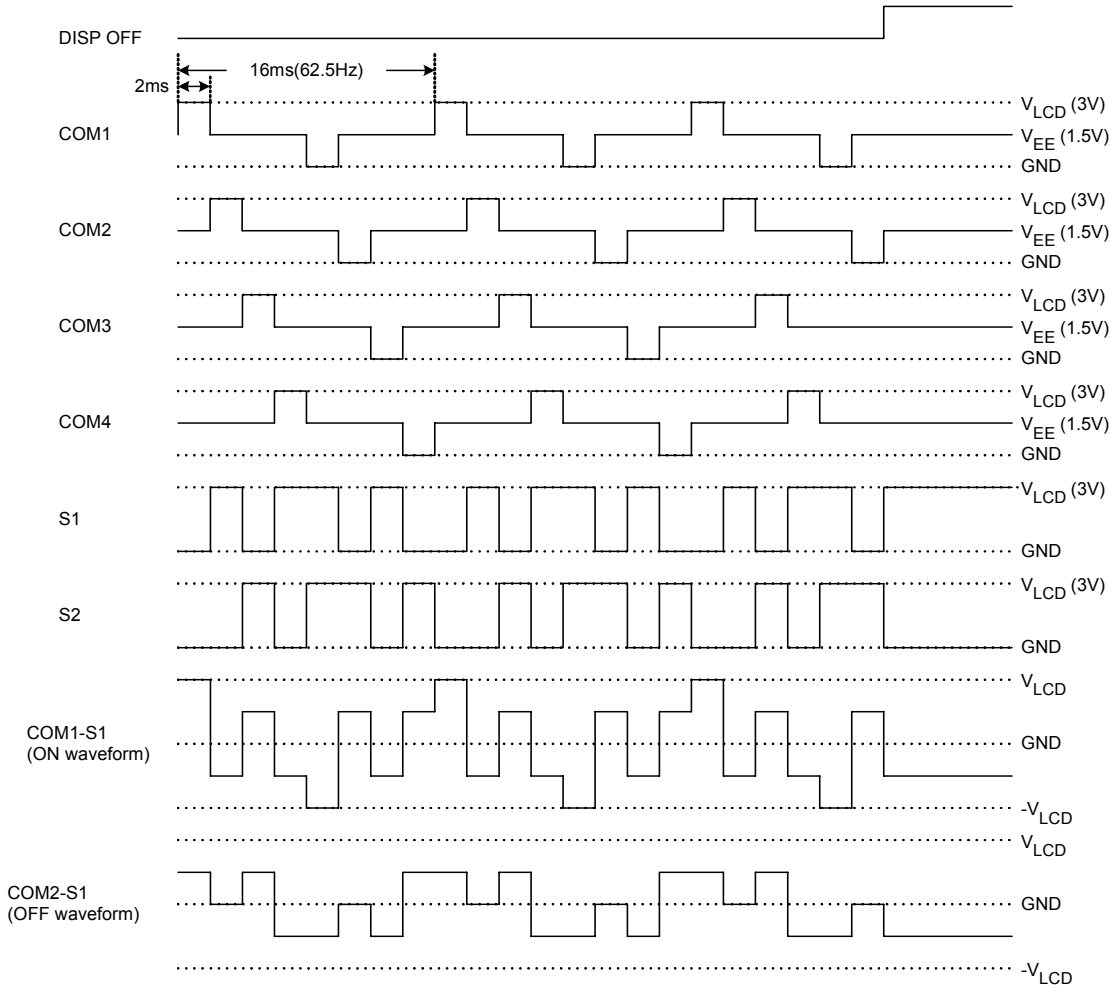


The example of segment data

Segment data (ϕ L13, ϕ L14)

	Y1	Y2	Y4	Y8
0 (S1)	COM1	COM2	COM3	COM4
	1	0	1	0
1 (S2)	COM1	COM2	COM3	COM4
	1	1	0	1

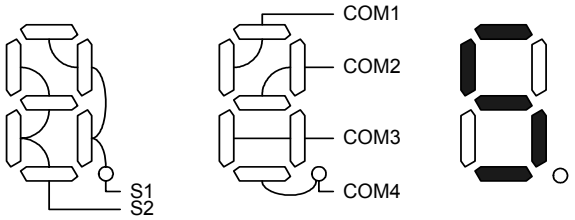
Data select (ϕ L/K1A)



Note: A common output becomes VLCD×1/2 level if "1" is set to the DISP OFF bit, and all the displays are turned off.

Note: All common outputs and segment outputs are fixed to the "L" level between 100ms the time of clock stop mode and after clock stop mode release.

- LCD output waveform at the time of 1 / 3 bias setting (BIAS bit ="1")
  The potential of the LCD driver wave form outputs the middle potential level of 1/3, 2/3 of V_{LCD}, the potential of V_{LCD} and GND by the frequency of the frame 125Hz.

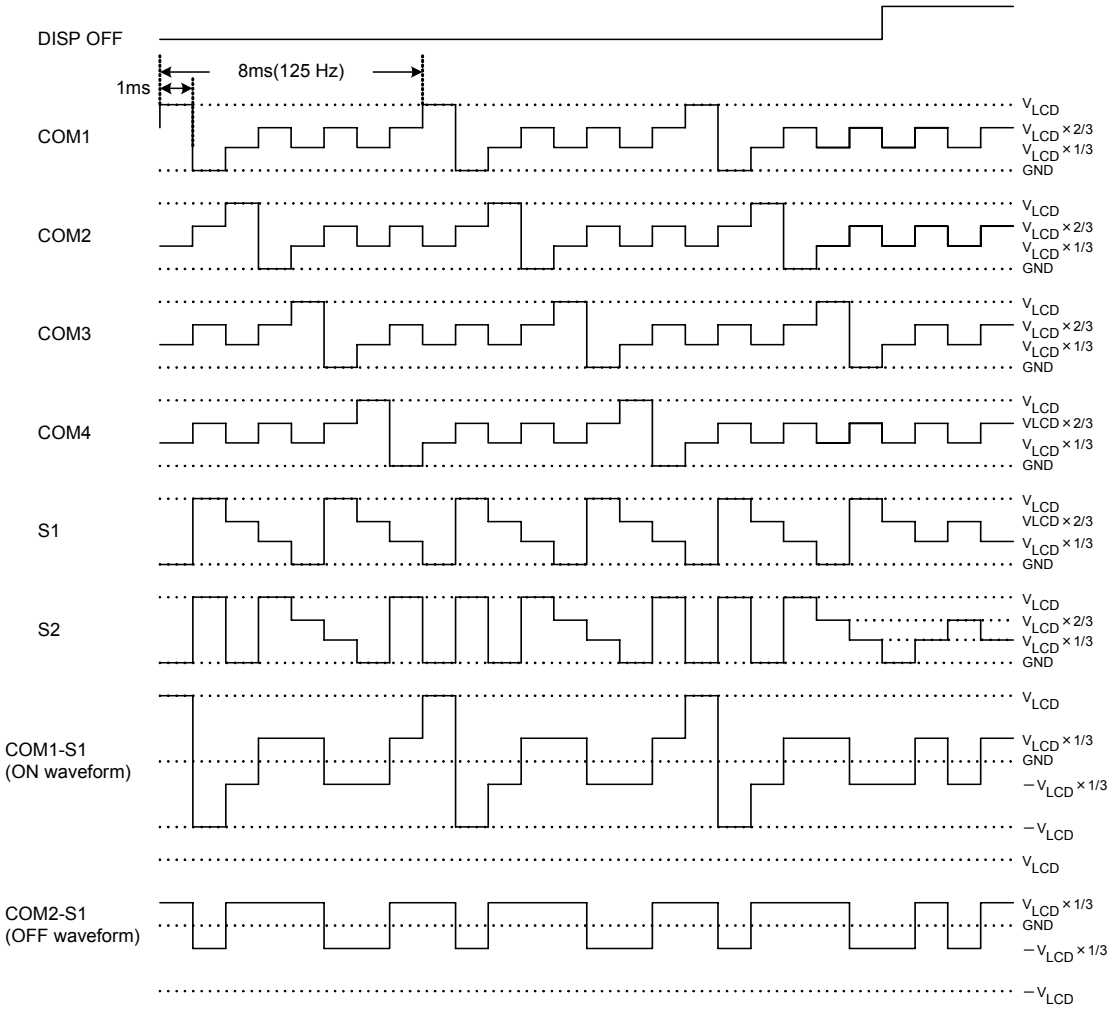


The example of segment data

Segment data (ϕ L13, ϕ L14)

	Y1	Y2	Y4	Y8
0 (S1)	COM1	COM2	COM3	COM4
	1	0	1	0
1 (S2)	COM1	COM2	COM3	COM4
	1	1	0	1

Data select (ϕ L/K1A)



Note: when "1" is set to the DISP OFF bit, the non-selection wave form is outputted from the common and segment output.

Note: All common outputs and segment outputs are fixed to the "L" level between 100ms the time of clock stop mode and after clock stop mode release.

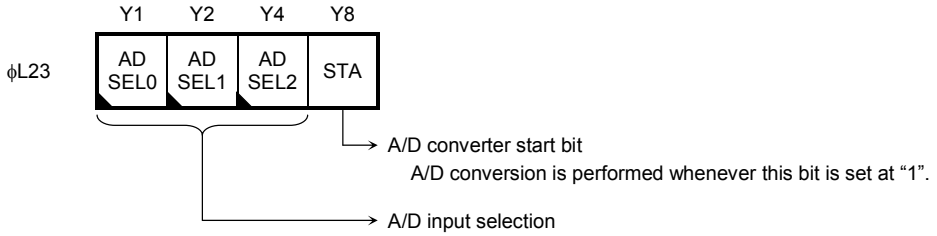
Note: When 1/3 bias is set, the frame frequency becomes twice at 1/2 bias.

Note: When 1/3 bias is set, Current consumption increases about about 100μA compared with 1/2 bias.

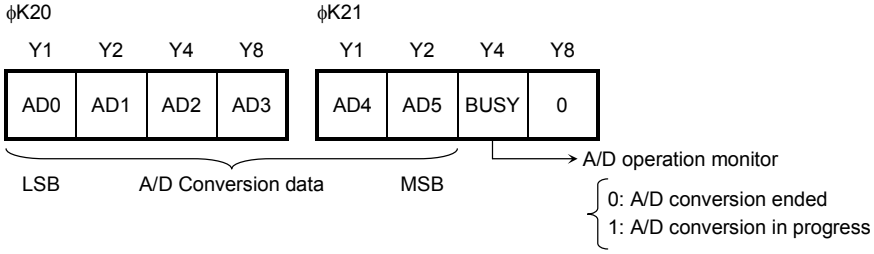
○ A/D Converter

The A/D converter is used for measuring the strength of electric fields, the voltage of batteries and key input that uses ladder resistance with 4-channel 6-bit resolution

1. A/D Converter Control Port and Data Port



SEL2	SEL1	SEL0	ADINPUT
0	0	0	ADin1
0	0	1	ADin2
0	1	0	ADin3
0	1	1	ADin4
1	*	*	$V_{reg}/2$



A/D converter is the serial comparison systems of 6 bit decomposition ability.

The standard voltage of A/D conversion is an internal power supply (V_{DD}). The voltage which divided this power supply into 64 and A/D input voltage is compared, and data is outputted to A/D conversion data port. A/D conversion input follows multiplex method for the 4-external input pins (A/Din1 to A/Din4 pin) and the 1/2 potential of Vreg pin voltage, and selected by A/D SEL0 to A/D SEL2 bits.

The A/D converter performs A/D conversion whenever the STA bit is set at "1", and this is ended after six machine cycles (240 μs). A/D conversion completion is determined by referring the BUSY bit, and the A/D conversion data is loaded into the data memory after conversion has finished.

The result of A/D conversion is required for by the following calculation.

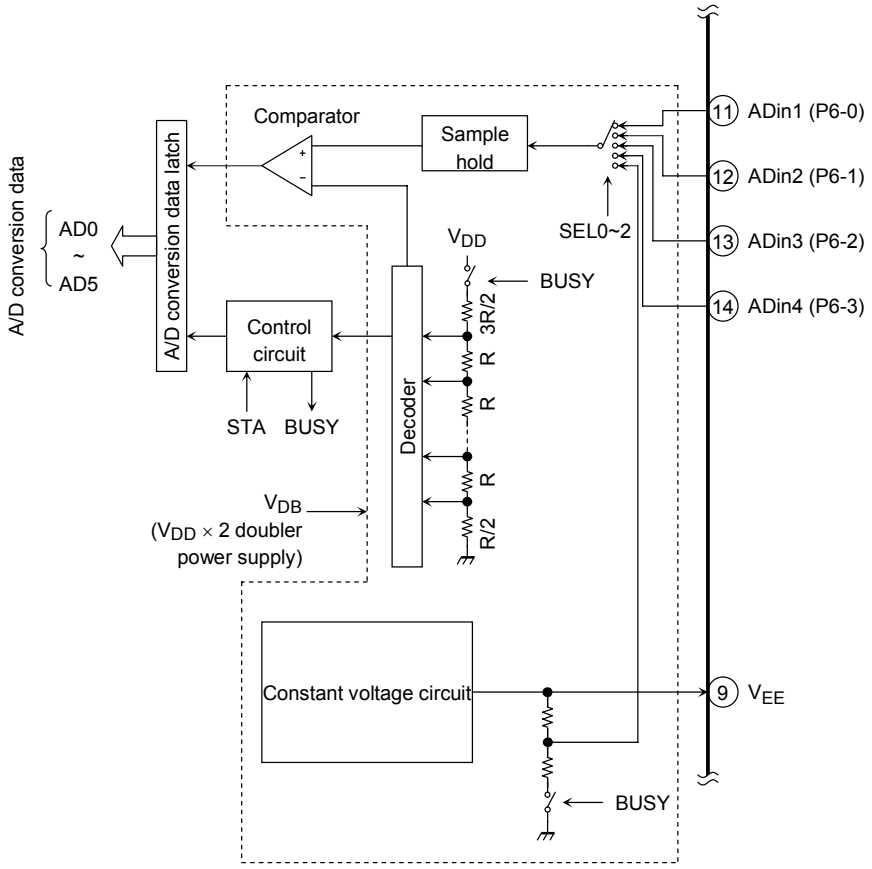
$$V_{DD} \times \frac{n - 0.5}{64} \quad (63 \geqq n \geqq 1) \quad \leqq \quad \text{A/D Input voltage} \quad \leqq V_{DD} \quad \frac{n + 0.5}{64} \quad (62 \geqq n \geqq 0)$$

(n is A/D conversion data value. [Decimal])

$V_{reg}/2$ to A/D input is used for battery detection. V_{reg} potential is 1.5 V and 1/2 potential: 0.75 V of V_{reg} pin voltage is chosen as A/D input and V_{DD} potential which is standard potential can be detected by carrying out A/D conversion of this potential. When V_{DD} potential is 1.5 V, A/D conversion data is set to 20H, and if A/D data goes up and V_{DD} potential serves as 0.75 V as V_{DD} potential falls, it will serve as 3FH.

These control are accessed with the OUT2/IN2 instruction for which [CN = 3H, 4H] has been specified in the operand.

2. A/D Converter Circuit Configuration



The A/D converter consists of a 6-bit D/A converter, sample hold, comparator, an A/D conversion latch and control circuit. Only when BUSY bit is "1", 6 bit D/A converter and a comparator part is in order to operate, no current consumption of A/D converter between A/D converters un-operating. 1/2 potential of V_{reg} constant voltage can choose as A/D input.

A/D converter part is driving using by doubler voltage V_{DB} (two times to V_{DD}).

Note: To the output data of I/O Port -6 (Nch open drain) corresponding to A/D input pin to use set up "1" and use it by changing into an input state.

Note: V_{EE} constant voltage potential is used as the drive voltage of the LCD driver, standard voltage of the object for CPU, the DC-DC converter and decrease voltage detection circuit for VT.

Note: The A/D input pin can impress the 0V to VDB pin level.

○ Programmable Counter

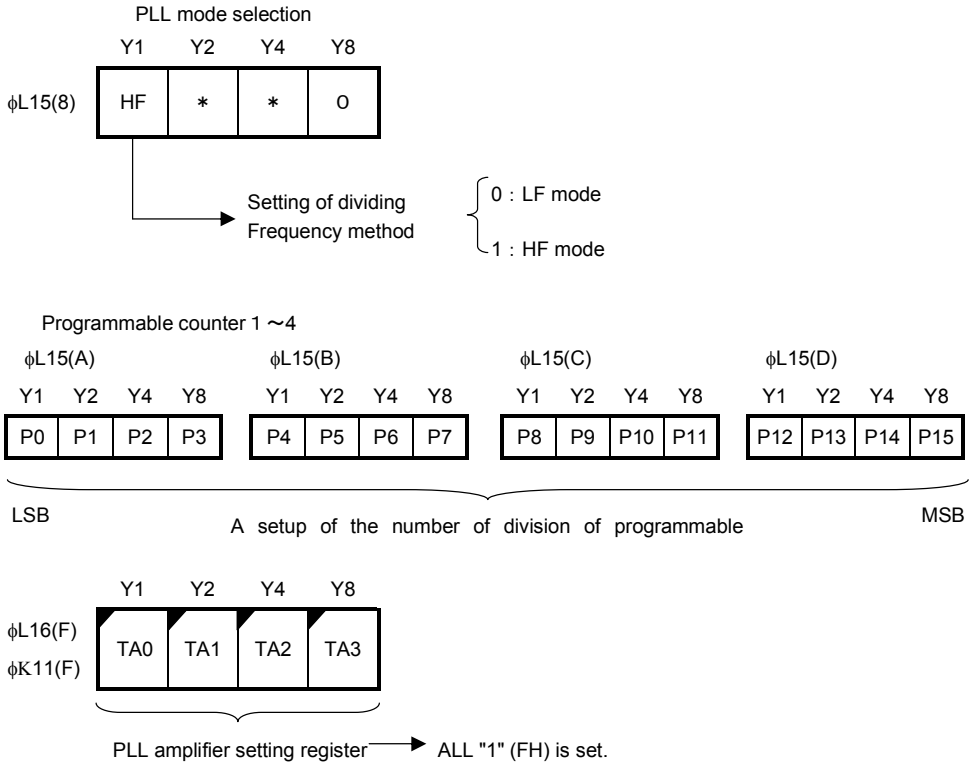
The programmable counter consists of two modulus Pre-scaller, 4-bit + 12 bit programmable counter and a port to control these elements. The programmable counter stops at PLL off mode operation, and operates at PLL on mode. The unnecessary radiation and current consumption can be decreased by the combination with the single-chip tuner with built-in 1/16 Pre-scaller .

The frequency divided with a programmable counter is input to the phase comparator, and the phase difference with a reference frequency is output from the phase comparator Moreover, the internal clock of a programmable counter can be used also for the phase difference detection of the DC-DC converter doubler clock and the phase comparator for VT.

(Refer to section in Reference frequency divider, DC-DC converter for VT, Phase comparator)

1. Programmable Counter Control Port

PLL mode select port sets the method of dividing frequency, and the programmable counter port sets the number of dividing frequency.



The setting of PLL mode select and the number of programmable counter dividing frequency is arranged in data port 6 selected in the select port. It is accessed by the OUT1 instruction that specifies [CN=5H] for the operand.

There are two kinds of methods of dividing frequency about the direct dividing frequency method (LF mode) and the Pulse swallow method (HF mode). Set it according to the frequency and the number of set dividing frequency used. The programmable counter becomes composition of 12 bits (P4 toP15) at the LF mode and 16 bits (P0 to P15) at the HF mode. The setting of the number of dividing frequency is set by writing it in MSB bit (φL15 (D)). When the MSB bit is set, all the data of P0 to P15 is updated. For this reason, even when changing a part, it is necessary to surely access and to set it at the end.

PLL input (OSCin) has the input amplifier. This amplifier gain is set by PLL amplifier setting register. Please set "1" (FH) to this register all.

Note : Please set "0" to the Y8 bit of PLL mode select port (φL15(8)).

Note : After the system is reset, all PLL amplifier setting registers are set in "1".

Note : In PLL amplifier setting registers, TA0 and the TA1 bit set the OSCin input amplifier, TA2, and the TA3 bit set the gain of the IFin input amplifier respectively.

2. Programmable Counter Divider Frequency Method, Gain Setting

Pulse swallow method and direct method of dividing frequency are selected by the HF bit. Set it according to the receiving frequency.

It combines with the single-chip tuner with built-in 1/16 or 1/8 pre-scaller and uses it. The local oscillator frequency of the tuner is input to the OSCin input at the MW/LW/SW band. The frequency in which 1/16 or 1/8 dividing the local oscillator frequency of the tuner is input to the OSCin input at the FM/TV band.

OSCin input has been fitted into the amplifier, and small amplitude possible. This input amplifier has register (ϕL16(F), ϕK11(F)) that A/Djusts the amplifier gain. Set "1" (FH) to this register all.

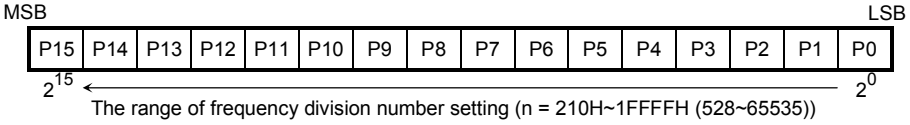
Mode	HF	Division Method	OSCin Operation Frequency Range	Example of Receiving Band	Division Range
LF	0	Direct division method	0.5~4 MHz	MW/LW	10HtoFFFH (16to4095)
HF	1	Pulse swallow method (1/15・16)	1~30 MHz	SW/FM/TV	210H～FFFFH (528to65535)

Note : A local oscillation input is common to each mode, and is altogether inputted into an OSCin pin.

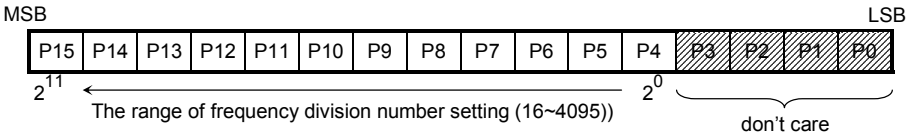
3. Frequency Division Number Setting

The frequency division number for the programmable counter is set in bits P0 to P15 in binary.

- Pulse swallow method (16 bit)



- Direct division method (12 bit)



Note : Set it to the value of dividing frequency in which the Priscara dividing frequency of the tuner is considered.

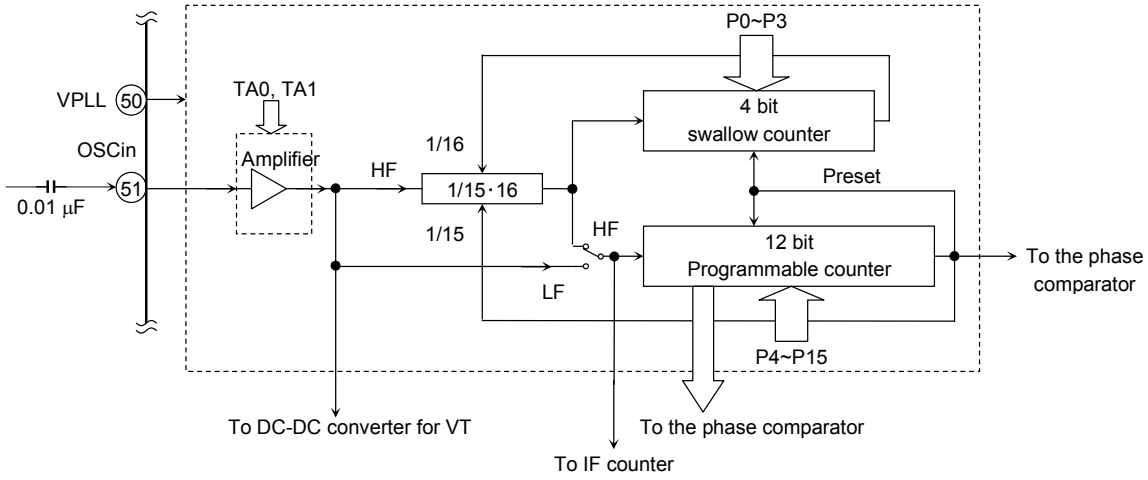
Note : The setting of the number of dividing frequency is set by writing it in MSB bit (ϕL15(D)).

4. Programmable Counter Circuit Configuration

This circuit consists of amplifier, two 1/15・16 modulus pre-scaller, the 4-bit swallow counter and a 12-bit binary programmable counter. In HF mode selection, 1/15・16 pre-scaller, 4 bit swallow counter and 12-bit binary programmable counter are used. In LF mode selection, only 12-bit binary programmable counter is used.

The OSCin input clock is supplied to the DC-DC converter for VT, and used as doubler clock. The clock divided with programmable counter is supplied to the phase comparator and the IF counter.

(Refer to section in DC-DC converter for VT, Phase comparator)



Note : The power supply of a programmable counter uses the V_{PLL} pin power supply. This power supply level can be supplied regardless of theV_{DD}/V_{CPU} pin power supply level. The V_{PLL} pin power supply can turn OFF at PLL off mode. The setting register power supply of a programmable counter uses the pin V_{CPU} power supply. Therefore, even if the pinV_{PLL} power supply is turned off, the contents of a register are held.

Note : OSCin pin has been fitted into the amplifier, and small amplitued possible by linking them to a condenser. OSCin input is high impedance when PLL is in the off mode.

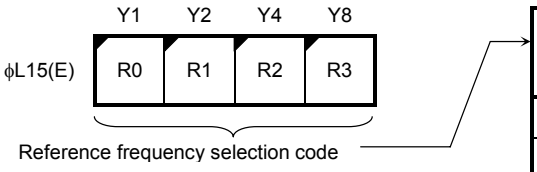
○ Reference Frequency Divider

The reference frequency divider divides the oscillation frequency of the external 75 kHz crystal and generates the following ten types of PLL reference frequency signals; 1kHz, 1.39kHz, 1,56kHz, 2.78kHz, 3kHz, 3.125kHz, 5kHz, 6.25kHz, 12.5kHz and 25 kHz. These signals are selected with reference port data.

The selected signal can be supplied as a reference frequency for the phase comparator as described below. Also, the PLL is switched on and off with the contents of the reference port.

1. Reference Port

The reference port is an internal port for selecting the ten reference frequency signals. This port is arranged in data port 6 selected in the select port. This port is accessed with the OUT1 instruction for which [CN = 5H] has been specified in the operand. When the content of the reference port is all "1", programmable counter, the IF counter, the reference counter, and the phase comparator stop and become PLL off modes. As the frequency division setting data for the programmable counter is updated when the reference port is set, it is necessary to set the frequency division number of the programmable counter prior to setting the reference port.



R3	R2	R1	R0		Reference Frequency
0	0	0	0	0	1 kHz
0	0	0	1	1	1.3889kHz
0	0	1	0	2	1.5625kHz
0	0	1	1	3	2.7778kHz
0	1	0	0	4	3 kHz
0	1	0	1	5	3.125 kHz
0	1	1	0	6	5 kHz
0	1	1	1	7	6.25 kHz
1	0	0	0	8	12.5 kHz
1	0	0	1	9	25 kHz
1	0	1	0	A	Prohibition
1	0	1	1	B	Prohibition
1	1	0	0	C	Prohibition
1	1	0	1	D	Prohibition
1	1	1	0	E	Prohibition
1	1	1	1	F	PLL off mode

Note : After resetting the system, this port is set to "1" and becomes PLL off mode.

Note : When the $\overline{\text{INH}}$ pin input enable setting is done by the $\overline{\text{INH}}$ ENA bit, PLL off mode is controlled by $\overline{\text{INH}}$ input and above-mentioned PLL off mode.

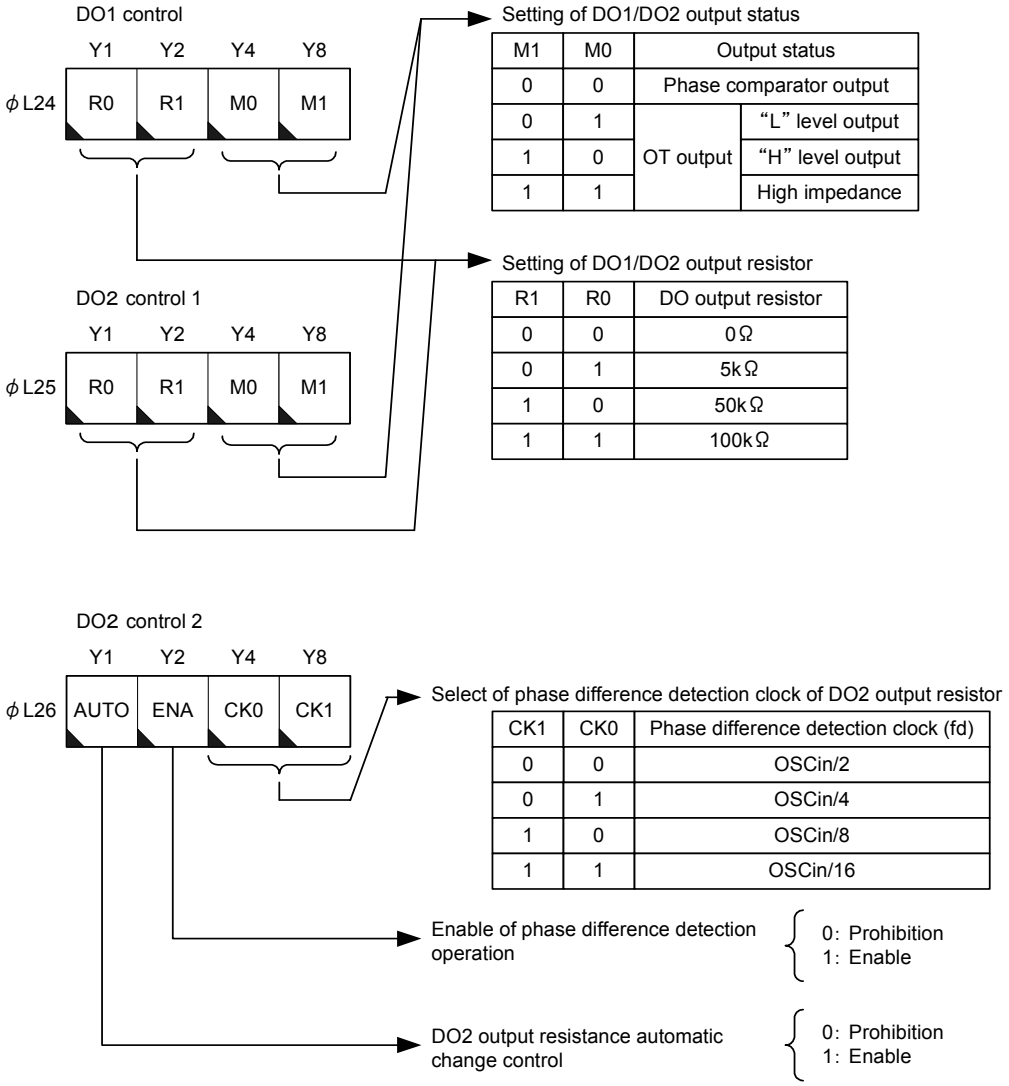
○ Phase Comparator and Lock Detection Port

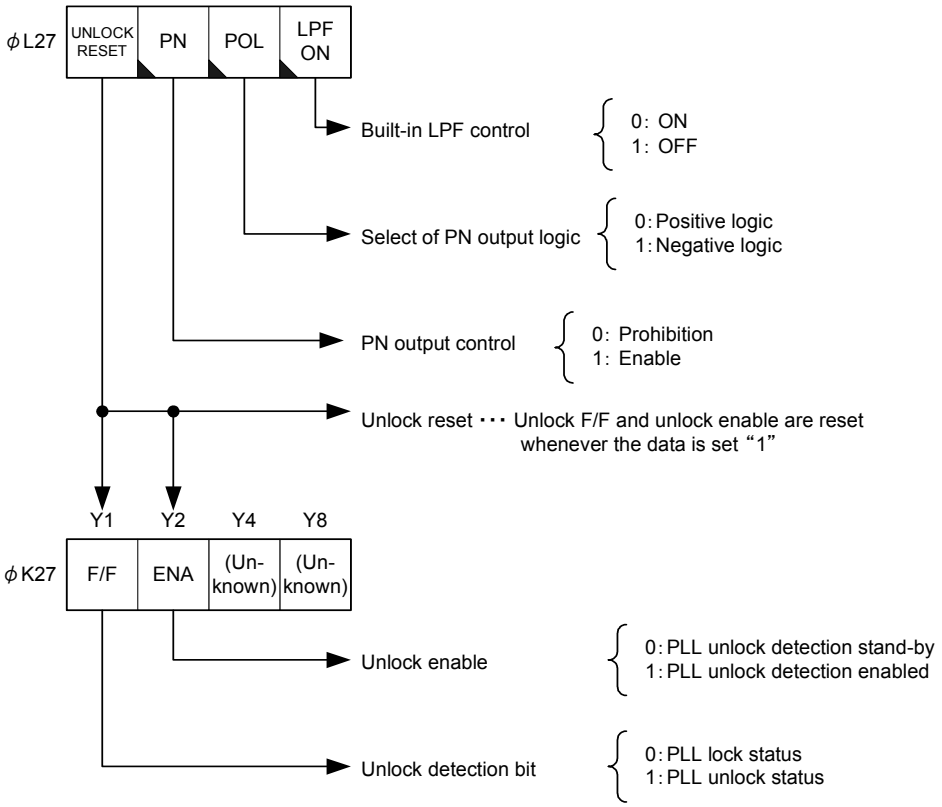
The phase comparator compares the difference in phasing between the reference frequency signal supplied from the reference frequency divider and frequency division output of the programmable counter and outputs the result. If then controls the VCO (Voltage control oscillator) via a low pass filter in order to ensure that the two frequency signals and the phase difference match.

It has two phase comparator pins and they contain the output resistance which can be set up individually in each pin. Three kinds of setup of 5/50/100kohm can perform this resistor. Furthermore, it has the automatic change which detects phase difference, the N channel transistor for LFP amplifier of 5.5 V resisting pressure and external charge pump output mode.

The phase comparator and the charge pump output use DC-DC converter power supply (V_{DB}: V_{DD}×2) for CPU. Phase comparator output pin (DO1/2) can be used with the DO control port as a general-purpose output port.

1. Phase Comparator (DO) Control Port and Unlock Detection Port





Note : The Y4/Y8 bit of unlock port (ϕK27) becomes unfixed.

The phase comparator control port and Unlock Detection Port are accessed by the OUT2 instruction which specified [CN=4H, 5H, 6H, 7H] to be operand parts, and the IN2 instruction which specified [CN=7H] to be an operand part. After the system is reset, these control bits are reset in "0".

● Setting of output mode (M0. M1 bit)

M0 and the M1 bit set the phase comparator output status (DO1/2 output pin). These bits can set the "H"/"L" level and high impedance (HZ) status.

Note : If it is set as PLL off-mode, "HZ" level is held at the phase comparator output status and When"H"/"L" level is set, "H"/"L" level is held.

Note : The PN output mode is given to priority when setting it to "PN =1 ".

● Setting of output resistor (R0, R1 bit)

R0 and R1 bit set the output resistance of the phase comparator output to DO1 and DO2 pin individually.

Note: The output resistance is set regardless of output mode (M0,M1) or the PN output mode. For this reason, when it set as the H"/"L" level or PN output mode, set "0" to these bits.

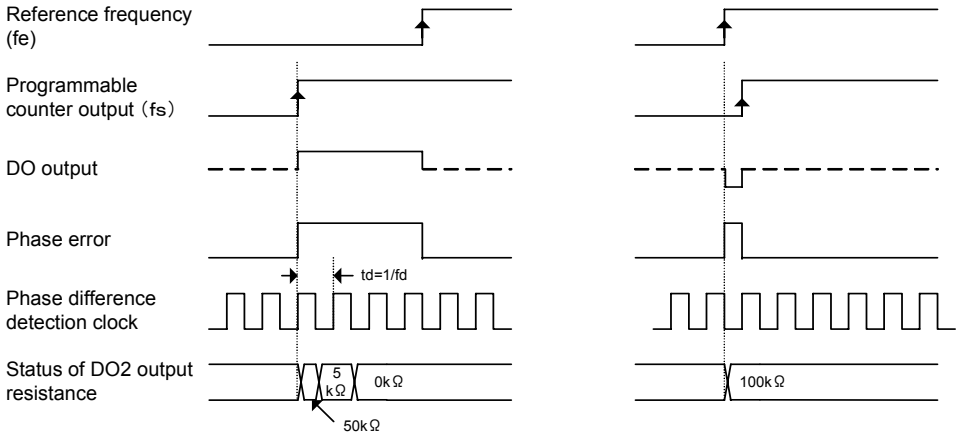
Note: When the pin DO2 is set to the phase difference automatic switch mode, the R0/R1 bit of DO2 control 1 becomes don 't care.

● Phase difference automatic switch mode (DO2 control 2 port: AUTO, ENA, CK0, CK1 bit)

The pin DO2 has the phase difference automatic switch mode that automatically switches the output resistance according to the phase difference. In this mode, when the phase difference pulse is short, the output resistance is enlarged and the output resistance is reduced as the phase difference pulse becomes long. That is, it operates by the low resistance when becoming high resistance in the state of the lock, and entering the state of unlock. Thus, the Lock-Up time can be improved by using this mode.

The phase difference detection operation is enabled when "1" is set to the ENA bit and the DO2 output resistance switch is performed when "1" is set to the AUTO bit.

Detection of phase difference is performed using the clock of operation from the programmable counter circuit. The unlock status is counted to the binary with this clock. This clock can select four kinds, 1/2, 1/4, 1/8, and 1/16 of the OSCin input. The output resistance setting time can be switched by switching the clock. This control selects the clock frequency by CK0 and the CK1 bit. Select the clock frequency according to the Lock-Up time. If necessary, turn off an automatic change after it locks, and change the output resistance to the fixed setting (R0 and R1 bit).



< The example of timing 1 > < The example of timing 2 >

Output resistance	Phase difference resistance period	
	fr＜fs (Example - 1)	fr＞fs (Example - 2)
100kΩ	—	0～td/2
50kΩ	0～0.5×td	0～1.5×td
5kΩ	0.5×td～td	td～2.5×td
0kΩ	td～2×td	2×td～2.5×td

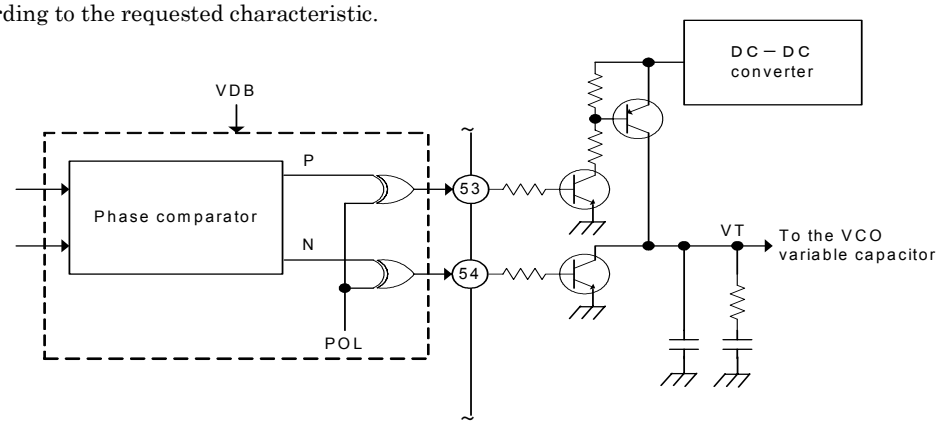
CK1	CK0	Phase difference detection clock (fd)
0	0	OSCin/2
0	1	OSCin/4
1	0	OSCin/8
1	1	OSCin/16

Note: The PN output mode is given to priority when setting it to " PN =1".

Note: When the DO2 output mode setting is only the phase comparator output, it becomes effective.

● PN output mode (PN, POL bit)

It has PN output mode using the external charge pump. The DO1/2 pin changes into P output and N output pin respectively if it sets it to this mode. Moreover, P/N output logic can be reversed by the POL bit. The following is an example of an external charge pump use circuit. Constitute the circuit according to the requested characteristic.



The example of external charge pump use circuit (PN="1")

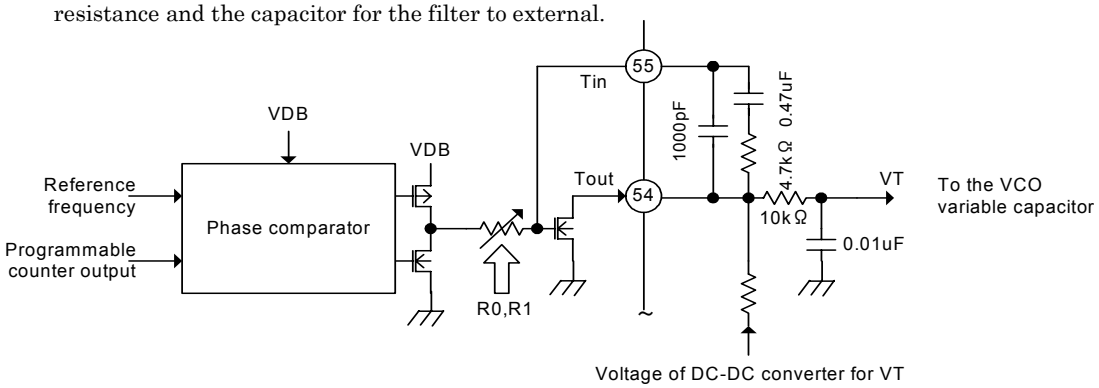
Note: Set "0" to POL bit excluding the PN output mode setting.

Note: When PN output mode is set, it is output by CMOS output. As for "H" level, the VDB pin level is output.

● Built-in LPF amplifier (LPF ON bit)

The N channel FET transistor for LPF is built in. The resisting pressure of this transistor is 5.5V. VCO (voltage control oscillator) which can carry out variable of the range of VT to 0~5.5V can be constituted using this transistor.

If "1" is set as the LPF ON bit, Built-in LPF will be in ON status, DO2 pin changes to the FET gate input (Tin), and P9-1 pin changes to the FET drain pin (Tout), respectively. The DO phase comparator output is connected with the FET gate pin, and LPF can be composed only of the connection of resistance and the capacitor for the filter to external.



Configuration of built-in low-pass filter amplifier (LPF ON ="1" setting)

Note: When building LPF into is used, the DO2 output mode, the resistance setting and the phase difference automatic switch mode can be used.

Note: The Tout output is 5.5V resisting pressure. Do not use this voltage exceed it.

Note: Set the resistance set with R0 and R1 according to the requested characteristic.

Note: The filter circuits illustrated in the above diagrams are for reference purposes only. It is necessary to examine the system band configration and characteristic and design actual circuits in accordance with requirements.

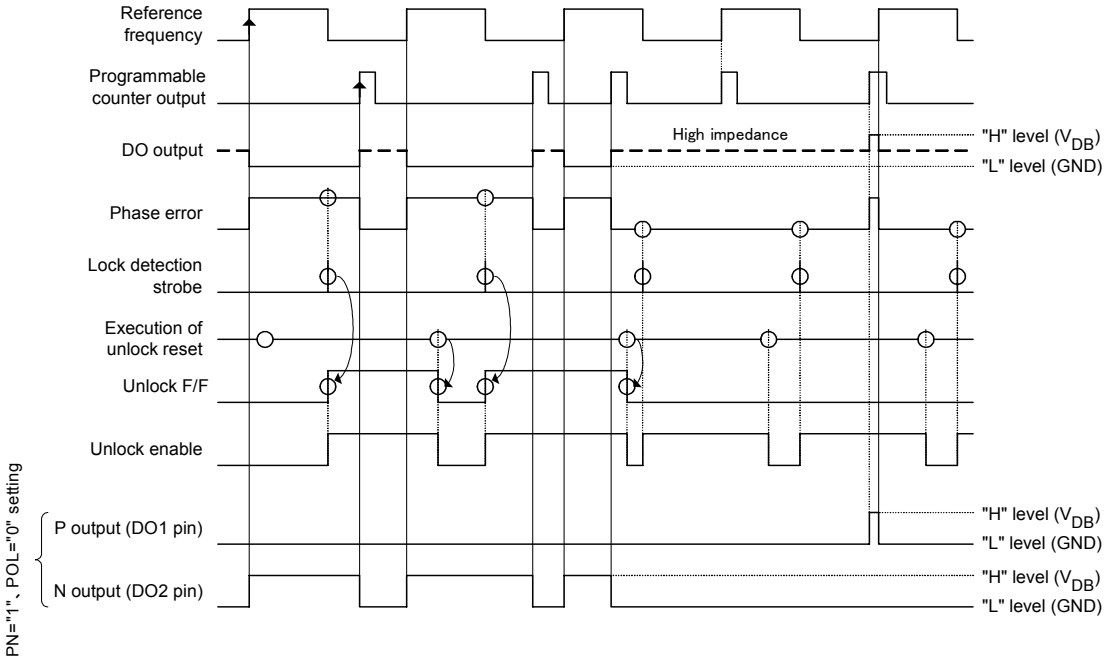
Note: The Tout pin is used also P9-0 pin. It becomes invalid the P9-0 output data at the time of built-in LPF use.

● Unlock detection port (UNLOCK RESET, UNLOCK F/F, ENA bit)

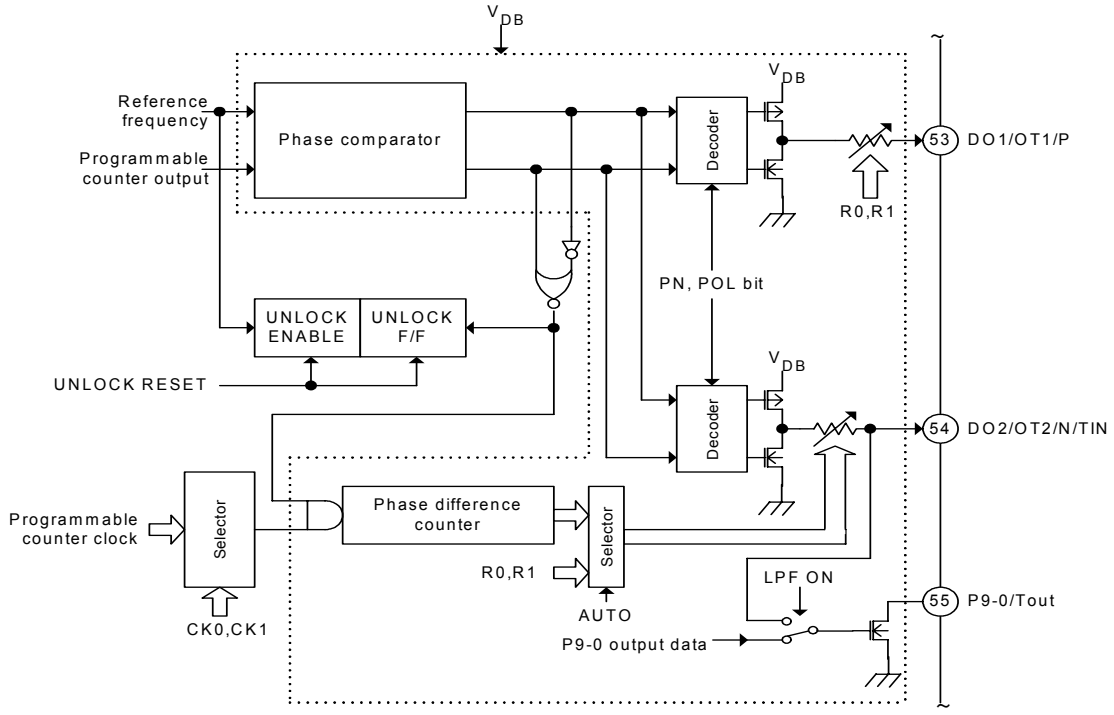
Unlock F/F detects the phase difference of a programmable counter division output and reference frequency to the timing from which about 180 degrees of phases shifted. When a phase does not suit at this time (that is unlock status), unlock F/F is set. The unlock F/F status is reset whenever the UNLOCK RESET bit is set as "1".

It is necessary to access to UNLOCK F/F after establishing more time than is required for the reference frequency cycle after the unlock F/F has been reset in order to detect the phase difference with the reference frequency cycle. It is for this purpose that the enable bit has been made available, but the unlock F/F must not be accessed until after it has been confirmed that the unlock enable has been set at "1".

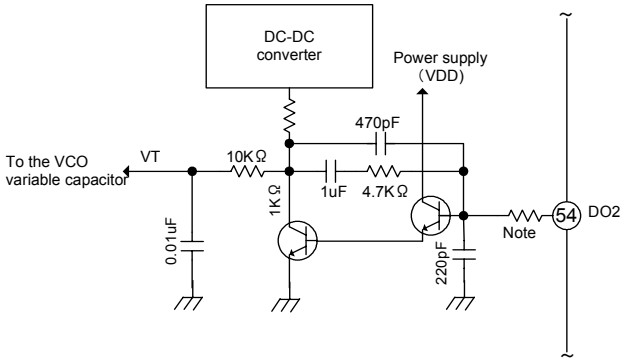
2. Phase Comparator, Unlock Port Timing



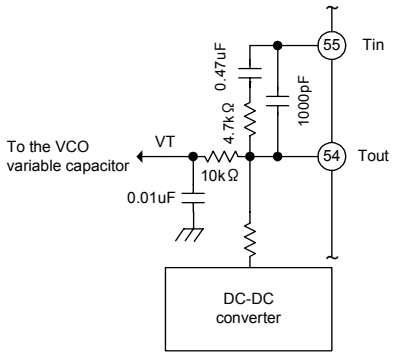
3. Phase Comparator, the Unlock Port Circuit Configuration



Note: The phase comparator circuit block uses the V_{DB} power supply. Therefore, the V_{DB} power supply level is output as for "H" level of phase comparator output pin (DO).



<Example of external low pass filter amplifier circuit >



<Example of built-in low pass filter amplifier circuit>

Note: A/Dd the output resistance if necessary though resistance is built into as for the phase comparator pn.

Note: Also refer to the DC-DC converter item for VT for the DC-DC converter. In A/Ddition, when the inside doubler transistor of DDCK1 is used for DC-DC converter voltage, design the tuner circuit so that the variable range of tuning voltage (VT) becomes large.

Note: Phase comparator output (DO1/2) becomes "HZ" at PLL off mode. The potential of the base of external LPF becomes unfixed when external low-pass filter (LPF) is used, and current consumption increases from power supply (VDD) through the transistor. Therefore, make phase comparator output (DO1/2) "L" level output at times and fix an off tuner (PLL off mode).

Note: The filter circuits illustrated in the above diagrams are for reference purposes only. It is necessary to examine the system band configration and characteristic and design actual circuits in accordance with requirements.

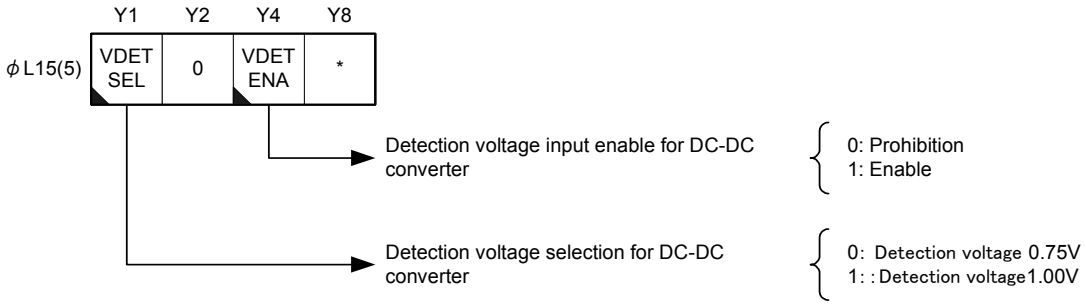
○ DC-DC converter for VT

The DC-DC converter is built into for the low-pass filter of PLL.

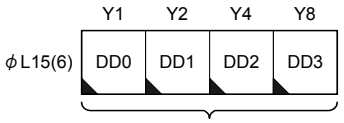
The DC-DC converter performs doubler using induced electromotive force of a coil. There are two kinds of pressure methods (the method of using the built-in N-channel transistor and the method of using an external transistor), and it selects it in proportion to the doubler voltage. Moreover, it has VT clamp function so that a certain voltage more than constancy certain is not impressed. The decrease of current consumption and this product can be protected by using the clamping function.

1. DC-DC converter for VT Control Port

DC-DC converter for VT control 1



DC-DC converter for VT control 2

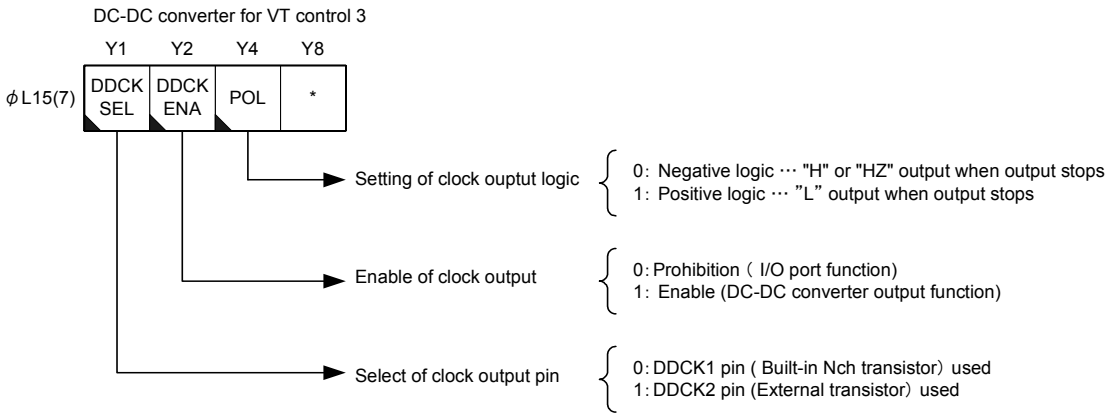


Select of clock output frequency for DC-DC converter

DD3	DD2	DD1	DD0		Output frequency	Note
0	0	0	0	0	Clock stopped	POL=0→DDCK output "L", POL=1→DDCK output "H" or " HZ"
0	0	0	1	1	PCTRin	The external clock can be used from the P3-3/PCTRin pin input. Note
0	0	1	0	2	75kHz	75kHz low speed oscillator clock
0	0	1	1	3	fosc/2	Programmable counter clock Note: fosc is OSCin input clock frequency.
0	1	0	0	4	fosc/4	
0	1	0	1	5	fosc/8	
0	1	1	0	6	fosc/16	
0	1	1	1	7	fosc/32	
1	0	0	0	8	fXT2	High-speed oscillator clock Note:Enable the high-speed oscillator at the time of using thehigh-speed oscillator.
1	0	0	1	9	fXT2/2	
1	0	1	0	A	fXT2/4	
1	0	1	1	B	fosc/3 注	Programmable counter clock Note: The ratio at "H" or "HZ" level and "L" level is 2:1 in the duty of fosc/3 at "POL =0". It reverses at "POL =1". Note: fosc is OSCin input clock frequency.
1	1	0	0	C	fosc/6	
1	1	0	1	D	fosc/12	
1	1	1	0	E	fosc/24	
1	1	1	1	F	fosc/48	

Note: Clocks other than the fosc/3 clock are all the duty 50%.

Note: At the time of using PCTRin input clock, put the pulse counter function into the enable status.



The DC-DC converter for VT outputs the doubler clock from DDCK1 (pin P8-1 and use combined) or DDCK2 (pin P9-2 and use combined). The doubler operation permission is done when setting it to the DDCK ENA bit "1" and the use pin is selected by the DDCK SEL bit.

The doubler voltage has the clamping function that becomes below certain constant voltage. Clamping is controlled with doubler detection voltage pin VDET (P8-1 pin and use combined). Potential in which the doubler voltage is resisting divided is input to the VDET pin. The doubler clock operates when the potential of the VDET pin becomes 0.75V or1.00V or less. The doubler voltage stops when becoming potential more than this. Detection voltage can select 0.75V and 1.00V, the detection operation is permitted when setting it to the VDET ENA bit "1".

A doubler clock can select 15 kinds of douler clocks. Select the frequency with a little influence of the beat etc. of the tuner.

The DC-DC converter control port for VT is arranged in data port 5, and accessed by the OUT1 instruction that specifies [CN=4H] for the operand part. These control bits are reset by "0" after system reset.

Note: Set "0" to the Y2 bit of DC-DC converter control 1(φL15(5)) for VT.

Note: When setting it to doubler clock pin (DDCK1/2) and doubler detection voltage input (VDET), the I/O port output data and the I/O control data of the pin of using combinedly become don 't care.

Note: The DC-DC converter detection voltage input permission (VDET ENA bit) put this bit into the prohibition status ("0") for PLL off mode or unused. It causes a current consumption increase.

2. DC- DC Converter for VT Setting

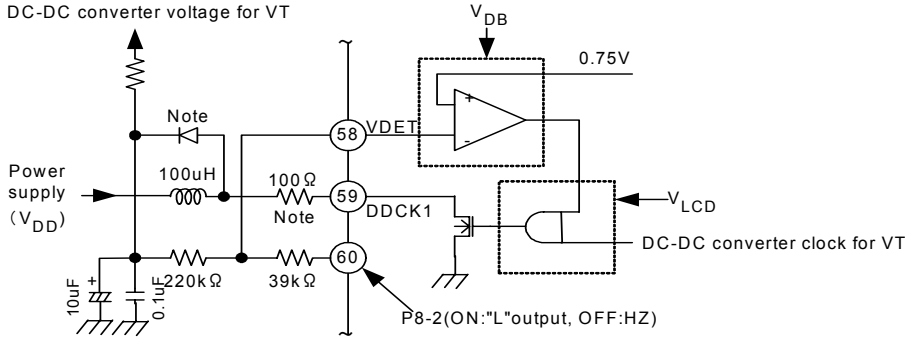
(1) DDCK1 Example of use of the built-in doubler transistor

DDCK1 pin has the Nch transistor for DC-DC converters, and can drive a direct coil. The resisting pressure voltage of this transistor is 6V, and it cannot doubler more than this. Usually, it controls by using the doubler clamping function so as not to become more than this resisting pressure. Please set POL bit to "0" at the time of using DDCK1 pin.

The following are examples of the DC-DC converter circuit that use the DDCK1 pin.

The generation pulse of the coil supplies and doublers through the diode by the clock output of the DDCK1 pin. And, this doublered voltage is supplied to the low-pass filter as a doubler voltage for VT.

In the example of the following, the P8-2 pin of 60 pins controls on/off of the division resistance. When the doubler is on, "L" level of the I/O port is output by the program and the resistance division is on status. When the doubler is off, the I/O port is set to "HZ" (input setting) and the resistance division is separated. It doesn't control like this, and the GND connection is not cared about instead of 60 pin connection. However, if GND connection is made, current will always consume through the coil and division resistance from the VDD power supply at the time of doubler OFF. Thus, this control prevents the current from consuming it by the doubler system circuit at the time of doubler OFF. Make such the control GND connection for unnecessary at the case where the power supply which is turned off is used at the time of tuner-off and the time of this system that is no problem even if it increases by consumption current.



Example of built-in DC-DC transistor doubler circuit

Note: The above-mentioned diode should use the Schottky diode of low VF.

Recommended diode: 1SS357

Note: Decide the coil constant for doubler according to the DC-DC converter clock frequency and the doubler current ability.

Note: Please connect the output resistance 100Ω of the above-mentioned DDCK1 pin if necessary when you influence the tuner characteristic by the clock output.

Note: There is no problem even if the Zener diode of 5.5V or less is used as substitution of clamping circuit (VDET) use. The VDET and doubler on/off control pin becomes unnecessary by using the Zener diode.

Note: When the doubler voltage exceeds the stipulated voltage when the clamp circuit is used, it stops. If doubler voltage is supplied during the DC-DC converter voltage supply for VT more than regulation, doubler operates to intermittence and the influence on the tuner characteristic can be considered. Therefore, we will recommend the decision of the ability and the low-pass filter lo A/D constant of pressure that doesn't exceed the detection voltage while the tuner is operating.

Note: The gate signal of the Nch transistor buffer of the DDCK1 pin uses the V_{LCD} (3V) power supply. Therefore, even if the V_{DD} power supply decreases, ste A/Dy doubler operation is possible.

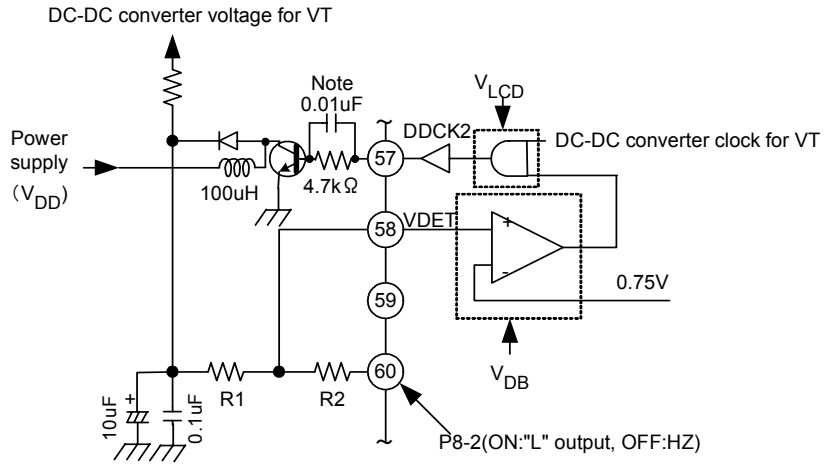
Note: In the above-mentioned use, design the tuner circuit so that the variable range of tuning voltage (VT) becomes wide.

Note: The filter circuits illustrated in the above diagrams are for reference purposes only. It is necessary to examine the system band configration and characteristic and design actual circuits in accordance with requirements.

(2) DDCK2 Example of use of the external doubler transistor

The DDCK2 pin is CMOS ftype and the DC-DC converter clock is output. The external transistor is used and it is doublered like DDCK1 pin. Since an external transistor is used, the doubler voltage can be set freely. Set the POL bit as "1" at the time of DDCK2 pin use.

The following are examples of the DC-DC converter circuit that use the DDCK2 pin. Please decide following R1/R2 resistance according to the requested doubler voltage. The P8-0 pin control is also similar to the DDCK1 pin.



Example of external DC-DC transistor pressure circuit

Note: Decide the coil constant for doubler according to the DC-DC converter clock frequency and the doubler current ability.

Note: There is no problem even if the Zener diode is used as substitution of clamping circuit (VDET) use. The VDET and doubler on/off control pin becomes unnecessary by using the Zener diode.

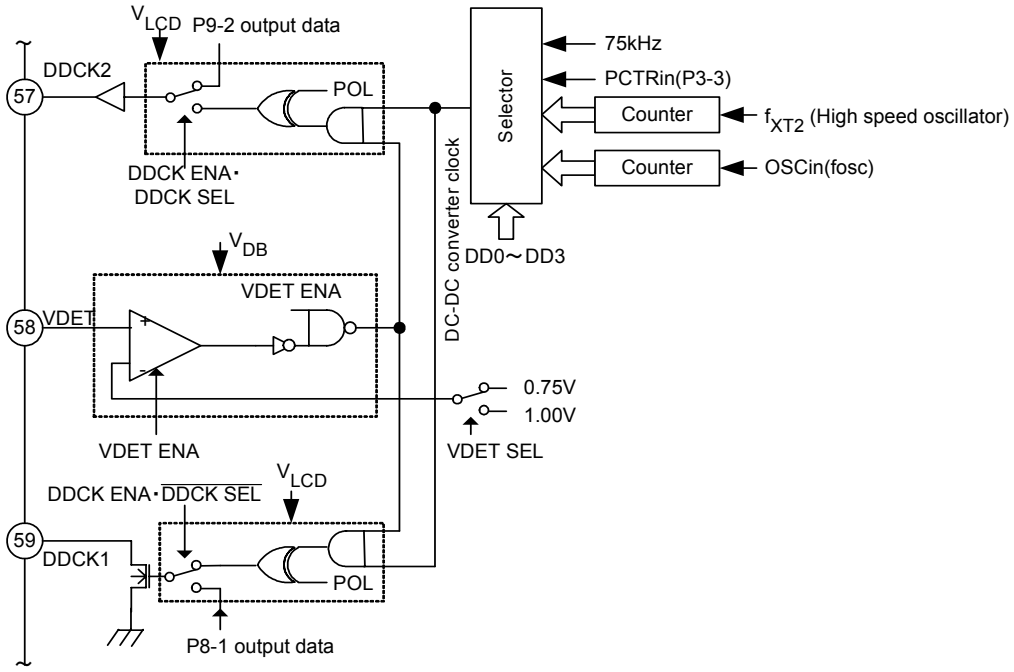
Note: Please A/Dd the charge improvement capacitor of the base input of an external transistor when the doubler ability is insufficient.

Note: Turn it off with the voltage of the DC-DC converter for VT decreased enough when off setting it with the P8-2 pin. Because a high voltage is impressed to the P8-2 pin, it causes destruction.

Note: The Pre-buffer power supply of the DDCK2 output pin uses the V_{LCD} (3V) pin power supply. Therefore, even if the V_{DD} power supply decreases, ste A/Dy pressure operation is possible. In A/Ddition, the "H" level of the DDCK2 pin outputs is outputted of the VDD power supply level.

Note: The filter circuits illustrated in the above diagrams are for reference purposes only. It is necessary to examine the system band configration and characteristic and design actual circuits in accordance with requirements.

3. DC-DC converter for VT configuration



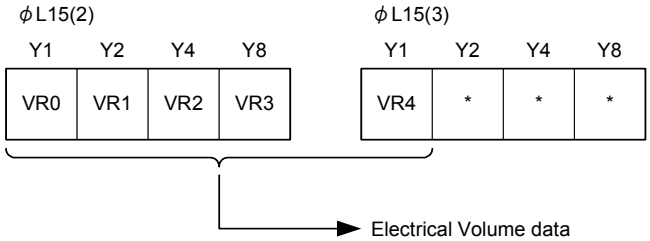
Note: The comparison voltage of pressure detection voltage (VDET) uses the V_{EE} constant voltage (1.5V) pin voltage in partial pressure.

○ Electrical Volume

The electronic volume of two-channel 32 steps (0 to 78dB, -∞dB) is built in. For this reason, electronic processing of headphone amplifier of volume regulation and part curtailment can be performed.

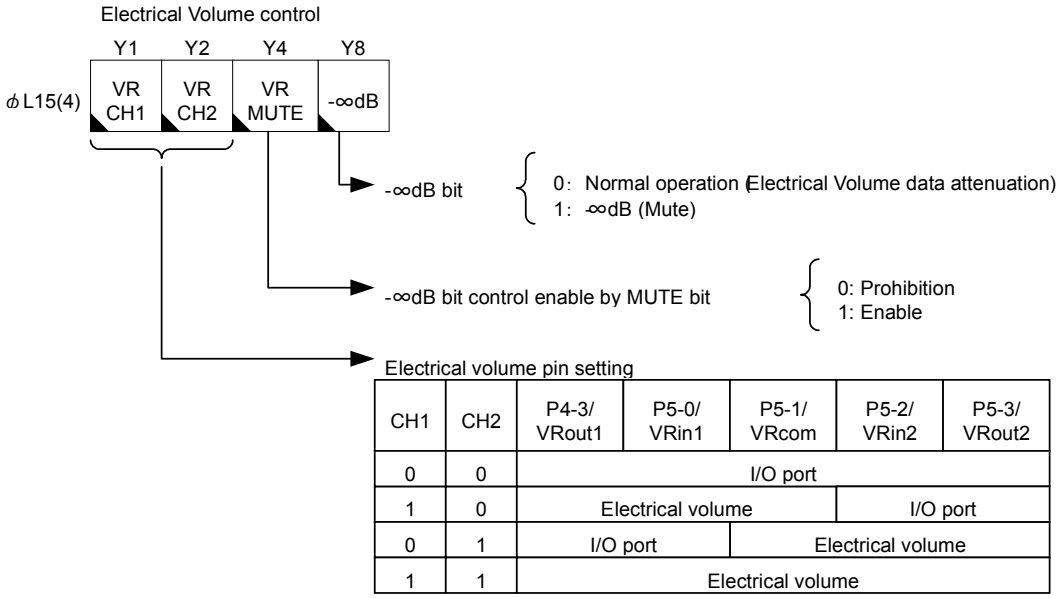
The pin for electronic volumes is making I/O Port 5 and I/O Port P4-3 pin serve a double purpose. The monaural stereo can correspond because it can switch one channel and two channels. In the attenuation level of an electronic volume, the range of -0 to -40db is -2db step, and -40 to78db is -4db step.

1. Electrical Volume Data Port and Control Port



Electrical Volume data

STEP	-∞dB	VR4	VR3	VR2	VR1	VR0	Attenuation level
1	1	*	*	*	*	*	-∞dB
	0	0	0	0	0	0	
2	0	0	0	0	0	1	-78dB
3	0	0	0	0	1	0	-74dB
4	0	0	0	0	1	1	-70dB
5	0	0	0	1	0	0	-66dB
6	0	0	0	1	0	1	-62dB
7	0	0	0	1	1	0	-58dB
8	0	0	0	1	1	1	-54dB
9	0	0	1	0	0	0	-50dB
10	0	0	1	0	0	1	-46dB
11	0	0	1	0	1	0	-42dB
12	0	0	1	0	1	1	-40dB
13	0	0	1	1	0	0	-38dB
14	0	0	1	1	0	1	-36dB
15	0	0	1	1	1	0	-34dB
16	0	0	1	1	1	1	-32dB
17	0	1	0	0	0	0	-30dB
18	0	1	0	0	0	1	-28dB
19	0	1	0	0	1	0	-26dB
20	0	1	0	0	1	1	-24dB
21	0	1	0	1	0	0	-22dB
22	0	1	0	1	0	1	-20dB
23	0	1	0	1	1	0	-18dB
24	0	1	0	1	1	1	-16dB
25	0	1	1	0	0	0	-14dB
26	0	1	1	0	0	1	-12dB
27	0	1	1	0	1	0	-10dB
28	0	1	1	0	1	1	-8dB
29	0	1	1	1	0	0	-6dB
30	0	1	1	1	0	1	-4dB
31	0	1	1	1	1	0	-2dB
32	0	1	1	1	1	1	-0dB



CH1	CH2	P4-3/ VRout1	P5-0/ VRin1	P5-1/ VRcom	P5-2/ VRin2	P5-3/ VRout2
0	0	I/O port				
1	0	Electrical volume			I/O port	
0	1	I/O port		Electrical volume		
1	1	Electrical volume				

Electronic volume is used combined with port 5 and port P4-3 pin.

It switches to the electronic volume pin by VR CH1 and the VR CH2 bit. If "1" is set to this bit, it becomes an electronic volume pin. An electronic volume has two channels. Channel 1(VR CH1 bit) and channel 2(VR CH2 bit) can respectively be individually set corresponding to VRout1/VRin1 pin and the VRout2/VRin2 pin.

The attenuation level of an electronic volume is set with the electronic volume data. The electronic volume data is five bits, and when the most significant bit is set, four subordinate position bits of the electronic volume data are updated. Therefore, the change only in the subordinate position should access the most significant bit.

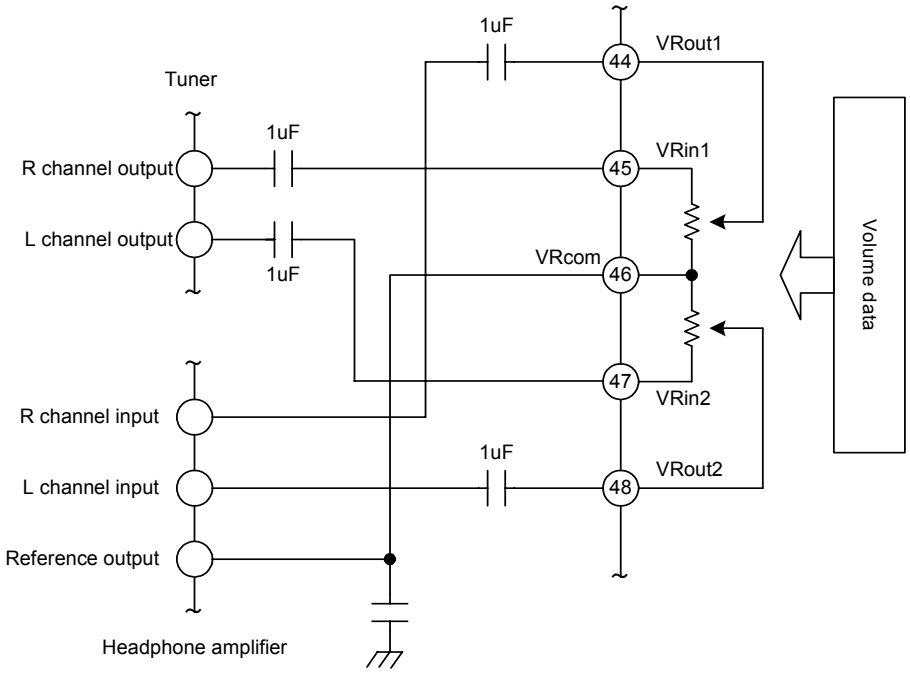
-∞dB bit can do the mute only by setting "1" to this bit. When it is set as -∞dB by this bit, electronic volume data is held, and if -∞dB is canceled again, it returns to the former attenuation level. The setting by -∞dB that sets all the electronic volume data to "0" and setting by -∞dB bit becomes the same operation.

Electronic volume can be set as -∞dB by input change of an I/O Port. The I/O port is change in the input that the break setting enable is done, and the MUTE bit is set to "1". When the MUTE bit becomes "1", it becomes mute (-∞dB). When the band switch etc. quickly does the mute, it uses it. When the VR MUTE bit is set to "1", this setting is enabled. In addition, since it is set up by the internal MUTE bit, it becomes effective even if it sets to MUTE/P9-1 pin as I/O Port. (Refer to section in MUTE output)

As for the electronic volume control port, it is arranged in data port 5, and the OUT1 instruction access which is specified [CN=4H] for the operand part is done. After the system is reset, the electronic volume control port is reset in "0".

2. Electronic Volume Configuration and Example of Circuit

An electronic volume is connected with the tuner and the headphone amplifier as follows and composed.



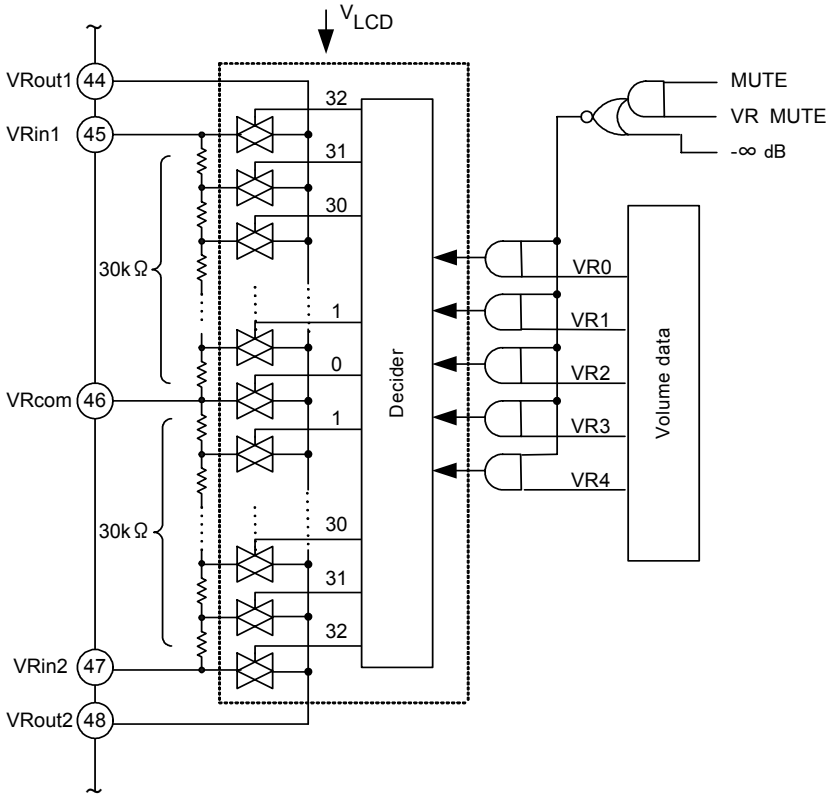
The example of IF counter auto mode operation timing

Electronic volume reference voltage (VRcom) is usually connected with the pin of the output of the reference of the headphone amplifier. When there is no reference output pin, connect this potential to GND level or V_{EE} pin (1.5V law voltage). However, when reference voltage (VRcom) is connected with GND, the distortion rate when input level (VRin) is 0.2Vp-p or less becomes 0.1% or less. It is necessary to note it because the distortion deteriorates when this input level is exceeded.

Note : The circuits illustrated in the above diagrams are for reference purposes only. It is necessary to examine the characteristic and design actual circuits in accordance with requirements.

3. Electronic Volume Configuration

Electronic volume consists of decoder analog switch, resistance, and control circuit. The V_{LCD} pin (3V) power supply is used for the power supply of decoder, analog switch and resistance part. Therefore, even if the pin V_{DD} power supply changes, steady operation is possible.



Note : The power supply of the analog circuit part of an electronic volume circuit part uses the $V_{LCD\ pin}$ (3V) power supply. Therefore, the range of the input of VRin1/2 is possible up to 3V. The power supply in the logic part uses theV_{CPU} pin power supply.

Note : The volume switch by zero crossing detection is not done. Therefore, when the attenuation level is switched, the Pots sound might be generated.

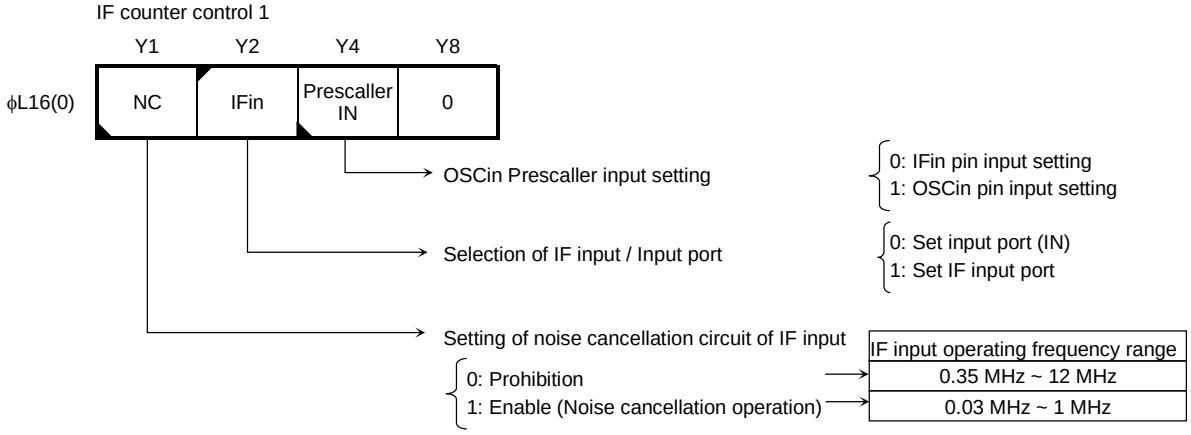
Note : The input total resistance of VRin1/2 is 30kΩ (Typ.).

Note : Distortion of the electronic volume is 0.05% (Typ.) and 0.1% (Max.) (VRin=0.4Vp-p is input).

○ IF Counter

The IF counter is 20-bit general-purpose IF counter that calculates Fm and AM intermediate frequencies (IF) during auto-tuning and can be used for detecting auto-stop signals, etc. VCO of an analog tuner is measured and detection of received frequency and detection of CR oscillation frequency can be performed.

1. IF Counter Control Port and Data Port



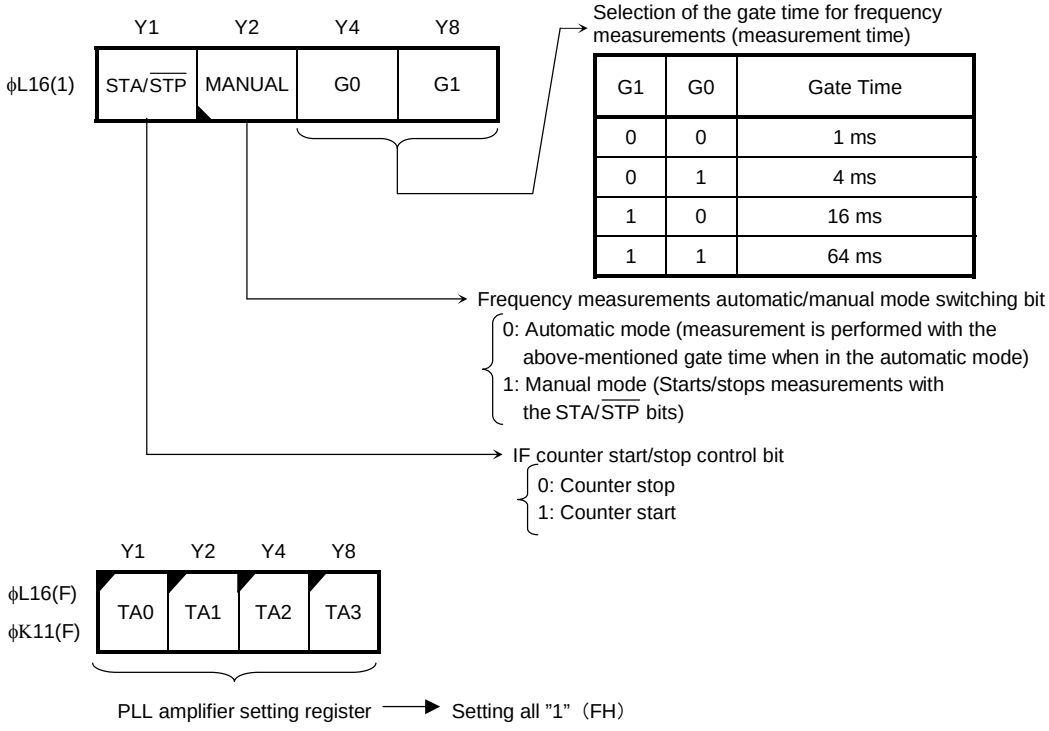
Note : At the time of an input port setup, the pin becomes CMOS input type and be able to detect frequency by IF counter.

Note : The IF input amplifier becomes off in PLL off mode when setting it to the IF input. Set to the input port when you use the IF counter in PLL off mode (CMOS input) and use it.

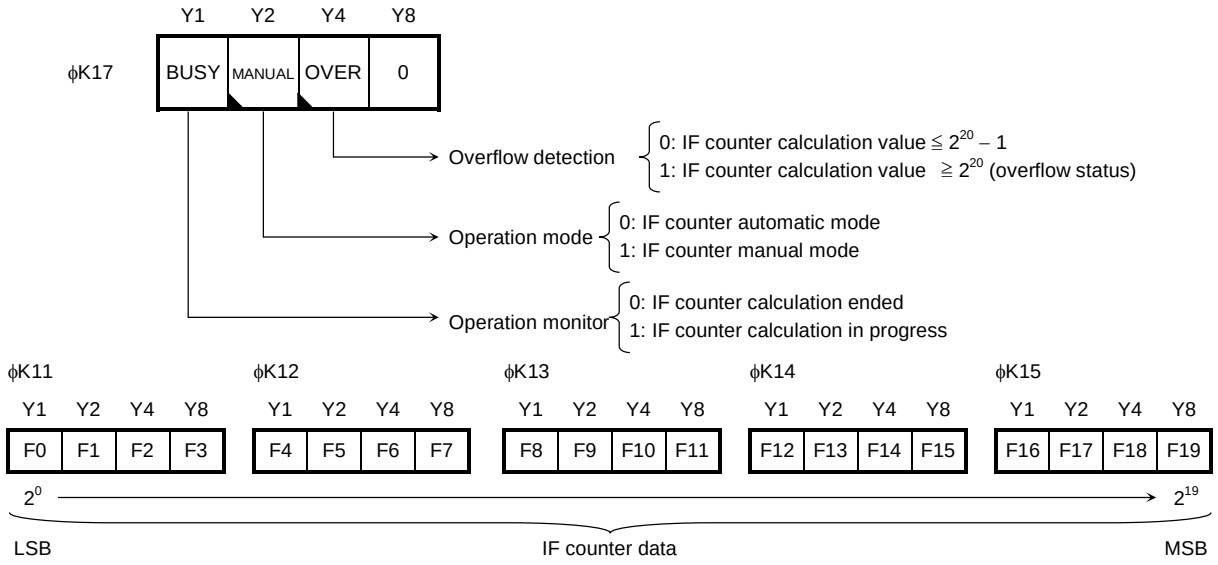
Note : when Pre-scaller input is set as IF counter input, 1/15・16 Pre-scaller is fixed to 16 dividing frequency and this frequency is inputted into IF counter at the time of a setup of a pulse swallow system.

Note :Refer to the programmable counter item for the range of the input frequency of the Pre-scaller input setting.

Note : Set "0" as Y8 bit of IF control 1 port (ϕ L16(0)).



Note : Among PLL amplifier setting registers, TA0 and the TA1 bit set the OSCin input amplifier, TA2 and the TA3 bit set the gain of the IFin input amplifier.



IF counter usually calculates of the IF signal from tuner, and detects auto stop signal. If "1" is set as IFin bit, IFin input amplifier operates and IF counter will be in an enable status. The gain of the input amplifier comes in variable by amplifier setting register port (ϕ L16(F), ϕ K11(F)). Set "1" to this register all. This amplifier becomes disabling at PLL off mode, and the IFin input becomes high impedance.

The range of the IF input frequency is different according to the NC bit. The internal noise cancellation circuit operates when "1" is set to the NC bit. The frequency range is set to 0.35 to12MHz when NC bit is "0." When NC bit is "1", noise cancellation circuit operates, and the frequency range is set to 0.03 to 1MHz. Set up according to IF frequency to detect.

There are two methods of IF counters of the calculation of IF counter auto mode and the IF counter manual mode. The calculation can be done by the following methods.

IF counter automatic mode

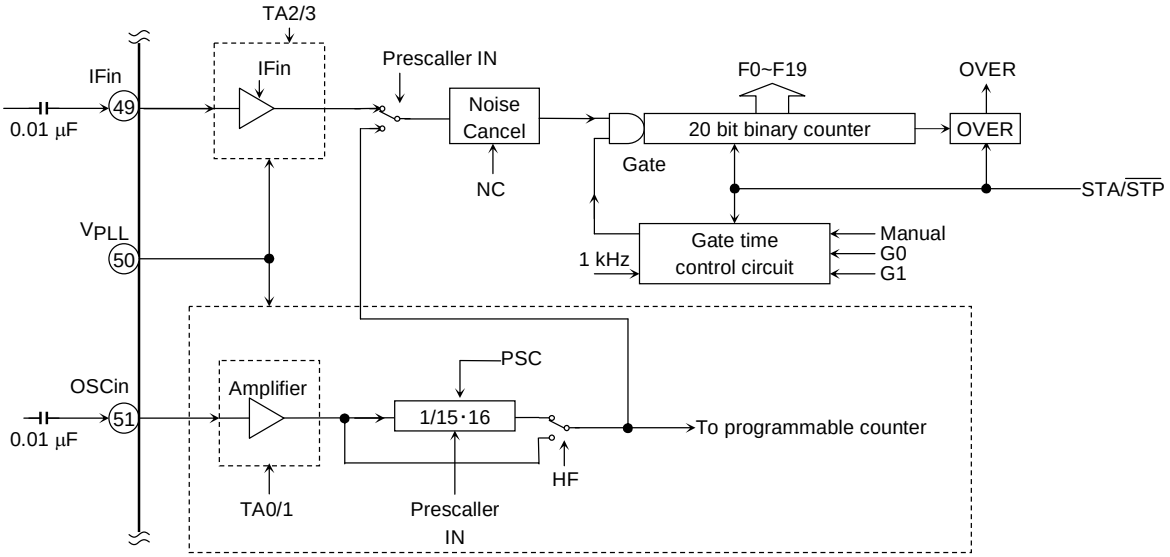
A setup in the auto mode of IF counter is set “0” to MANUAL bit and gate time is set up according to the frequency band to measure. If the STA/$\overline{\text{STP}}$ is set “1”, operation of IF counter will be started and the set-up clock in gate time will be inputted, and this number of input pulses is counted and it ends. An end of the calculation of IF counter can be judged by referring to BUSY bit. When more 2^{20} pulses are inputted for a total numerical value, OVER bit is set to “1”. BUSY bit and OVER bit are judged “0” and the frequency inputted can be measured by taking in IF data of F0 to F19.

IF counter manual mode

By internal time base (10 Hz etc.), it is used when gate time is controlled and it measures frequency. The manual mode is set “1” to MANUAL bit. At this time, a gate time setup serves as don't care. In STA/$\overline{\text{STP}}$ bit is set to “1”, it starts calculation. In STA/$\overline{\text{STP}}$ bit is set to “0”, it will end and calculation will take in data by the binary

1. IF Counter Circuit Configuration

The IF counter consists of the input amplifier, the gate time control circuit and the 12 + 8 bit binary counter. The clock of OSCin Pre-scaller and CR oscillation clock can be inputted as an IF counter

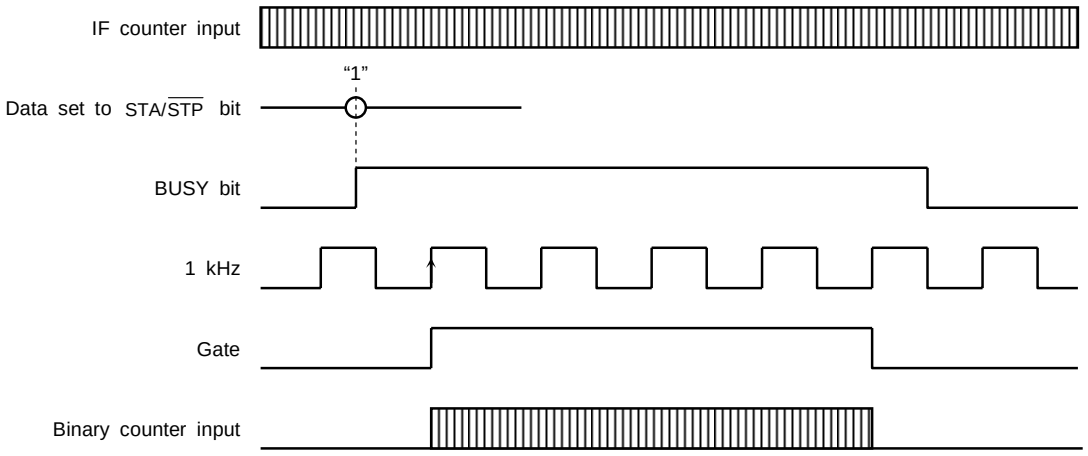


Note : All the binary counters of IF counter operate in a standup

Note : At the time of calculating of the OSCin Pre-scaller clock at IF counter, if PLL mode is set in the HF mode, 1 / 15-16 is fixed to 1 / 16 dividing frequency. Moreover, it is input directly in the LF mode.

Note : The VPLL pin power supply is used for the power supply of the input amplifier of IF counter, and OSCin input amplifier programmable counter part. This power supply level can be supplied regardless of the V_{DD}/V_{CPU} pin power supply level. Moreover, V_{PLL} pin power supply can turn OFF at the time of PLL off-mode. In A/Ddition, the power supply of the control register of IF counter or IF counter is using the V_{CPU} pin power supply. For this reason, the contents of register are held even if it turns off V_{PLL} pin power supply.

Note : IFin pin contains input amplifier and small-size width operation is possible. Moreover, IFin input becomes high impedance at PLL off mode.

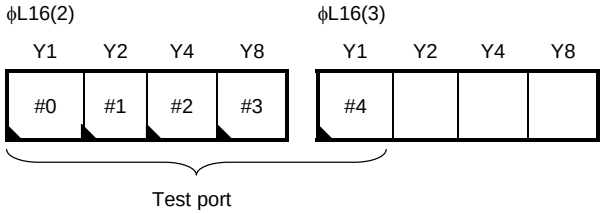


The example of IF counter auto mode operation timing

Note : IF counter uses the 1kHz clock. For this reason, it is delayed for a maximum of 1ms after executing a start instruction until a gate opens.

○ Test Port

It is an internal port to test the function of the device. These ports are arranged in data port 7 and accessed by the OUT1 instruction that specifies [CN = 6H] for the operand part. "0" is usually se with the program.



If the following data is set as test port from #3 to #0, various signals can be m A/De to output from MUTE pin.

#3	#2	#1	#0	Data	MUTE Pin output
0	0	0	0	0	MUTE output
0	0	0	1	1	Programmable counter frequency
0	0	1	0	2	Reference frequency
0	0	1	1	3	2 Hz
0	1	0	0	4	Prohibition
׀	׀	׀	׀	׀	
1	1	1	1	F	

Note : The MUTE pin is P9-1 pin and using combinedly. In case various signals are made to output from MUTE pin, it is necessary to set it as MUTE pin.

○ Application to an Emulator Tip

If pulse is inputted into TEST pin for $\overline{\text{RESET}}$ pin among the "L" level, operation of a device will serve as various test modes and the device operates as an emulator chip. Three kinds of test modes are prepared and can constitute a soft development tool by using three devices.

Radio operation can be checked by the connection between this soft development tool and IC for tuners, performing soft development.

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Power supply voltage	(Note 1)	V_{DD}	−0.3 to 4.0	V
Output Voltage 1	(Note 2)	V_{O1} (*)	−0.3 to V_{DB} + 0.3	V
Output Voltage 2	(Note 2)	V_{O2} (*)	−0.3 to 6.0	V
Input Voltage 1	(Note 3)	V_{IN1} (*)	−0.3 to V_{LCD} + 0.3	V
Input Voltage 2	(Note 3)	V_{IN2} (*)	−0.3 to V_{CPU} + 0.3	V
Input Voltage 3	(Note 3)	V_{IN3} (*)	−0.3 to 6.0	V
Input Voltage 4	(Note 3)	V_{IN4} (*)	−0.3 to V_{PLL} + 0.3	V
Input Voltage 5	(Note 3)	V_{IN5} (*)	−0.3 to V_{DD} + 0.3	V
Input Voltage 6	(Note 3)	V_{IN6} (*)	−0.3 to V_{DB} + 0.3	V
Power dissipation		P_D	100	mW
Operating temperature		T_{opr}	−10 to 60	°C
Storage temperature		T_{stg}	−65 to 150	°C

Note 1: A power supply voltage item (V_{DD}) is a the maximum rating of $V_{DD}/V_{CPU}/V_{DB}/V_{PLL}/V_{LCD}$ pin.
The potential relation is as shown follows, VDD ≤ VLCD, VDD ≤ VDB, VDD ≤ VCPU, VCPU ≤ VLCD

Note 2: The each item of output voltage is corresponded to following pin.
VO1: I/O port 6 pins, VO2: DDCK1, Tout, I/O port 8 pins

Note 3: The each item of input voltage is corresponded to following pin.
V_{IN1}: All I/O port pins excluding under pins
V_{IN2}: $\overline{\text{RESET}}$ pin
V_{IN3}: I/O port 8 pins, P9-0 pin
V_{IN4}: OSC_{in}, IF_{in} pins
V_{IN5}: $X_{in}1$ pin
V_{IN6}: I/O port 6, T_{in} pins

Electrical Characteristics
(Unless otherwise noted, Ta = 25°C, V_{DD} = V_{PLL} = 1.5 V, VDB = V_{CPU} =3.0 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Range of operating supply voltage (Note 1)	V_{DD}	—	(V_{DD}) (*)	0.9	to	1.8	V
	V_{CPU}	—	(V_{CPU}) (*)	1.2	to	3.6	
	V_{PLL}	—	(V_{PLL}) PLL operation (*)	0.9	to	1.8	
Range of memory hold voltage	V_{HD}	—	(V_{CPU}) Back-up mode (*)	0.75	~	3.6	
Operating current (Note2)	I_{DD1}	—	PLLOperation, OSCin = 30 MHz	—	1.0	1.5	mA
	I_{DD2}	—	Under CPU operation only, (PLL off, LCD driver operating)	—	150	300	μA
	I_{DD3}	—	In Hard wait mode, (Crystal oscilator operating only)	—	120	—	
	I_{DD4}	—	In Soft wait mode, (CPU intermittent operating only)	—	140	—	
Memoey retention current	I_{HD1}	—	(V_{DD}, V_{PLL}) CKSTP instruction excuted	—	0.1	10	
	I_{HD2}	—	(V_{CPU}) CKSTP instruction excuted (At setting the detect the voltage off), V_{DD} off (At setting the detect the voltage on)	—	0.01	0.5	

Note 1: Use power supply voltage in the range; $V_{DD} \leq V_{LCD}$, $V_{DD} \leq V_{DB}$, $V_{DD} \leq V_{CPU}$ and $V_{CPU} \leq V_{LCD}$.

Note 2: Power supply current of operation is total current of V_{DD}, V_{CPU}, and V_{PLL} power supply pins.

Crystal Oscillator Circuit (X_{in1}, X_{out1})

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Crystal oscilation frequency	f_{XT1}	—	(Xin_1, $Xout_1$) (*)	—	75	—	kHz
Crystal oscilation start-up time	t_{st1}	—	(Xin_1, $Xout_1$) f_{XT1}= 75 kHz	—	—	1.0	s
Xin1 amplifire feedback resistor	R_{fXT1}	—	(Xin_1 – $Xout_1$)	—	20	—	MΩ
Xout1 output resistor	R_{OUT1}	—	($Xout_1$)	50	100	200	kΩ

High Speed Oscillator Circuit (X_{in2}, X_{out2})

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
High speed oscilation frequency range	f_{XT2}	—	(Xin_2, $Xout_2$) (*)	300	—	600	kHz
High speed oscilation start-up time	t_{st2}	—	(Xin_2, $Xout_2$) f_{XT2} = 300 to 600 kHz	—	—	100	ms
Xin2 amplifire feedback resistor	R_{fXT2}	—	(Xin_2 - $Xout_2$)	—	1	—	MΩ
Xout2 output resistor	R_{OUT2}	—	($Xout_2$)	1	2	4	kΩ
Oscilator operating current (Note 3)	I_{XT2}	—	(Xin_2 - $Xout_2$)	—	50	—	μA

Note 3: This current value is increasing consumption current value when high-speed oscillator is used.

For conditions marked by an asterisk (*), guaranteed when V_{DD} = V_{PLL} = 0.9 to 1.8 V, V_{CPU} = 1.2 to 3.6 V, Ta = -10 to 60°C

Constant Voltage Output (V_{EE}), Doubler Voltager Output (V_{LCD})

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Dobler boosting voltage	VDB1	—	(VDB) GND reference Clamp off, Charge–pump doubler voltage	—	VDD × 2	—	V
	VDB2	—	(VDB) GND reference Clamp voltage = 2.0 V	—	2.0	—	
	VDB3		(VDB) GND reference Clamp voltage = 2.5 V	—	2.5	—	
	VDB4		(VDB) GND reference Clamp voltage = 3.0 V	—	3.0	—	
	VLCD		(VLCD) GND reference	—	VEE × 2	—	
Clump doubler voltage setting eroor	ΔVDB		(VDB) Charge pump doubler V_{EE} = 1.5 V	—	—	0.05	V
			(VDB) Switching regulalor doubler, V_{EE} = 1.5 V	—	—	±0.05	
Constant voltage	VEE	—	(VEE) GND reference (*)	1.46	1.50	1.54	V

Programmable Counter, IF Counter

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating frequency range	HF mode	f HF	—	(OSCin) V_{IN} = 0.1 to 0.6 V_{p-p}(*)	1.0	to	30	MHz
	LF mode	f LF	—	(OSCin) V_{IN} = 0.1 to 0.6 V_{p-p}(*)	0.5	to	4	
	IFin1	f IF1	—	(IFin) V_{IN} = 0.1 to 0.6 V_{p-p} (*) NC = 0 setting	0.35	~	12	
	IFin2	f IF2	—	(IFin) V_{IN} = 0.1 to 0.6 V_{p-p} (*) NC = 1 setting	0.03	~	1	
Input amplitude range	HF mode	VHF	—	(OSCin) f_{IN} = 1.0 to 30 MHz (*)	0.1	to	0.6	V_{p-p}
	LF mode	VLF	—	(OSCin) f_{IN} = 0.5 to 10 MHz (*)	0.1	to	0.6	
	IFin1	VIF1	—	(IFin) f_{IN} = 0.35 to 12 MHz (*) NC = 0 setting	0.1	to	0.6	
	IFin2	VIF2	—	(IFin) f_{IN} = 0.03 to 1 MHz (*) NC = 1 setting	0.1	to	0.6	
Input amplifire feedback resistor		Rf_{IN1}	—	(OSCin)	250	500	1000	kΩ
		Rf_{IN2}	—	(IFin)	250	500	1000	kΩ

For conditions marked by an asterisk (*), guaranteed when V_{DD} = V_{PLL} = 0.9 to 1.8 V, V_{CPU} = 1.2 to 3.6 V, Ta = -10 to 60°C

I/O port 1 to 6 (P1-0 to P16-3), Seirial Interface (SCK1/2, RX1/2, SDIO1/2, TX1/2) (Note4)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH1	—	V_{DD} = 0.9 to 1.8 V, V_{LCD} = 3.0V, V_{OH} = V_{DD} − 0.2 V (Except I/O port 6,8,P9-0)	−0.4	−0.8	—	mA
		IOH1L	—	V_{DD} = 0.9V, V_{LCD} = 3.0V, V_{OH} = V_{DD} − 0.2 V (Except I/O port 6,8,P9-0)	—	−0.5	—	
	"L" level	IOL1	—	V_{DD} = 0.9 to 1.8 V, V_{LCD} = 3.0V, V_{OL} = 0.2 V (Except I/O port 8,P9-0)	0.4	0.8	—	
		IOL2	—	V_{DD} = 0.9 to 1.8 V, V_{LCD} = 3.0V, V_{OL} = 0.2 V (P8-0 to P8-3)	2	4	—	
		IOL3	—	V_{DD} = 0.9 to 1.8 V, V_{LCD} = 3.0V, V_{OL} = 0.2 V (P9-0)	—	20	—	
Input leak currrent		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V (Except I/O port 6,8)	—	—	±1.0	μA
			—	V_{IH} = V_{DB}, V_{IL} = 0 V (P6-0 to P6-3)				
			—	V_{IH} = 5.5 V, V_{IL} = 0 V (P8-0 to P8-3, P9-0)				
Input voltage	"H" level	V_{IH}	—	—	V_{DD} × 0.8	to	V_{DD}	V
	"L" level	V_{IL}	—	—	0	to	V_{DD} × 0.2	
Input pull-up/pull-down resistor		R_{IN1}	—	When P3-0 to P3-3 are set to pull-up or pull-down	25	50	100	kΩ
Input pull-down resistor		R_{IN2}	—	(TEST) When $\overline{RESET}$ = "L"	—	10	—	kΩ
SCK input frequency		fSIO	—	When I/O ports are set to srial clock input (SCK1/SCK2)	—	—	200	kHz

Note 4: the electrical characteristic in serial interface conditions is same as characteristic in the same I/O port.

LCD Driver Output (COM1 to COM4, S1 to S18)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	IOH4	—	V_{LCD} = 3.0 V, V_{OH} = V_{LCD} − 0.2 V	—	−0.2	—	mA
	"L" level	IOL4	—	V_{LCD} = 3.0 V, V_{OL} = 0.2 V	—	0.5	—	
Bias vlotage	1/3 V_{LCD} level	VBS2	—	V_{LCD} = 3 V, No load, When 1/3 bais type select	0.85	1.00	1.15	V
	1/2 V_{LCD} level	VBS3	—	V_{LCD} = 3 V, V_{EE} = 1.5 V, No load, When 1/2 bais type select	1.35	1.5	1.65	
	2/3 V_{LCD} level	VBS4	—	V_{LCD} = 3 V, No load, When 1/3 bais type select	1.85	2.00	2.15	
LCD driver operaating current (Note 5)		I_{LCD2}	—	No load, When 1/2 bais type select	—	5	—	μA
		I_{LCD3}	—	No load, When 1/3 bais type select	—	100	—	

Note 5: This current value is increasing consumption current value when LCD driver circuit is used.

Electrical Volume (VRout1, VRin1, VRcom, VRin2, VRout2)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Volume resistor	R_{VR}	—	IN to GND resitor	15	30	60	kΩ
Switch on resistor	R_{ON}	—	Analog switch on resistor	—	500	800	Ω
Attenuation error	ΔATT	—	—	—	0	±2.0	dB

A/D Converter (ADin1 to A/Din4)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog iput voltage range	VAD	—	(ADin1 to A/Din4)	0	to	V_{DB}	V
Resolution	VRES	—	—	—	6	—	bit
Conversion total error	—	—	—	—	±0.5	±1.0	LSB
Analog input leak	ILI	—	$V_{IH} = V_{DB}$, $V_{IL} = 0$ V (A/Din1 to A/Din4)	—	—	±1.0	μA

Phase Comparator (DO1/OT1/P, DO2/OT2/N)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH5}	—	V_{DB} = 3.0 V, $V_{OH} = V_{DB} - 0.2$ V When output resistor is off	−0.4	−0.8	—	mA
	"L" level	I_{OL5}	—	V_{DB} = 3.0 V, V_{OL} = 0.2 V When output resistor is off	0.4	0.8	—	
Output reistor		ROUT1	—	(DO1, DO2)	—	5	—	kΩ
		ROUT2	—	(DO1, DO2)	—	50	—	
		ROUT3	—	(DO1, DO2)	—	100	—	
Tri-state current		ITL	—	(DO1, DO2) V_{DB} = 3.0 V, V_{TLH} = 3.0 V, V_{TLL} = 0 V	—	—	±100	nA

DC-DC Converter Doubler Vlotage Detection for VT (VDET, DDCK1, DDCK2)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Doubler voltage range	VOUT	—	—	0	~	5.5	V
Doubler voltage detection set up error	ΔVDET	—	(VDET) V_{EE} = 1.5 V	—	—	±0.05	V
Detection operating current (Note 6)	IDET	—	(VDET)	—	10	—	μA
"H" level output current	IOH1	—	(DDCK2) VOL = 0.2 V, When set up DDCK2	−0.4	−0.8	—	mA
"L" level output current	IOL1	—	(DDCK2) VOL = 0.2 V, When set up DDCK1	0.4	0.8	—	
	IOL2	—	(DDCK1) VOL = 0.2 V, When set up DDCK1	2	4	—	
Output off leak current	IOFF	—	(DDCK1) VIH = 5.5 V, When set up DDCK1	—	—	±1.0	μA

Note 6: This current value is increasing consumption current value when doubler voltage detection circuit is used.

Transistor for Low Pass Filter (Tout, Tin)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
"L" level output current	IOL3	—	(Tout) V_{OL} = 0.2 V, Tin = 1.5 V		20	—	mA
Output off leak ccurrent	Ioff	—	(Tout) V_{OH} = 5.5 V, Tin = 0 V	—	—	±1.0	μA
Input leak current	ILI	—	(Tin) VOB = V_{IH} = 3.6 V V_{IL} = 0 V	—	—	±1.0	μA

Reset Signal Input ($\overline{\text{RESET}}$)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leak current		ILI	—	V_{CPU} = V_{IH}, V_{IL} = 0 V	—	—	±1.0	μA
Input Vlotage	"H" level	V_{IH}	—	—	V_{CPU} × 0.8	to	V_{CPU}	V
	"L" level	V_{IL}	—	—	0	to	V_{CPU} × 0.2	

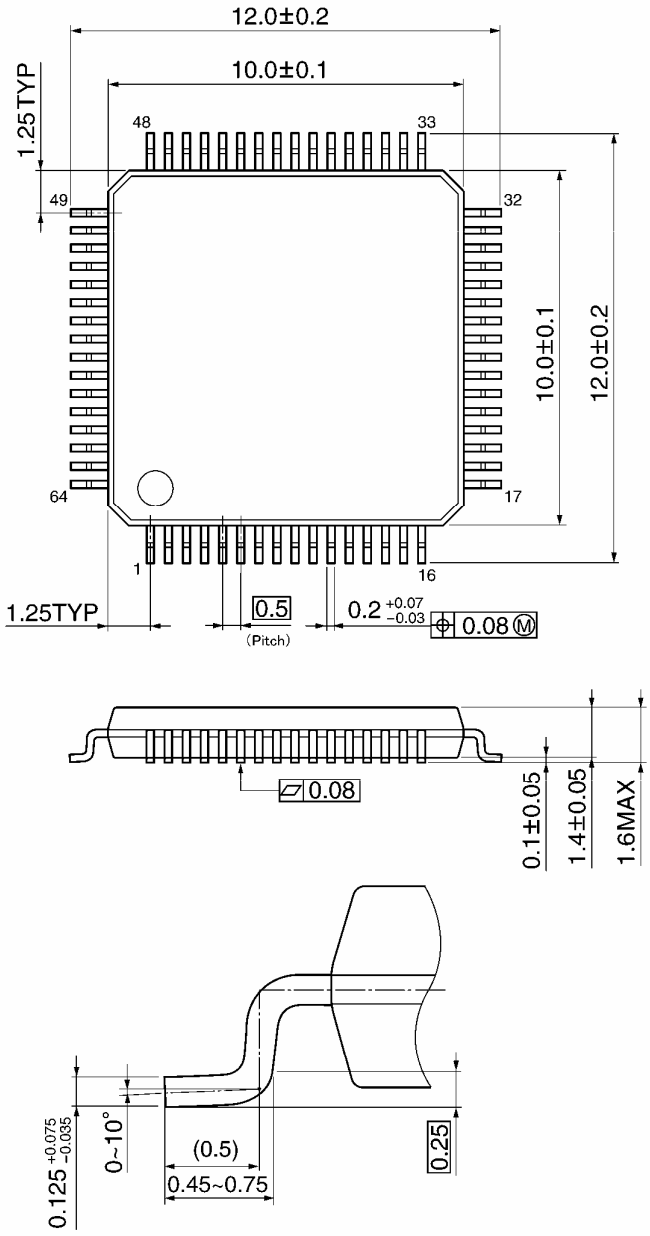
Detected Reduce Vlotage Circuit

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Detected reduce voltage set up error	ΔVBL	—	(VDD) V_{EE} = 1.5 V	—	—	±0.03	V
Detected reduce voltage operating current (Note 7)	ILI	—	—	—	20	—	μA

Note 7: This current value is increasing consumption current value when detected reduces voltage circuit is used.

Package Dimensions

LQFP64-P-1010-0.50E Unit: mm



Note : Lead type Pd-Pff

Weight: 0.32 g (typ.)

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