

2-Mbit (128K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

Features

- AEC-Q100 qualified
- High speed
 - t_{AA} = 10 ns; 12 ns
- Temperature range
 - Automotive-A: -40 °C to 85 °C
 - Automotive-E: -40 °C to 125 °C
- Embedded error-correcting code (ECC) for single-bit error correction^[1]
- Low active and standby current
 - Active current, I_{CC} = 40-mA typical (Automotive-E)
 - Standby current, I_{SB2} = 6-mA typical (Automotive-E)
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- TTL compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

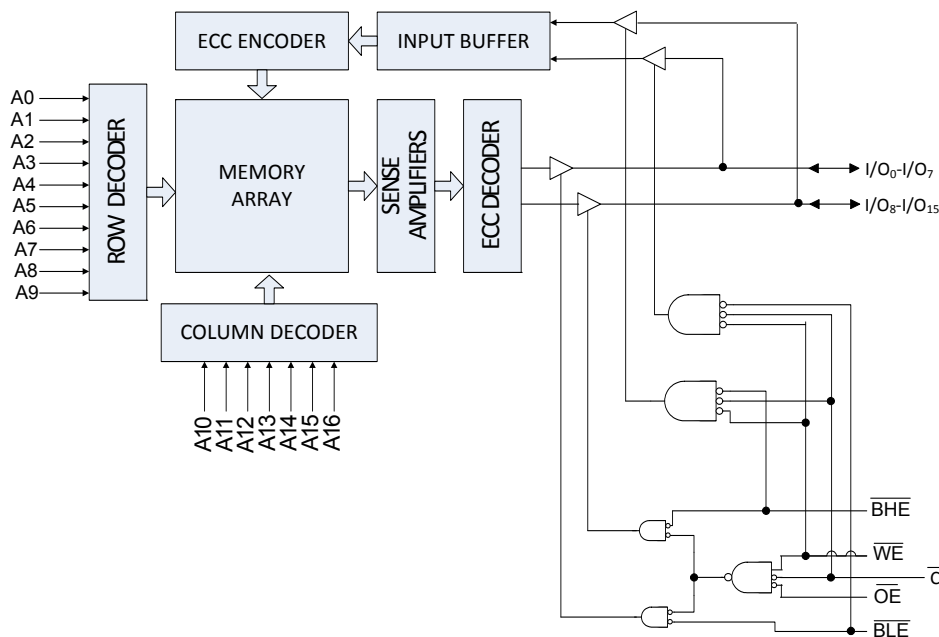
CY7C1011G is a high-performance CMOS fast static RAM automotive part with embedded ECC. This device has a single Chip Enable (\overline{CE}) input, and is accessed by asserting it LOW.

To perform data writes, assert the Write Enable (\overline{WE}) input LOW, and provide the data on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{16}) pins. The Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. \overline{BHE} controls I/O_8 through I/O_{15} and \overline{BLE} controls I/O_0 through I/O_7 .

To perform data reads, assert the Output Enable (\overline{OE}) input and provide the required address on the address lines. You can access read data on the I/O lines (I/O_0 through I/O_{15}). To perform byte access, assert the required byte enable signal (\overline{BHE} or \overline{BLE}) to read either the upper byte or the lower byte of data from the specified address location.

All I/O s (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (\overline{CE} LOW), or when the control signals are deasserted (\overline{OE} , \overline{BLE} , \overline{BHE}).

Logic Block Diagram – CY7C1011G



Note

1. This device does not support automatic write-back on error detection.

Contents

Pin Configurations	3	Ordering Information	12
Product Portfolio	3	Ordering Code Definitions	12
Maximum Ratings	4	Package Diagrams	13
Operating Range	4	Acronyms	15
DC Electrical Characteristics	4	Document Conventions	15
Capacitance	5	Units of Measure	15
Thermal Resistance	5	Document History Page	16
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	17
Data Retention Characteristics	6	Worldwide Sales and Design Support	17
Data Retention Waveform	6	Products	17
AC Switching Characteristics	7	PSoC® Solutions	17
Switching Waveforms	8	Cypress Developer Community	17
Truth Table	11	Technical Support	17

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.2 mm) pinout^[2]

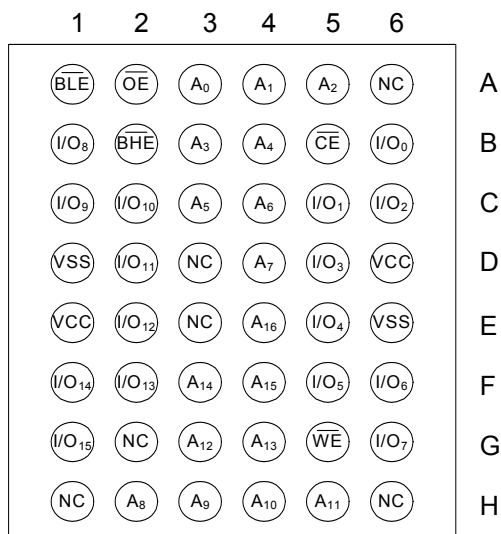
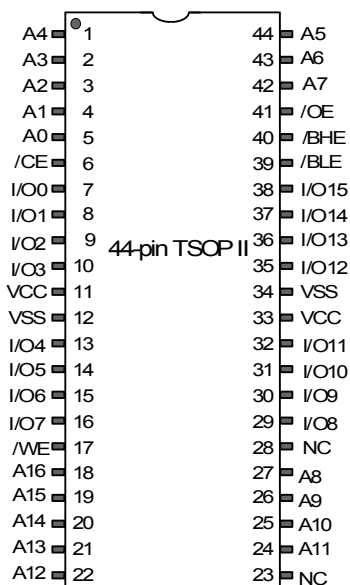


Figure 2. 44-pin TSOP II pinout^[2]



Product Portfolio

Product	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation			
				Operating I _{CC} , (mA)		Standby, I _{SB2} (mA)	
				f = f _{max}			
				Typ ^[3]	Max	Typ ^[3]	Max
CY7C1011G30	Automotive-E	2.2 V–3.6 V	10, 12	40	50	6	14
	Automotive-A		10	38	45	6	8

Notes

- NC pins are not connected internally to the die.
- Typical values are included for reference only and are not guaranteed or tested.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied -55 °C to +125 °C

Supply voltage
on V_{CC} relative to GND^[4] -0.5 V to $V_{CC} + 0.3$ V

DC voltage applied to outputs
in HI-Z State^[4] -0.3 V to $V_{CC} + 0.3$ V

DC input voltage^[4] -0.3 V to $V_{CC} + 0.3$ V

Current into outputs (in low state) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Automotive-E	-40 °C to +125 °C	2.2 V to 3.6 V
Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions	10 ns (Automotive-A)			10 ns/ 12ns (Automotive-E)			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2	–	–	2	–	–	V
		2.7 V to 3.0 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	–	–	2.2	–	–	
		3.0 V to 3.6 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	–	–	2.4	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	–	–	0.4	–	–	0.4	V
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	–	–	0.4	–	–	0.4	
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V	–	2	–	$V_{CC} + 0.3^{[4]}$	2	–	$V_{CC} + 0.3^{[4]}$	V
		2.7 V to 3.6 V	–	2	–	$V_{CC} + 0.3^{[4]}$	2	–	$V_{CC} + 0.3^{[4]}$	
V_{IL}	Input LOW voltage	2.2 V to 2.7 V	–	-0.3 ^[4]	–	0.6	-0.3 ^[4]	–	0.6	V
		2.7 V to 3.6 V	–	-0.3 ^[4]	–	0.8	-0.3 ^[4]	–	0.8	
I_{IX}	Input leakage current		$GND \leq V_{IN} \leq V_{CC}$	-1	–	+1	-5	–	+5	μA
I_{OZ}	Output leakage current		$GND \leq V_{OUT} \leq V_{CC}$, Output disabled	-1	–	+1	-5	–	+5	μA
I_{CC}	Operating supply current		$V_{CC} = 3.6 \text{ V}$, $I_{OUT} = 0 \text{ mA}$, CMOS levels	–	38	45	–	40	50	mA
I_{SB1}	Automatic CE power down current – TTL inputs		$V_{CC} = 3.6 \text{ V}$, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	–	–	15	–	–	24	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		$V_{CC} = 3.6 \text{ V}$, $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$	–	6	8	–	6	14	mA

Note

4. $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

Capacitance

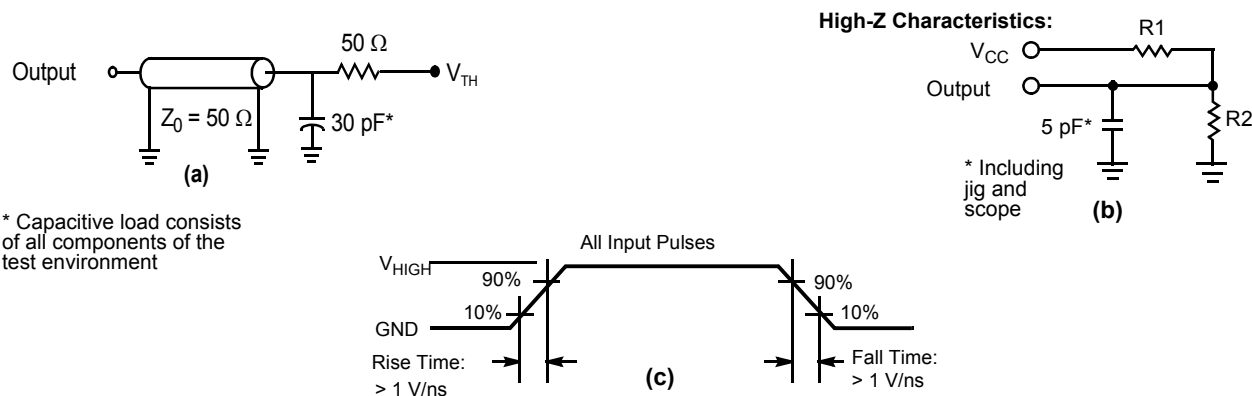
Parameter ^[5]	Description	Test Conditions	All Packages	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter ^[5]	Description	Test Conditions	48-ball VFBGA	44-pin TSOPII	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	30.68	66.82	$^{\circ}\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		14.83	15.97	$^{\circ}\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[6]



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{TH}	1.5	V
V_{HIGH}	3	V

Notes

5. Tested initially and after any design or process change that may affect these parameters.

6. Full-device AC operation assumes a 100- μs ramp time from 0 to $V_{CC(\text{min})}$ and a 100- μs wait time after V_{CC} stabilization.

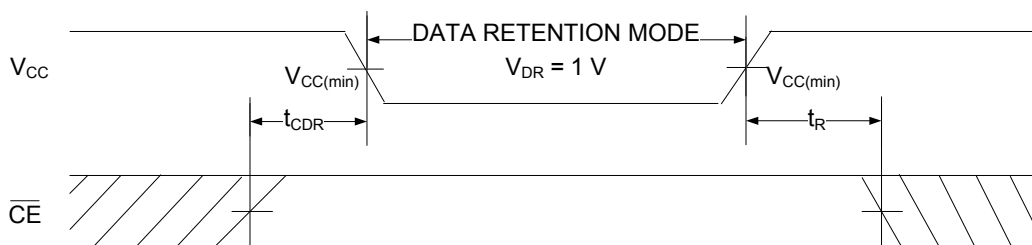
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Automotive-A		Automotive-E		Unit
			Min	Max	Min	Max	
V_{DR}	V_{CC} for data retention	—	1	—	1	—	V
I_{CCDR}	Data retention current	$V_{CC} = 1.2\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	—	8	—	14	mA
$t_{CDR}^{[7]}$	Chip deselect to data retention time	—	0	—	0	—	ns
$t_R^{[7, 8]}$	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$, $t_{AA} = 10\text{ ns}$	10	—	10	—	ns
		$V_{CC} \geq 2.2\text{ V}$, $t_{AA} = 12\text{ ns}$	—	—	12	—	ns

Data Retention Waveform

Figure 4. Data Retention Waveform^[8]



Notes

7. These parameters are guaranteed by design.
8. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min.)} \geq 100\text{ }\mu\text{s}$.

AC Switching Characteristics

Over the Operating Range

Parameter ^[9]	Description	10 ns (Automotive-A/ Automotive-E)		12 ns (Automotive-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{RC}	Read cycle time	10	–	12	–	ns
t _{AA}	Address to data	–	10	–	12	ns
t _{OHA}	Data	3	–	3	–	ns
t _{ACE}	\overline{CE} LOW to data ^[10]	–	10	–	12	ns
t _{DOE}	\overline{OE} LOW to data	–	4.5	–	7	ns
t _{LZOE}	\overline{OE} LOW to low impedance ^[10, 11]	0	–	0	–	ns
t _{HZOE}	\overline{OE} HIGH to HI-Z ^[10, 11]	–	5	–	6	ns
t _{LZCE}	\overline{CE} LOW to low impedance ^[10, 10, 11]	3	–	3	–	ns
t _{HZCE}	\overline{CE} HIGH to HI-Z ^[10, 10, 11]	–	5	–	6	ns
t _{PU}	\overline{CE} LOW to power up ^[10, 11]	0	–	0	–	ns
t _{PD}	\overline{CE} HIGH to power down ^[10, 11]	–	10	–	12	ns
t _{DBE}	Byte enable to data valid	–	4.5	–	7	ns
t _{LZBE}	Byte enable to low impedance ^[11]	0	–	0	–	ns
t _{HZBE}	Byte disable to HI-Z ^[11]	–	6	–	6	ns
Write Cycle ^[12, 13]						
t _{WC}	Write cycle time	10	–	12	–	ns
t _{SCE}	\overline{CE} LOW to write end ^[10]	7	–	8	–	ns
t _{AW}	Address setup to write end	7	–	8	–	ns
t _{HA}	Address hold from write end	0	–	0	–	ns
t _{SA}	Address setup to write start	0	–	0	–	ns
t _{PWE}	\overline{WE} pulse width	7	–	8	–	ns
t _{SD}	Data setup to write end	5	–	6	–	ns
t _{HD}	Data hold from write end	0	–	0	–	ns
t _{LZWE}	\overline{WE} HIGH to low impedance ^[10, 11]	3	–	3	–	ns
t _{HZWE}	\overline{WE} LOW to HI-Z ^[10, 11]	–	5	–	6	ns
t _{BW}	Byte Enable to write end	7	–	8	–	ns

Notes

9. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 5, unless specified otherwise.
10. t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} , t_{LZOE} , t_{LZCE} , t_{LZWE} , and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 5. Transition is measured ± 200 mV from steady state voltage.
11. These parameters are guaranteed by design and are not tested.
12. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and \overline{BHE} or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
13. The minimum write cycle pulse width for Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY7C1011G (Address Transition Controlled) [14, 15]

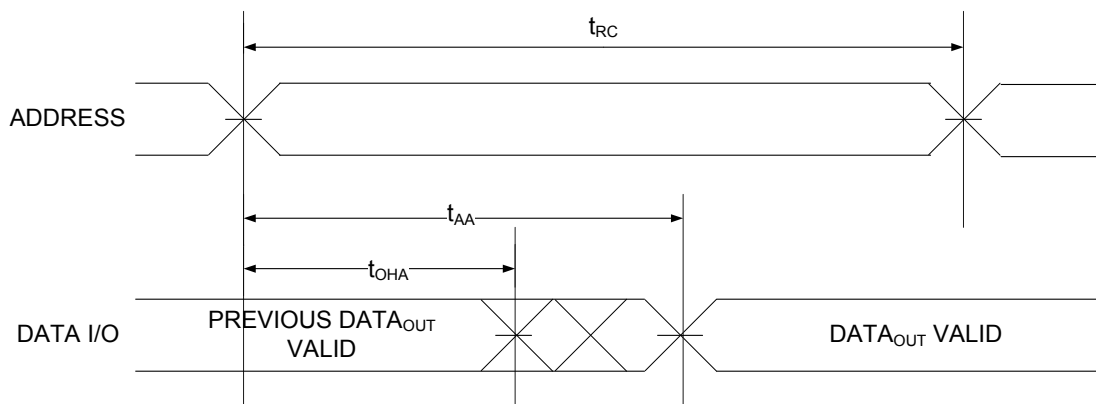
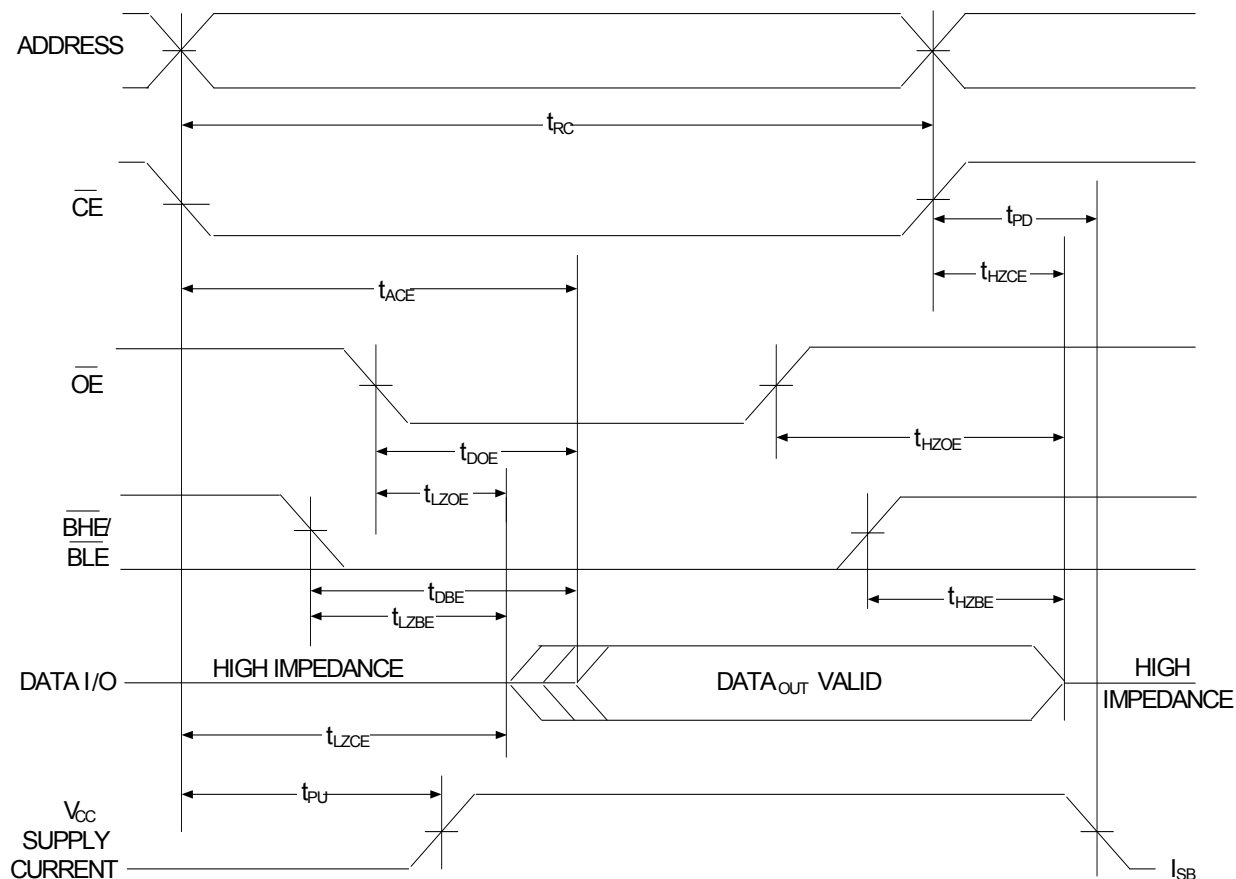


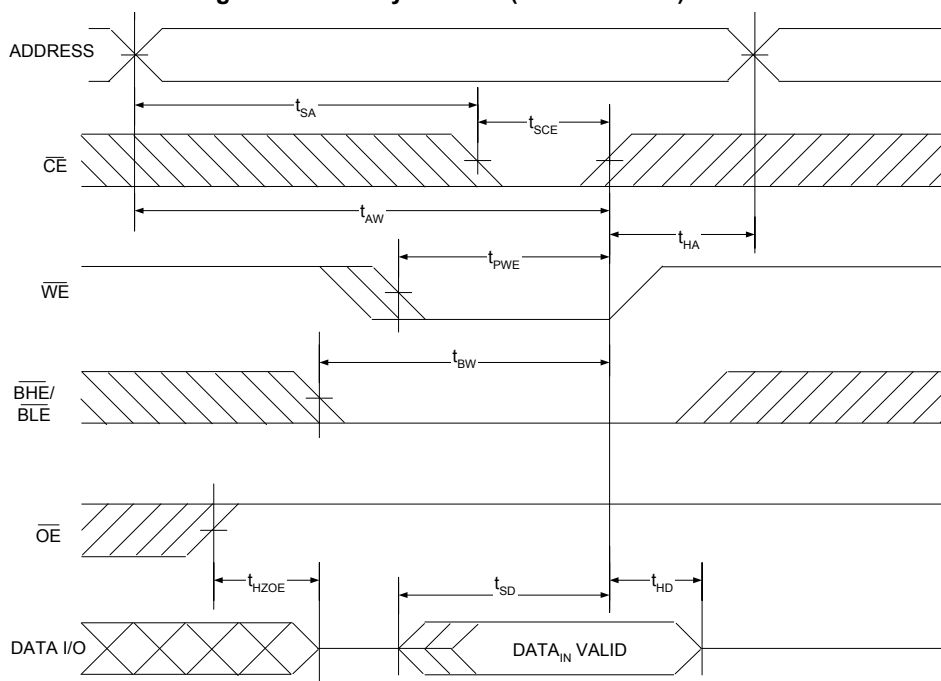
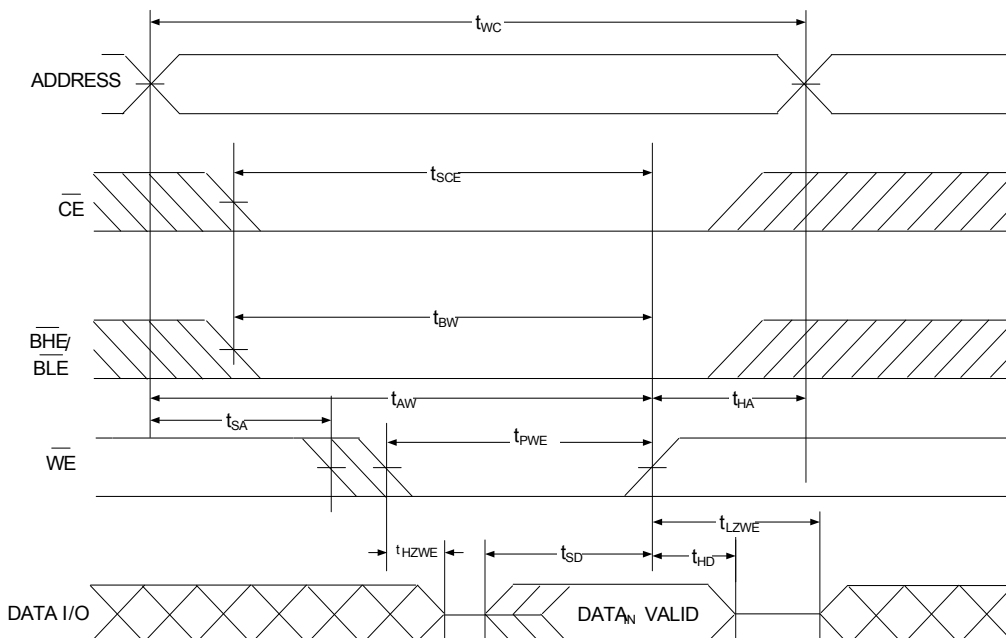
Figure 6. Read Cycle No. 2 (\overline{OE} Controlled) [15]



Notes

14. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} .

15. \overline{WE} is HIGH for read cycle.

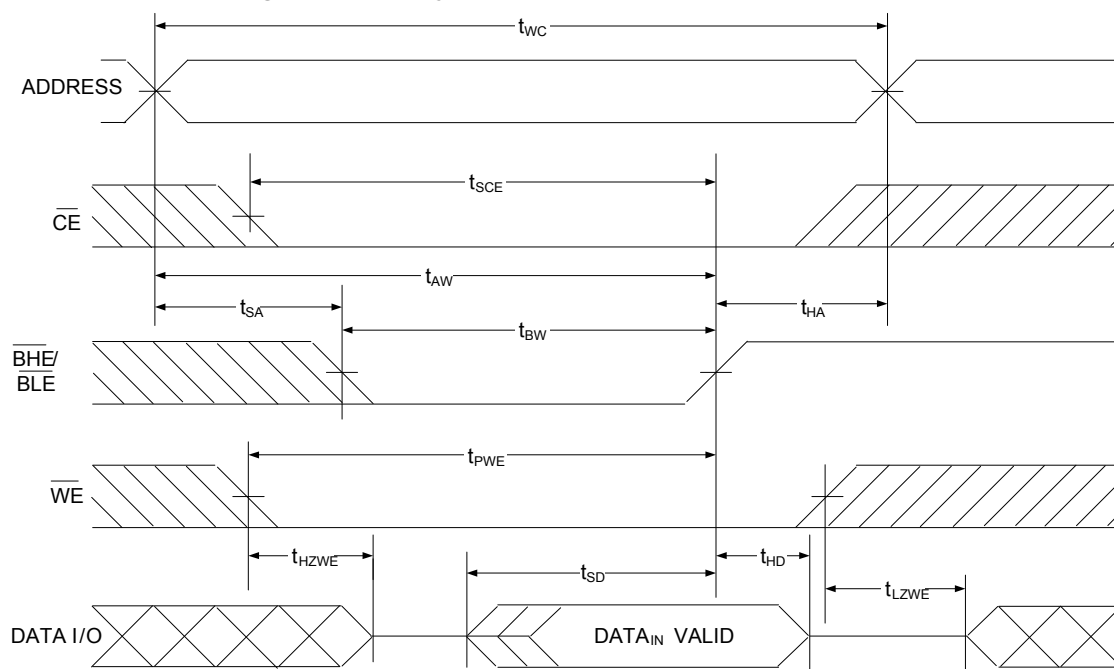
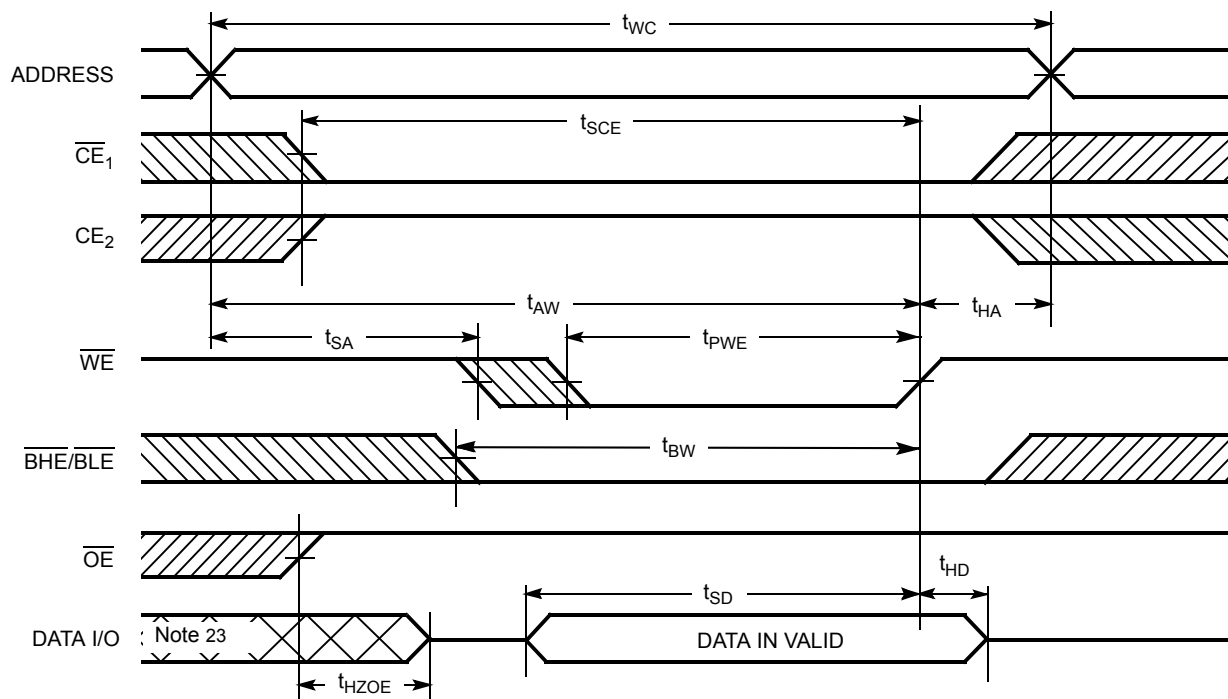
Switching Waveforms (continued)
Figure 7. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [16, 17, 18]

Figure 8. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [16, 17, 18, 19]

Notes

16. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.

17. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$ and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

18. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.

19. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE} .

Switching Waveforms (continued)
Figure 9. Write Cycle No. 3 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled) [20, 21]

Figure 10. Write Cycle No. 4 ($\overline{\text{WE}}$ Controlled) [20, 21, 22]

Notes

20. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$ and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

21. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.

22. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.

23. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	HI-Z	HI-Z	Power-down	Standby (I _{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I _{CC})
L	L	H	L	H	Data out	HI-Z	Read lower bits only	Active (I _{CC})
L	L	H	H	L	HI-Z	Data out	Read upper bits only	Active (I _{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
L	X	L	L	H	Data in	HI-Z	Write lower bits only	Active (I _{CC})
L	X	L	H	L	HI-Z	Data in	Write upper bits only	Active (I _{CC})
L	H	H	X	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I _{CC})

Ordering Information

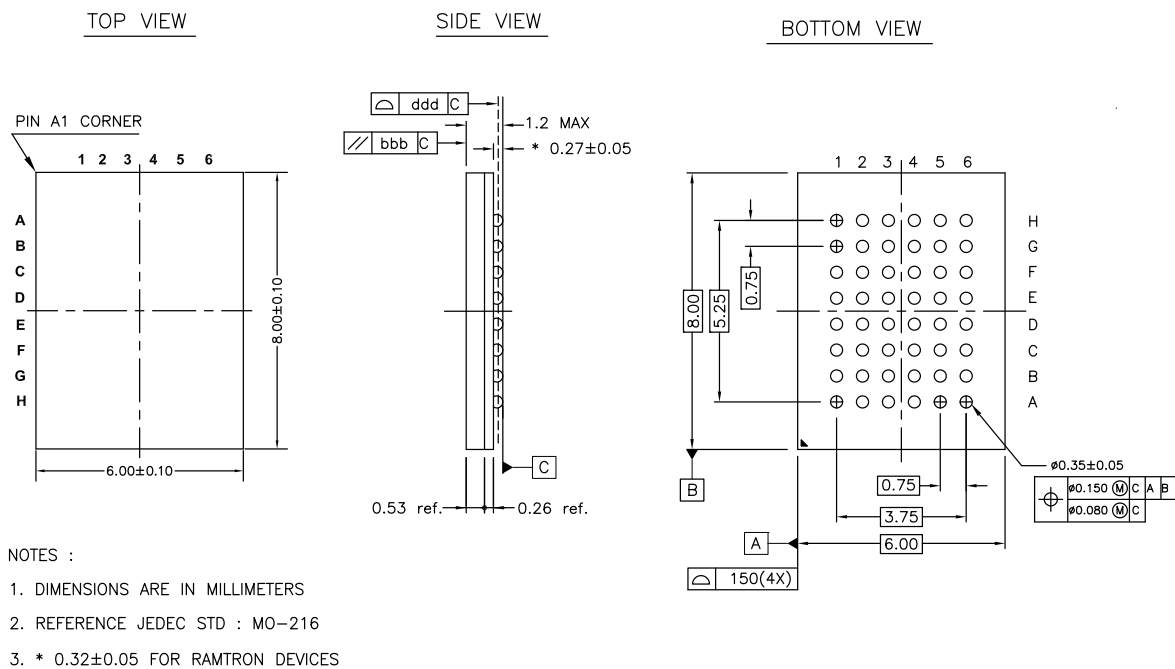
Speed (ns)	Ordering Code	Voltage Range	Package Diagram	Package Type (All Pb-free)	Operating Range
10	CY7C1011G30-10ZSXA	2.2 V–3.6 V	51-85087	44-pin TSOP II	Automotive-A
	CY7C1011G30-10ZSXAT	2.2 V–3.6 V	51-85087	44-pin TSOP II, Tape & Reel	Automotive-A
	CY7C1011G30-10BAJXE	2.2 V–3.6 V	001-85259	48-ball VFBGA	Automotive-E
	CY7C1011G30-10BAJXET	2.2 V–3.6 V	001-85259	48-ball VFBGA, Tape & Reel	Automotive-E
12	CY7C1011G30-12ZSXE	2.2 V–3.6 V	51-85087	44-pin TSOP II	Automotive-E
	CY7C1011G30-12ZSXET	2.2 V–3.6 V	51-85087	44-pin TSOP II, Tape & Reel	Automotive-E

Ordering Code Definitions

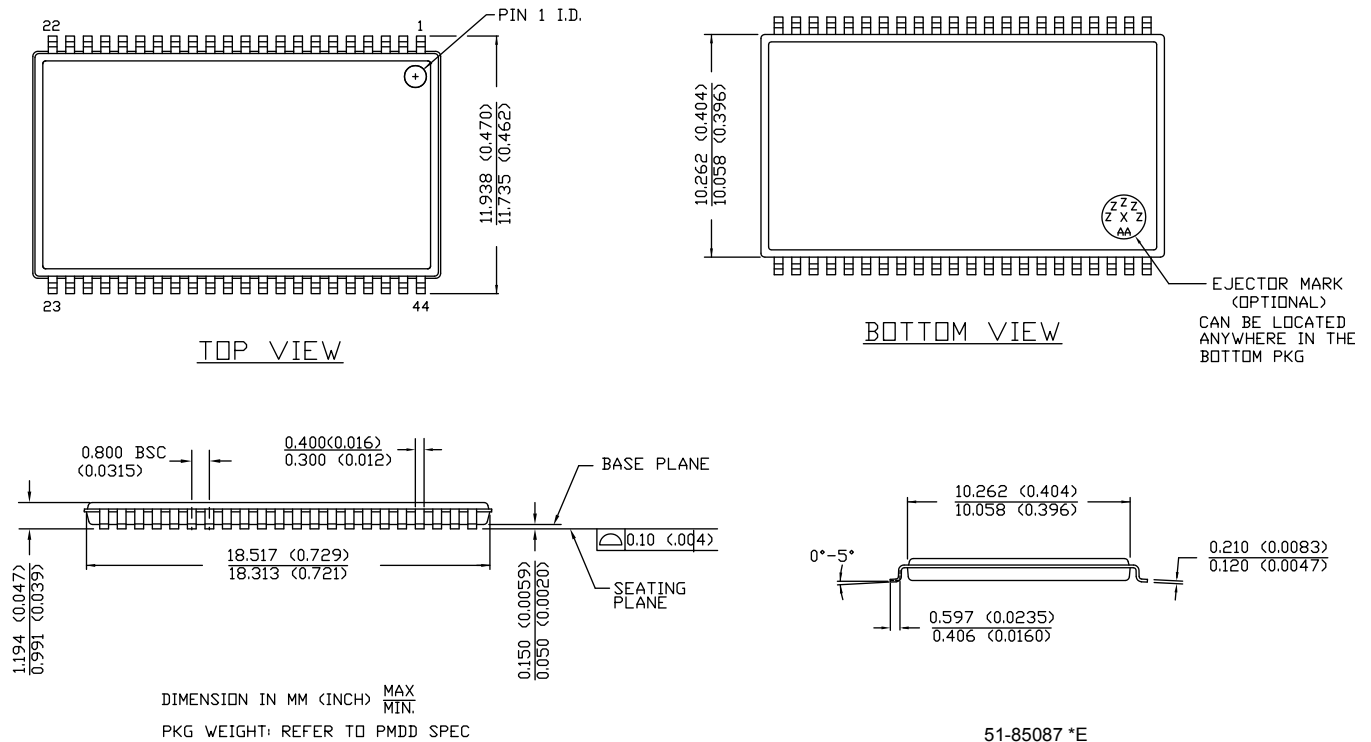
CY	7	C	1	04	1	G	30	-	XX	XX	J	X	X	X	
															X = blank or T blank = Bulk; T = Tape and Reel
															Temperature Range: X = A or E A = Automotive-A; E = Automotive-E
															Pb-free
															J = JEDEC Compliant (only for BGA package)
															Package Type: XX = BA or ZS BA = 48-ball VFBGA; ZS = 44-pin TSOP II
															Speed: XX = 10 ns or 12 ns
															Voltage Range: 30 = 2.2 V–3.6 V
															Process Technology: Revision Code "G" = 65 nm Technology
															Data Width: 1 = × 16-bits
															Density: 04 = 4-Mbit
															Family Code: 1 = Fast Asynchronous SRAM family
															Technology Code: C = CMOS
															Marketing Code: 7 = SRAM
															Company ID: CY = Cypress

Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.2 mm) BA48M/BK48M (0.35 mm Ball Diameter) Package Outline, 001-85259



001-85259 *A

Package Diagrams (continued)
Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087


Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1011G Automotive, 2-Mbit (128K words × 16-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-95423				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*A	4998910	NILE	11/02/2015	Changed status from Preliminary to Final.
*B	5024020	NILE	11/23/2015	Updated Ordering Information : Updated part numbers.
*C	5692050	NILE	04/27/2017	Added 12 ns speed bin related information in all instances across the document. Updated Features : Added "AEC-Q100 qualified". Updated DC Electrical Characteristics : Removed details of V _{OH} parameter corresponding to "2.7 V to 3.6 V". Added details of V _{OH} parameter corresponding to "2.7 V to 3.0 V" and "3.0 V to 3.6 V". Updated Note 4 (Replaced "2 ns" with "20 ns"). Updated Ordering Information : Updated part numbers. Updated to new template. Completing Sunset Review.
*D	5725360	NILE	05/03/2017	Updated Ordering Information : Updated part numbers.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2015–2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.