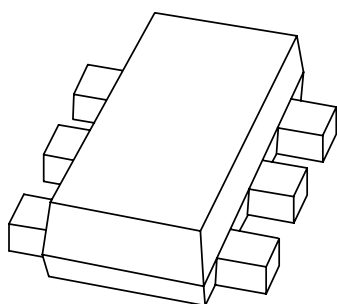


# DATA SHEET



## **PESD3V3L5UV; PESD5V0L5UV** Low capacitance 5-fold ESD protection diode arrays in SOT666 package

Product specification

2004 Mar 23

## Low capacitance 5-fold ESD protection diode arrays in SOT666 package

**PESD3V3L5UV;  
PESD5V0L5UV**

### FEATURES

- Uni-directional ESD protection of up to five lines
- Bi-directional ESD protection of up to four lines
- Low diode capacitance
- Maximum peak pulse power:  $P_{pp} = 25 \text{ W}$  at  $t_p = 8/20 \mu\text{s}$
- Low clamping voltage:  $V_{CL(R)} = 12 \text{ V}$  at  $I_{pp} = 2.5 \text{ A}$
- Ultra low leakage current:  $I_{RM} = 8 \text{ nA}$  at  $V_{RWM} = 5 \text{ V}$
- ESD protection > 20 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge);  $I_{pp} = 2.5 \text{ A}$  at  $T_p = 8/20 \mu\text{s}$ .

### APPLICATIONS

- Cellular handsets and accessories
- Portable electronics
- Computers and peripherals
- Communications systems
- Audio and video equipment.

### DESCRIPTION

Low capacitance 5-fold ESD protection array in the ultra small SOT666 plastic package designed to protect up to five transmission or data lines from the damage caused by Electrostatic Discharge (ESD).

### MARKING

TYPE NUMBER	MARKING CODE <sup>(1)</sup>
PESD3V3L5UV	*E1
PESD5V0L5UV	*E2

#### Note

1. \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

### ORDERING INFORMATION

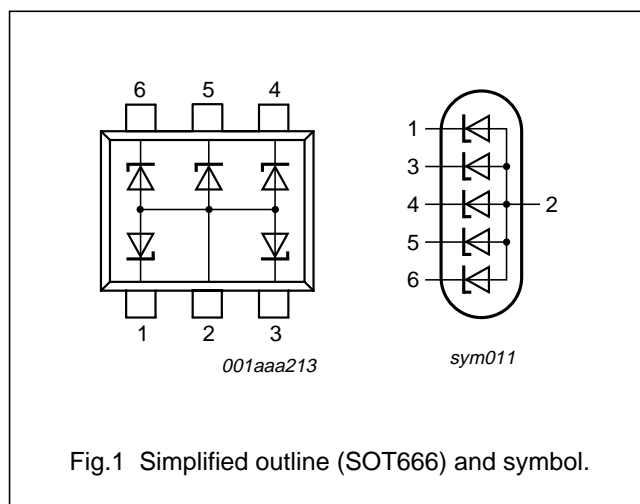
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PESD3V3L5UV	–	plastic surface mounted package; 6 leads	SOT666
PESD5V0L5UV	–	plastic surface mounted package; 6 leads	SOT666

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	VALUE	UNIT
$V_{RWM}$	reverse standoff voltage PESD3V3L5UV	3.3	V
	PESD5V0L5UV	5	V
$C_d$	diode capacitance PESD3V3L5UV	22	pF
	PESD5V0L5UV	16	pF
	number of protected lines	5	

### PINNING

PIN	DESCRIPTION
1	cathode 1
2	common anode
3	cathode 2
4	cathode 3
5	cathode 4
6	cathode 5



## Low capacitance 5-fold ESD protection diode arrays in SOT666 package

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per diode</b>					
P <sub>pp</sub>	peak pulse power	8/20 μs pulse; notes 1 and 2	–	25	W
I <sub>pp</sub>	peak pulse current	8/20 μs pulse; notes 1 and 2	–	2.5	A
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operation ambient temperature		–65	+150	°C
T <sub>stg</sub>	storage temperature		–65	+150	°C

### Notes

1. Non-repetitive current pulse 8/20 μs exponentially decaying waveform; see Fig.2.
2. Measured from any of pins 1, 3, 4, 5 or 6 to pin 2.

### ESD maximum ratings

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
<b>Per diode</b>				
ESD	electrostatic discharge capability	IEC 61000-4-2 (contact discharge); notes 1 and 2	20	kV
		HBM MIL-Std 883	10	kV

### Notes

1. Device stressed with ten non-repetitive Electrostatic Discharge (ESD) pulses; see Fig.3.
2. Measured from any of pins 1, 3, 4, 5 or 6 to pin 2.

### ESD standards compliance

ESD STANDARD	CONDITIONS
IEC 61000-4-2, level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
HBM MIL-Std 883, class 3	> 4 kV

Low capacitance 5-fold ESD protection  
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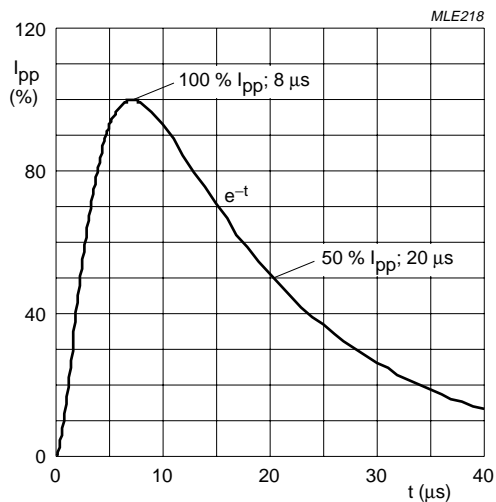


Fig.2 8/20  $\mu s$  pulse waveform according to IEC 61000-4-5.

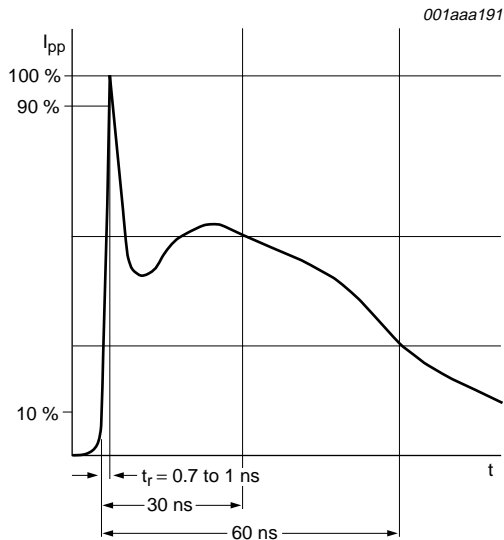


Fig.3 Electrostatic Discharge (ESD) pulse waveform according to IEC 61000-4-2.

# Low capacitance 5-fold ESD protection diode arrays in SOT666 package

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## CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per diode</b>						
$V_{RWM}$	reverse stand-off voltage PESD3V3L5UV		–	–	3.3	V
	PESD5V0L5UV		–	–	5	V
$I_{RM}$	reverse leakage current PESD3V3L5UV	$V_{RWM} = 3.3\text{ V}$	–	75	300	nA
	PESD5V0L5UV	$V_{RWM} = 5\text{ V}$	–	5	25	nA
$V_{BR}$	breakdown voltage PESD3V3L5UV	$I_R = 1\text{ mA}$	5.3	5.6	5.9	V
	PESD5V0L5UV		6.4	6.8	7.2	V
$C_d$	diode capacitance PESD3V3L5UV	$f = 1\text{ MHz}$ ; $V_R = 0\text{ V}$ ; see Fig.5	–	22	28	pF
	PESD5V0L5UV		–	16	19	pF
$V_{CL(R)}$	clamping voltage PESD3V3L5UV	notes 1 and 2 $I_{pp} = 1\text{ A}$	–	–	10	V
		$I_{pp} = 2.5\text{ A}$	–	–	12	V
	PESD5V0L5UV	$I_{pp} = 1\text{ A}$	–	–	10	V
		$I_{pp} = 2.5\text{ A}$	–	–	12	V
$r_{diff}$	differential resistance PESD3V3L5UV	$I_R = 1\text{ mA}$	–	–	200	$\Omega$
	PESD5V0L5UV		–	–	100	$\Omega$

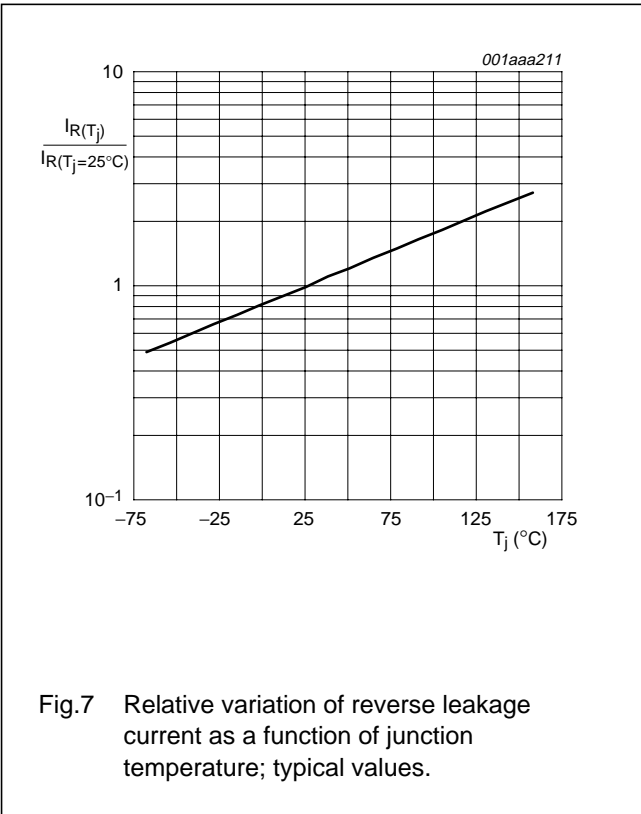
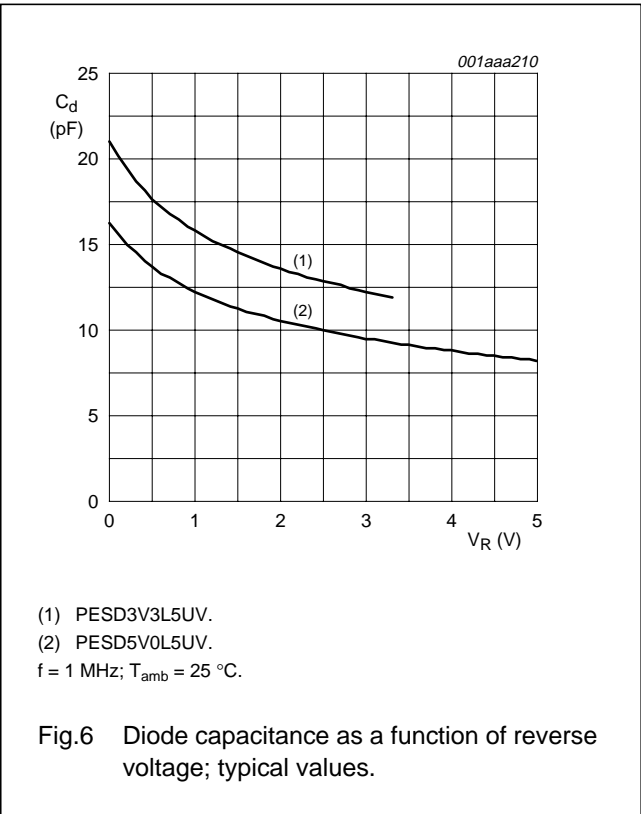
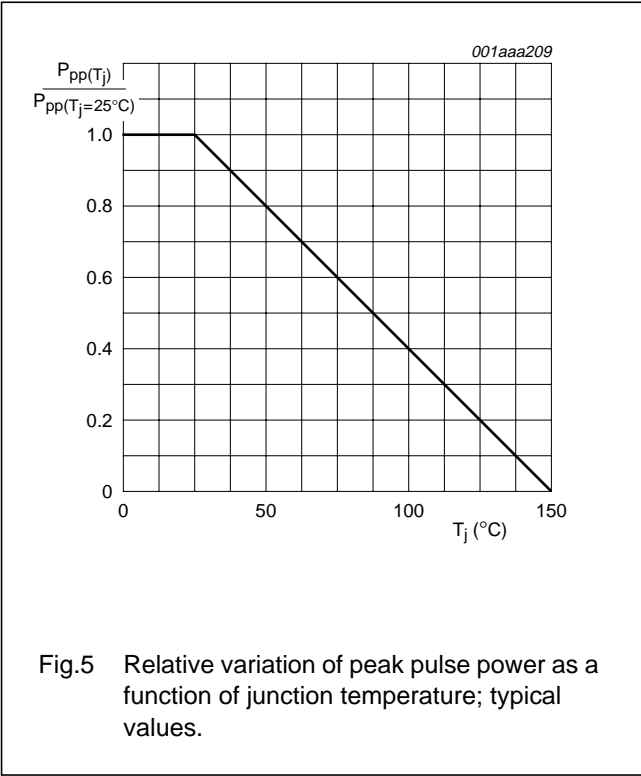
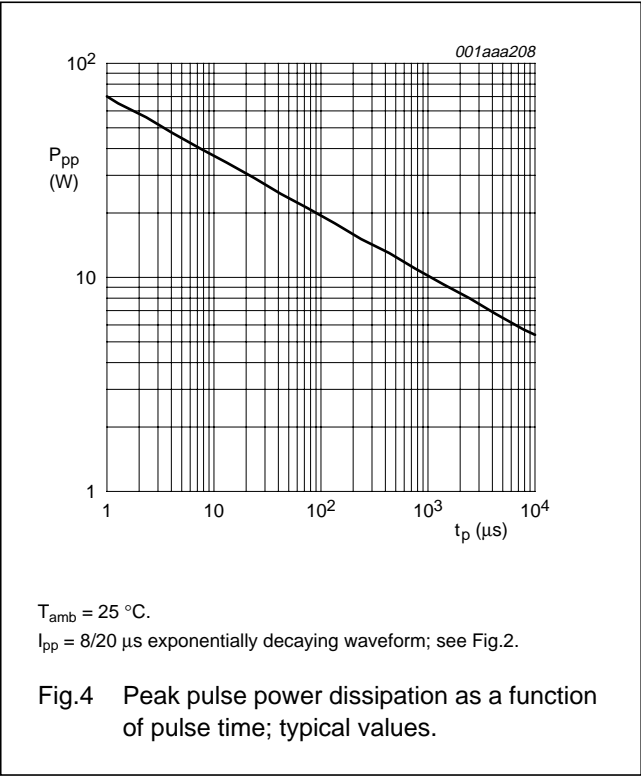
## Notes

1. Non-repetitive current pulse 8/20  $\mu\text{s}$  exponentially decaying waveform; see Fig.2.
2. Measured from any of pins 1, 3, 4, 5 or 6 to pin 2.

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GRAPHICAL DATA



## Low capacitance 5-fold ESD protection diode arrays in SOT666 package

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PESD5V0L5UV

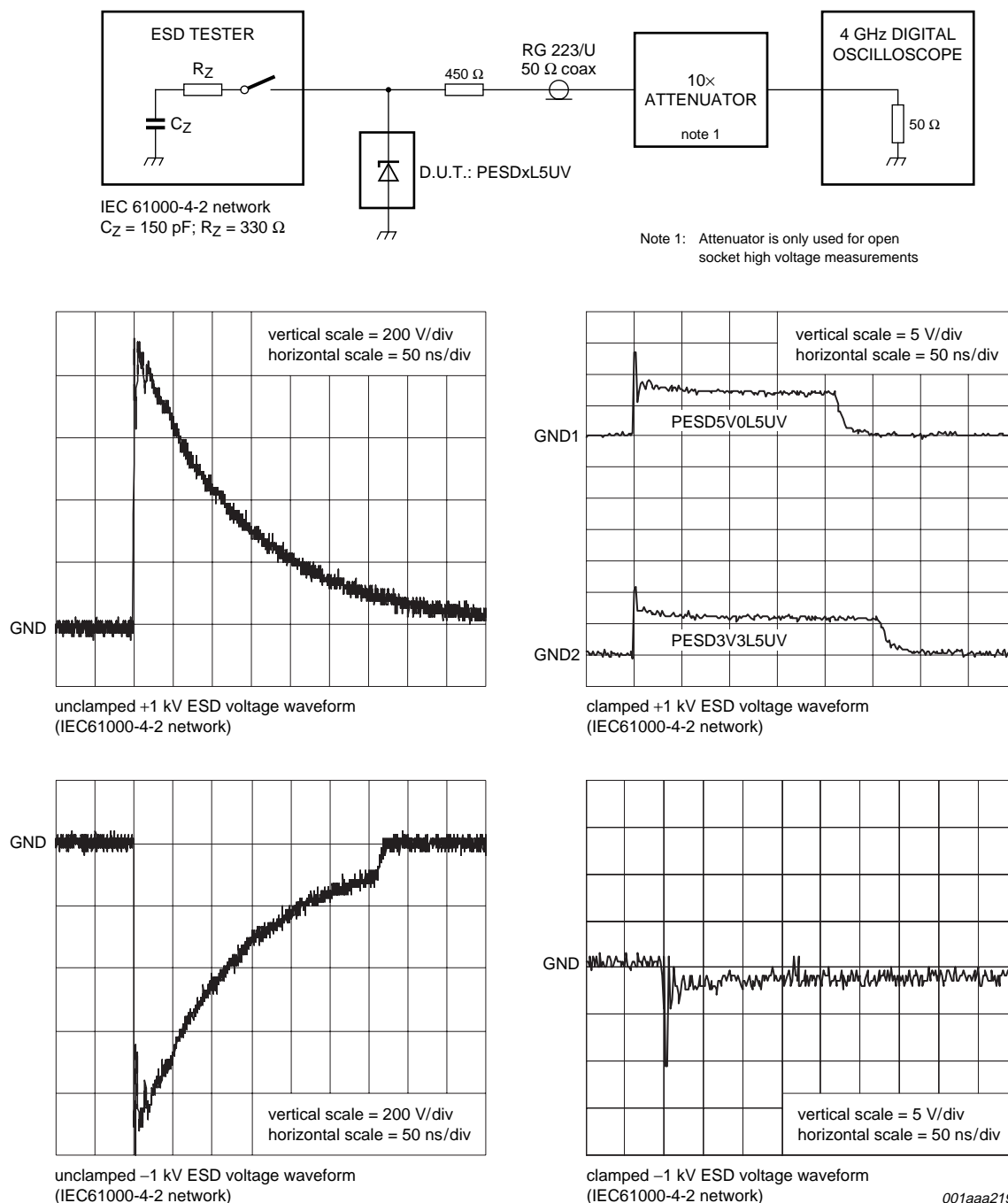


Fig.8 ESD clamping test setup and waveforms.

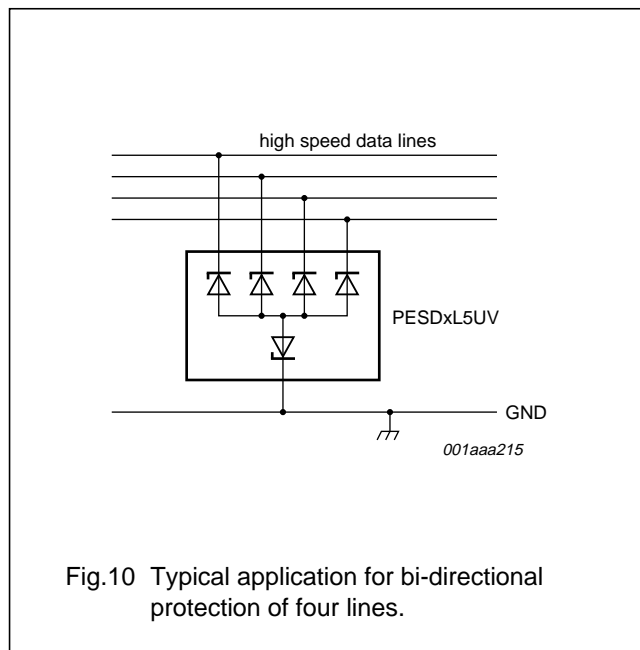
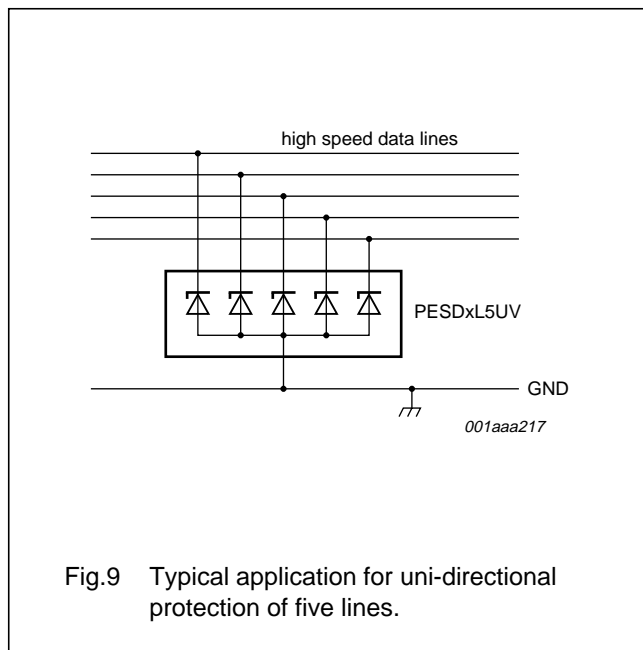
## Low capacitance 5-fold ESD protection diode arrays in SOT666 package

PESD3V3L5UV;  
PESD5V0L5UV

### APPLICATION INFORMATION

The PESDxL5UV is designed for the uni-directional protection of up to five lines or bi-directional protection of four lines from the damage caused by Electrostatic Discharge (ESD) and surge pulses. The PESDxL5UV may be used on lines where the signal polarities are above or below ground. PESDxL5UV can withstand and provides protection from a surge of 25 watts peak pulse power per line for a 8/20  $\mu$ s waveform.

#### Typical application



#### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. The protection device should be placed as closely as possible to the input terminal or connector.
2. The path length between the protection device and the protected line should be as short as possible.
3. Parallel signal paths should be kept to a minimum.
4. Running protection conductors in parallel with unprotected conductor should be avoided.
5. All printed-circuit board conductive loops (including power and group loops) should be kept to a minimum.
6. The length of the transient return path to ground should be kept to a minimum.
7. The use of shared transient return paths to a common ground point should be avoided.
8. Ground planes should be used whenever possible.
9. For multilayer printed-circuit boards, ground vias should be used.



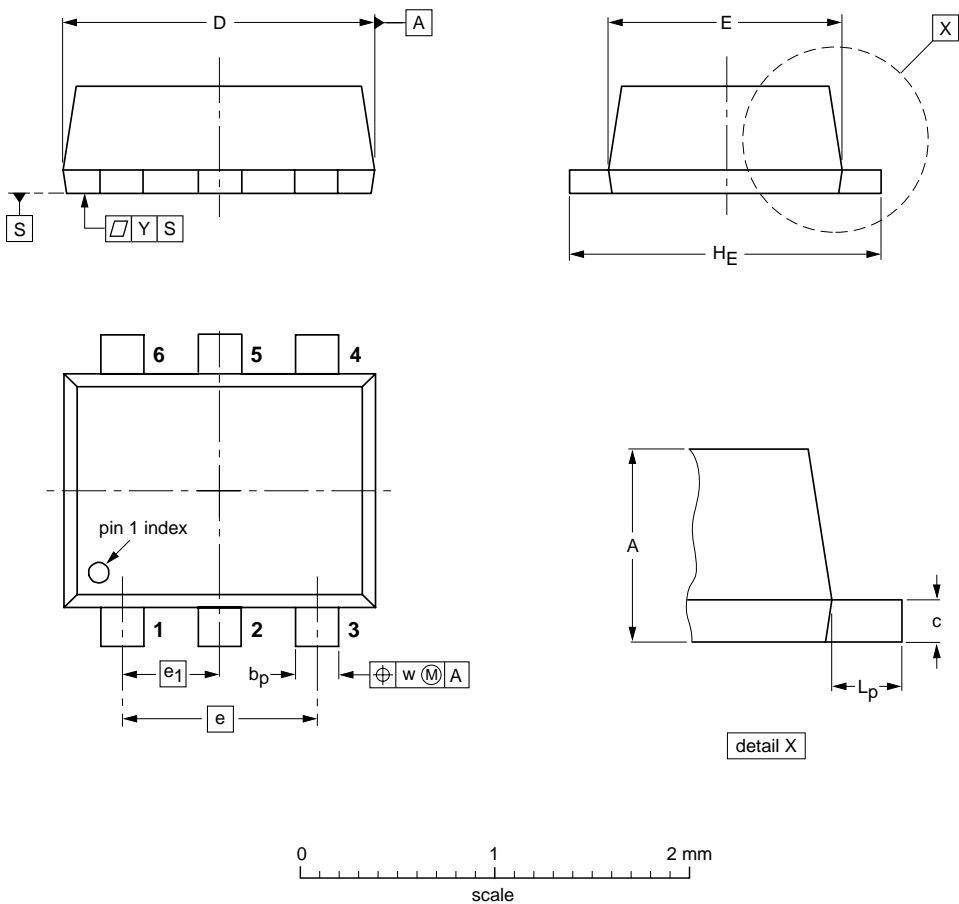
Low capacitance 5-fold ESD protection  
diode arrays in SOT666 package

PESD3V3L5UV;  
PESD5V0L5UV

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						<del>01-01-04</del> 01-08-27

# Low capacitance 5-fold ESD protection diode arrays in SOT666 package

PESD3V3L5UV;  
PESD5V0L5UV

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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