PI74FCT543T/544T
(25Ω Series) PI74FCT2543T

Fast CMOS
Latched Transceivers

Product Features:

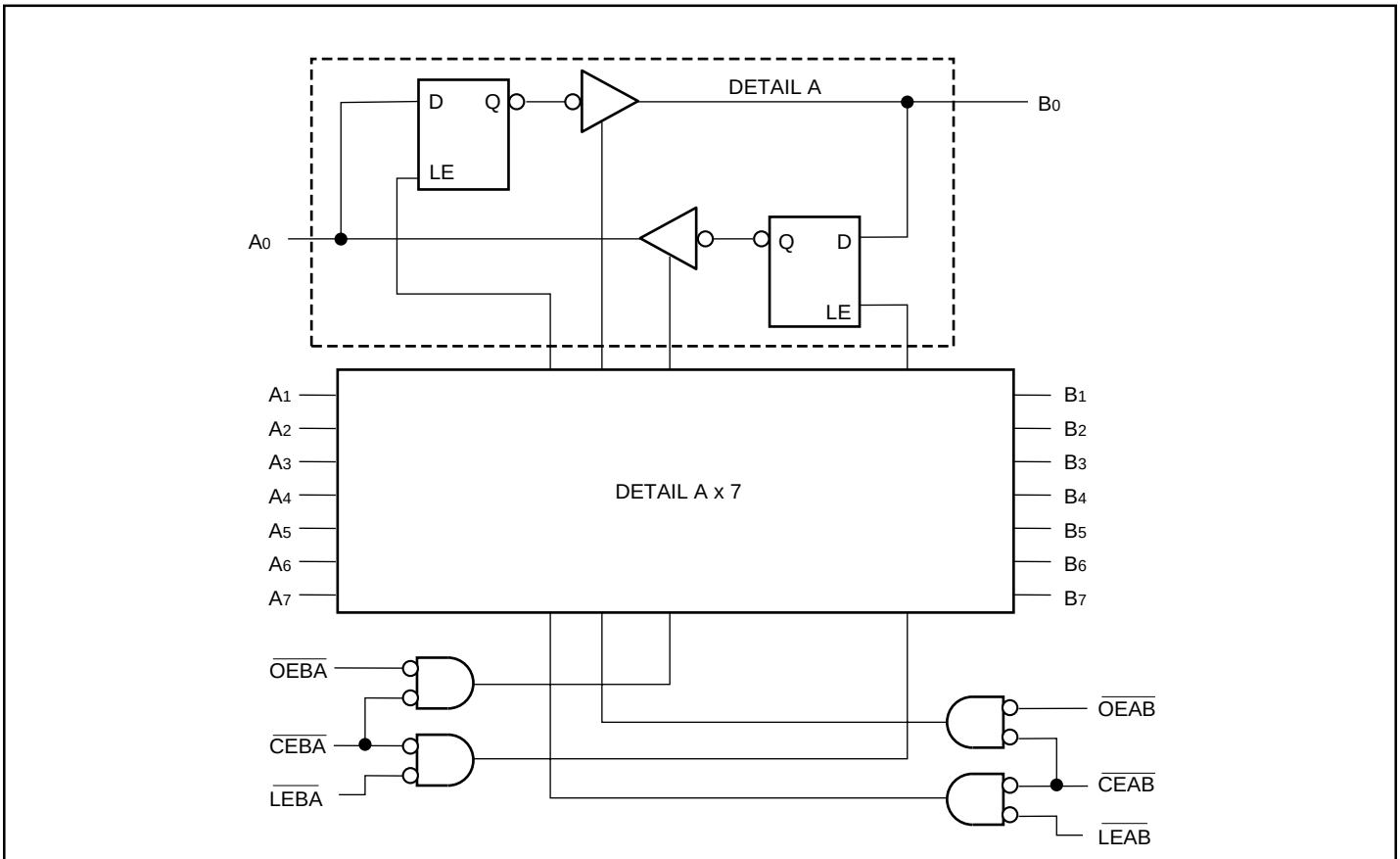
- PI74FCT543T/544/2543T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  – 24-pin 300 mil wide plastic DIP (P)
  – 24-pin 150 mil wide plastic QSOP (Q)
  – 24-pin 150 mil wide plastic TQSOP (R)
  – 24-pin 300 mil wide plastic SOIC (S)
- Device models available on request

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25 ohm series resistor on all outputs to reduce noise because of reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT543T/544T and PI74FCT2543T is an 8-bit wide non-inverting transceiver designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A0–A7 or to take data from B0–B7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs. The PI74FCT543T is a non-inverting of the PI74FCT544T.

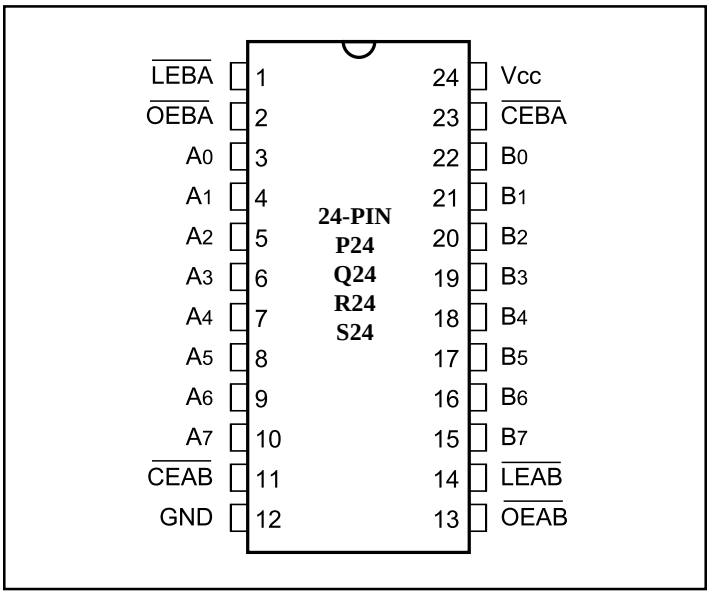
PI74FCT543/544/2543T Logic Block Diagram



NOTE: PI74FCT543/2543T function is shown.

PS2020A 03/11/96

PI74FCT543/544/2543T Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A0-A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0-B7	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
VCC	Power

PI74FCT543/2543T Truth Table (Non-Inverting)[1,2] For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0–B7
H	—	—	Storing	High-Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

1. *Before $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   — = Don't Care or Irrevelant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0 mA	2.4	3.0		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64 mA		0.3	0.55	V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA (25Ω Series)		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	(Except I/O pins) V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	(Except I/O pins) V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{IH}	Input HIGH Current	(I/O pins Only) V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	(I/O pins Only) V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current		V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5V		—	—	100	µA
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = VCC One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz (LEAB) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} f_I = 5 MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		1.5	3.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		2.0	5.5[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz (LEAB) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = Vcc Eight Bits Toggling f_I = 2.5 MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		3.8	7.3[5]	
			V_{IN} = 3.4V V_{IN} = GND		6.0	16.3[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT543/2543T (non-inverting) Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	543T/2543T Com. Min	543T/2543T Com. Max	543AT/2543AT Com. Min	543AT/2543AT Com. Max	543CT/2543CT Com. Min	543CT/2543CT Com. Max	543DT Com. Min	543DT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	C_L = 50 pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_N, $\overline{LEAB}$ to B_N		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	ns
t_{PZH} t_{PZL}	Output Disable Time[3] $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	ns
t_{SU}	Setup Time, HIGH or LOW A_N or B_N to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	2.0	—	2.0	—	1.5	—	ns
t_H	Hold Time, HIGH or LOW A_N or B_N to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	1.5	—	ns
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW[3]		5.0	—	5.0	—	5.0	—	3.0	—	ns

PI74FCT544T (inverting) Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	544T Com. Min	544T Com. Max	544AT Com. Min	544AT Com. Max	544CT Com. Min	544CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	C_L = 50 pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_N, $\overline{LEAB}$ to B_N		2.5	12.5	2.5	8.0	2.5	7.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N		2.0	12.0	2.0	9.0	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Disable Time[3] $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N		2.0	9.0	2.0	7.5	2.0	6.5	ns
t_{SU}	Setup Time, HIGH or LOW A_N or B_N to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	2.0	—	2.0	—	ns
t_H	Hold Time, HIGH or LOW A_N or B_N to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	ns
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW[3]		5.0	—	5.0	—	5.0	—	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.