AN6555, AN6556, AN6556S

Low Noise Dual Operational Amplifiers

■ Outline

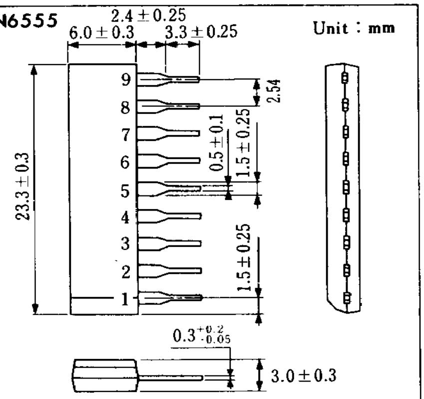
The AN6555, the AN6556, and the AN6556S are low noise, high slew rate dual operational amplifiers with phase compensation circuits built-in.

They are suited for application to various electronic circuits such as active filters and audio preamplifiers.

■ Features

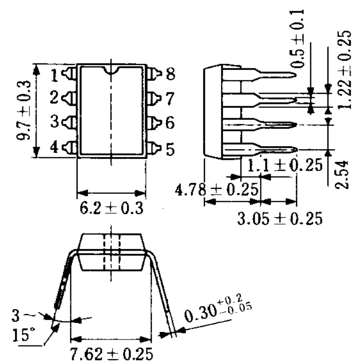
- Phase compensation circuit
- High gain : $G_V = 100$ dB typ.
- Low noise : input referred noise voltage $V_{nI} = 1.5\mu V_{rms}$ typ.
- High slew rate : $SR = 2V/\mu s$ typ.
- Output short-circuit protection

AN6555 Unit : mm



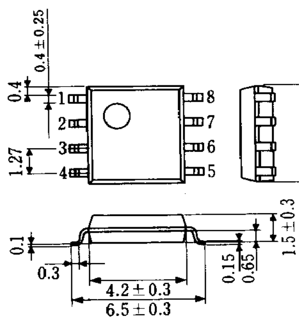
9-Lead SIL Plastic Package

AN6556 Unit : mm



8-Lead DIL Plastic Package

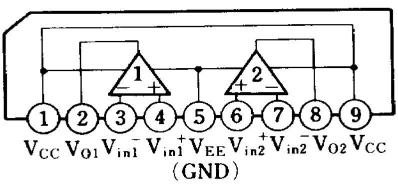
AN6556S Unit : mm



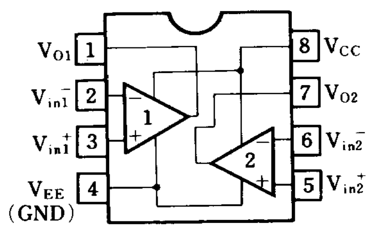
8-Lead PANAFLAT Package(SO-8D)

■ Block Diagrams

AN6555



AN6556
AN6556S



■ Pin

〈AN6555〉

Pin No.	Pin Name
1	V_{CC}
2	Ch. 1 Output
3	Ch. 1 Invert Input
4	Ch. 1 Non Invert Input
5	V_{EE}(GND)
6	Ch. 2 Non Invert Input
7	Ch. 2 Invert Input
8	Ch. 2 Output
9	Vcc

〈AN6556, AN6556S〉

Pin No.	Pin Name
1	Ch. 1 Output
2	Ch. 1 Invert Input
3	Ch. 1 Non Invert Input
4	V_{EE}(GND)
5	Ch. 2 Non Invert Input
6	Ch. 2 Invert Input
7	Ch. 2 Output
8	Vcc

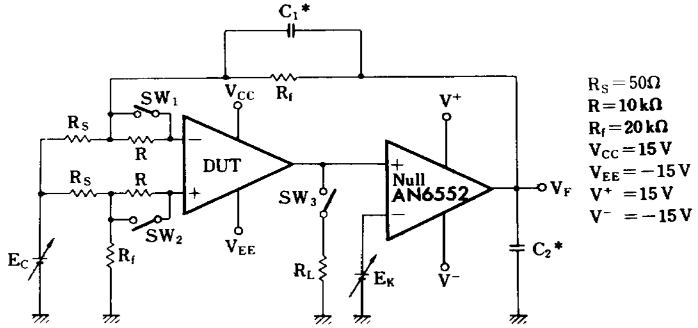
■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V_{CC}	±18	V
	Differential Input Voltage	V_{ID}	±30	V
	Common-Mode Input Voltage	V_{ICM}	±15	V
Power Dissipation	AN6555, AN6556S	P_D	500	mW
	AN6556S		360	
Operating Ambient Temperature		T_{opr}	−20～+75	℃
Storage Temperature	AN6555, AN6556	T_{stg}	−55～+150	℃
	AN6556S		−55～+125	

■ Electrical Characteristics (V_{CC}=15V, V_{EE}=−15V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(offset)}$	1	$R_S \leq 10k\Omega$		0.5	6	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_{Bias}	1				500	nA
Voltage Gain	G_V	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	100		dB
Maximum Output Voltage	$V_{O(max.)}$	2	$R_L \geq 10k\Omega$	±12	±14		V
			$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage Width	V_{CM}	3		±12	±14		V
Common-Mode Rejection Ratio	CMR	1		70	90		dB
Supply Voltage Rejection Ratio	SVR	1			30	150	μV/V
Power Consumption	P_C	4	$R_L = \infty$		90	170	mW
Slew Rate	SR	5	$R_L \geq 2k\Omega$		2		V/μs
Input Referred Noise Voltage	V_{nI}	6	$R_S = 1k\Omega$, DIN/AUDIO		1.5		μV_{rms}

Test Circuit 1 ($V_{I(offset)}$, I_{IO}, I_{Bias}, G_V, CMR, SVR)

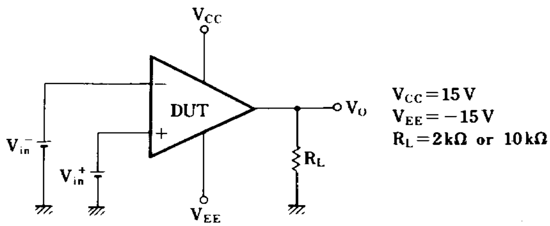


* C_1 and C_2 are capacitors for the prevention of oscillation.

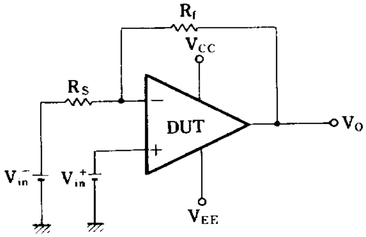
Item	Measurement Conditions
Input Offset Voltage	V_{F1} is measured with the SW_1, and SW_2 set to ON, the SW_3 set to OFF and $E_C=E_K=0V$. Can be given by $V_{1(offset)}=\frac{V_{F1}}{400}(V)$
Input Offset Current	V_{F2} is measured with the SW_1, SW_2 and SW_3 set to OFF, and $E_C=E_K=0V$. Can be given by $I_{IO}=\frac{\lvert V_{F2}-V_{F1}\rvert}{4\times10^6}(A)$
Input Bias Current	V_{F3} is measured with the SW_1 set to ON, the SW_2 set to OFF, the SW_3 set to OFF and $E_C=E_K=0V$. V_{F4} is measured with the SW_1 and SW_2 reversed. Can be given by. $I_{Bias}=\frac{\lvert V_{F3}-V_{F4}\rvert}{8\times10^6}(A)$
Voltage Gain	V_{F5} is measured with the SW_1' SW_2 and SW_3 set to ON, and $E_K=10V$. V_{F5}' is measured with $E_K=-10V$. Can be given by $G_V=20\log\left(\frac{8000}{\lvert V_{F5}-V_{F5}'\rvert}\right)$
Common-Mode Rejection Ratio	V_{F6} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K=0V$ and $E_C=5V$. V_{F6}' is measured with $E_C=-5V$. Can be given by. $CMR=20\log\left(\frac{4000}{\lvert V_{F6}-V_{F6}'\rvert}\right)$
Supply Voltage Rejection Ratio I	V_{F7} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K=E_C=0V$ and $V_{CC}=10V$. Can be given by $SVR(+)=\frac{\lvert V_{F7}-V_{F2}\rvert}{2\times10^3}$
Supply Voltage Rejection Ratio II	V_{F8} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K=E_C=0V$ and $V_{EE}=-10V$. Can be given by $SVR(-)=\frac{\lvert V_{F8}-V_{F2}\rvert}{2\times10^3}$

Note) When not specified in the above table, $V_{CC}=15V$ and $V_{EE}=-15V$.

Test Circuit 2 ($V_{O(max.)}$)



Test Circuit 3 (V_{CM})

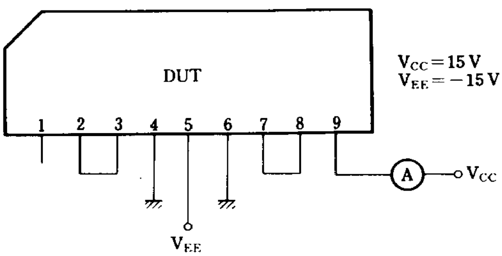


$V_{CC}=15V$
$V_{EE}=-15V$
$R_S=200\Omega$
$R_f=2k\Omega$

Note) Apply a voltage of $|V_{in}^+|>12V$ and check $V_O=V_{in}^+ + \frac{R_f}{R_s}(V_{in}^+ - V_{in}^-)$.

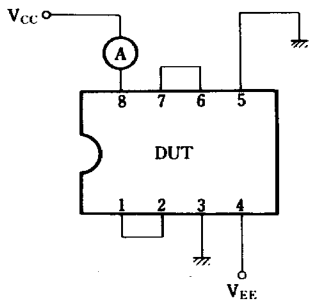
Test Circuit 4 (P_C)

AN6555

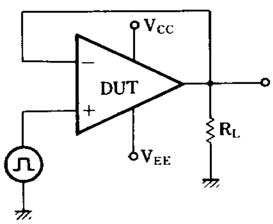


$V_{CC}=15V$
$V_{EE}=-15V$

AN6556, AN6556S

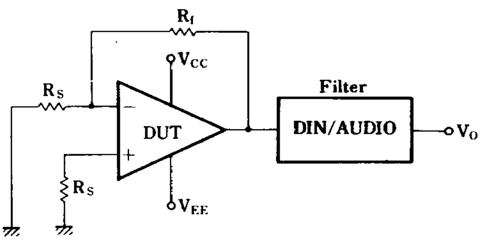


Test Circuit 5 (SR)



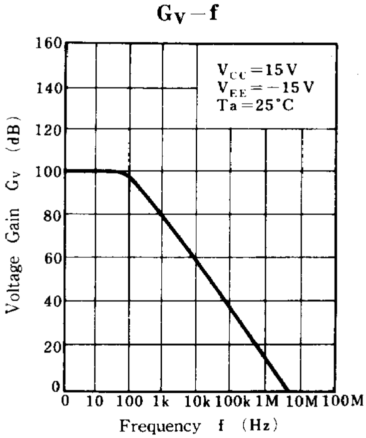
$V_{CC}=15V$
$V_{EE}=-15V$
$R_L=2k\Omega$

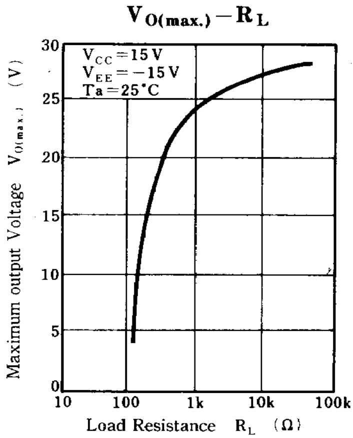
Test Circuit 6 (V_{ni})

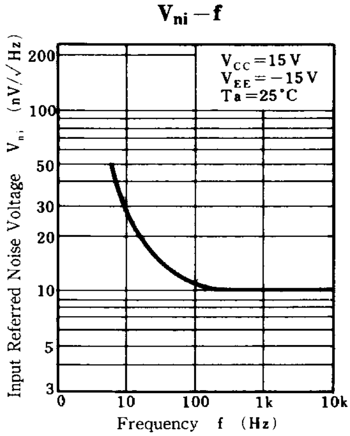


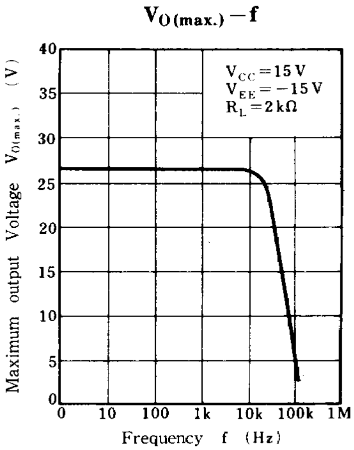
$V_{CC}=15V$
$V_{EE}=-15V$
$R_f=9.1k\Omega$
$R_S=1k\Omega$

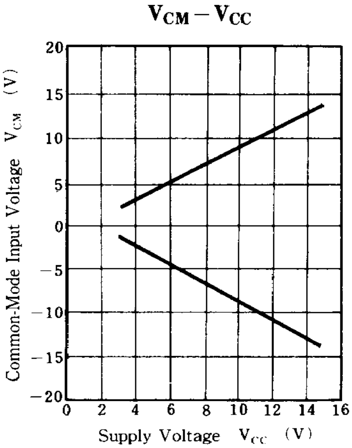
Note) An input referred noise voltage $V_{ni}=\frac{V_O}{(1+R_f/R_s)}$ is given.

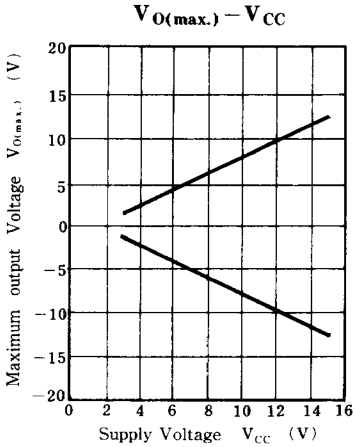

Gv − f
Vcc = 15 V
VEE = −15 V
Ta = 25°C
Voltage Gain Gv (dB)
160
140
120
100
80
60
40
20
0
0 10 100 1k 10k 100k 1M 10M 100M
Frequency f (Hz)

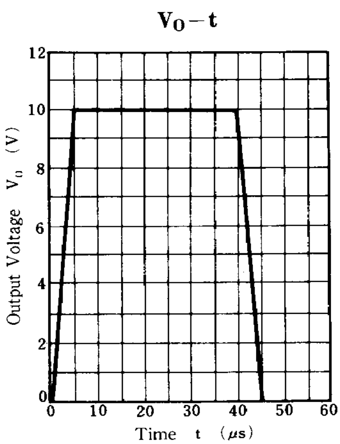

VO(max.) − RL
Vcc = 15 V
VEE = −15 V
Ta = 25°C
Maximum output Voltage VO(max.) (V)
30
25
20
15
10
5
0
10 100 1k 10k 100k
Load Resistance RL (Ω)

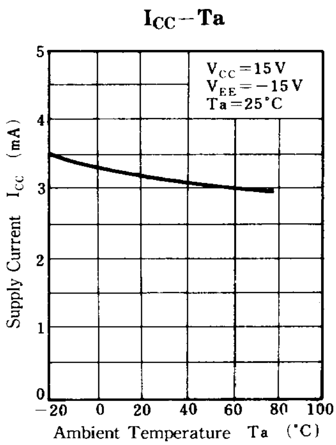

Vni − f
Vcc = 15 V
VEE = −15 V
Ta = 25°C
Input Referred Noise Voltage Vni (nV/√Hz)
200
100
50
30
20
10
5
3
0 10 100 1k 10k
Frequency f (Hz)


VO(max.) − f
Vcc = 15 V
VEE = −15 V
RL = 2 kΩ
Maximum output Voltage VO(max.) (V)
40
35
30
25
20
15
10
5
0
0 10 100 1k 10k 100k 1M
Frequency f (Hz)


VCM − VCC
Common-Mode Input Voltage VCM (V)
20
15
10
5
0
−5
−10
−15
−20
0 2 4 6 8 10 12 14 16
Supply Voltage Vcc (V)


VO(max.) − VCC
Maximum output Voltage VO(max.) (V)
20
15
10
5
0
−5
−10
−15
−20
0 2 4 6 8 10 12 14 16
Supply Voltage Vcc (V)


VO − t
Output Voltage VO (V)
12
10
8
6
4
2
0
0 10 20 30 40 50 60
Time t (μs)


ICC − Ta
Vcc = 15 V
VEE = −15 V
Ta = 25°C
Supply Current Icc (mA)
5
4
3
2
1
0
−20 0 20 40 60 80 100
Ambient Temperature Ta (°C)

■ Application Circuit