

AEIC-7272-S16

Quad Differential Line Driver

Separate Logic Bias and Driver Bias

With Tri-State Outputs



Data Sheet

Description

These line drivers are pin compatible with 26LS31 in applications where pin 4 = 5V and pin 12 = GND. Internal clamp diodes allow trouble-free operation when driving cable lengths exceeding 100m. Split supplies are provided to minimize standby power dissipation in high voltage applications. The logic should be powered from a regulated 5V supply at the VccBias pin. The output stages may then be powered by a separate supply at VccDrivers, up to 30V. Output voltage swings of 0.3V to VCC-1.9V are typical. The outputs are protected against shorts to ground, shorts to Vcc and to other outputs, by a two-fold scheme of current limiting and thermal shutdown. This assures highly reliable operation in harsh environments.

This part is available in 16L SOIC (Pb-free) package.

Applications

- Encoders
- Industrial controls

Features

- Supply (Bias) Voltage Range 3.5 V to 30 V
- Operation to 800 KHz
- CMOS and TTL Compatible Inputs
- Separate logic bias and driver supply pins
- Optional single supply operation for moderate power applications
- High Impedance Buffered Inputs with hysteresis
- Tri-State outputs
- 80 mA peak SINK/SOURCE current

Pin Assignment

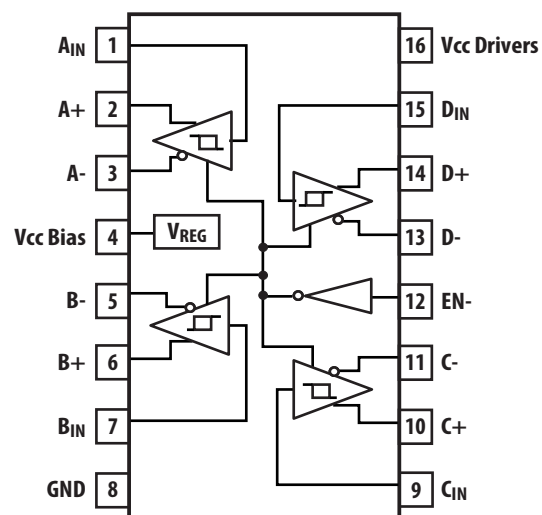


Table 1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Units	Test Conditions
Operating Temperature Range	T _A	-55	125	°C	
Supply (Driver) Voltage Range	V _{CCD}	4.5	30	V	

Table 2. Electrical Characteristics

Unless otherwise specified, T_A = 25° C and EN- < 0.8 V.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Overtmp Operate Point (junction)	T _{JOP}	-	172	-	°C	Note 1
Overtmp Release Point (junction)	T _{JRP}	-	136	-	°C	Note 1
Vcc Bias Voltage Range	V _{CCB}	3.5	5	30	V	
Vcc Drivers Voltage Range	V _{CCD}	4.5	5	30	V	
Supply Current V _{CCB1} (BIAS)	I _{CCB1}	-	11.9	16.0	mA	V _{CCB} and V _{CCD} = 5 V
Supply Current V _{CCD1} (DRIVERS)	I _{CCD1}	-	2.4	3.3	mA	V _{CCB} and V _{CCD} = 5 V
Supply Current V _{CCB2}	I _{CCB2}	-	2.5	3.4	mA	V _{CCB} and V _{CCD} = 5 V, EN- > 2 V
Supply Current V _{CCD2}	I _{CCD2}	-	0.0	0.1	mA	V _{CCB} and V _{CCD} = 5 V, EN- > 2 V
Supply Current V _{CCB3}	I _{CCB3}	-	12.1	18.5	mA	V _{CCB} and V _{CCD} = 30 V
Supply Current V _{CCD3}	I _{CCD3}	-	2.4	3.3	mA	V _{CCB} and V _{CCD} = 30 V
Supply Current V _{CCB4}	I _{CCB4}	-	2.6	3.5	mA	V _{CCB} and V _{CCD} = 30 V, EN- > 2 V
Supply Current V _{CCD4}	I _{CCD4}	-	0.0	0.1	mA	V _{CCB} and V _{CCD} = 30 V, EN- > 2 V
Enable Input Threshold	V _{THE}	0.8	1.5	2	V	
Enable Low Level Input Current	I _{ILE}	-10	0	10	μA	V _{IN} = 0 V, V _{CCB} = 5 V
Enable High Level Input Current	I _{IHE}	-	108	150	μA	V _{IN} = 5 V, V _{CCB} = 5 V
High Impedance Output Leakage	I _{OZ}	-4.0	0.0	4.0	μA	V _{CCD} = 30 V, EN- > 2 V, Output at 15 V
Input Positive-Going Threshold	V _{T+}	1.05	1.25	1.45	V	V _{CCB} = 5 V
Input Negative-Going Threshold	V _{T-}	0.75	0.95	1.15	V	V _{CCB} = 5 V
Input Hysteresis	V _H	-	0.3	-	V	V _{CCB} = 5 V
Low Level Input Current	I _{IL}	-4.0	-0.1	-	μA	V _{IN} = 0 V, V _{CCB} = 5 V
High Level Input Current	I _{IH}	-	0	4.0	μA	V _{IN} = 5 V, V _{CCB} = 5 V
Low Level Output1	V _{OL1}	-	375	500	mV	I _{OL} = 20 mA, V _{CCD} = 5 V
Low Level Output2	V _{OL2}	-	370	500	mV	I _{OL} = 20 mA, V _{CCD} = 30 V
High Level Output1	V _{OH1}	2.4	2.8	-	V	I _{OH} = -20 mA, V _{CCD} = 5 V
High Level Output2	V _{OH2}	27.7	28.1	-	V	I _{OH} = -20 mA, V _{CCD} = 30 V

Note:

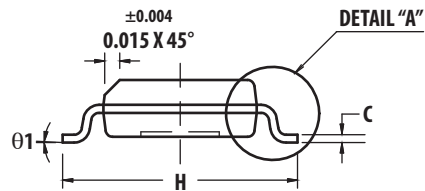
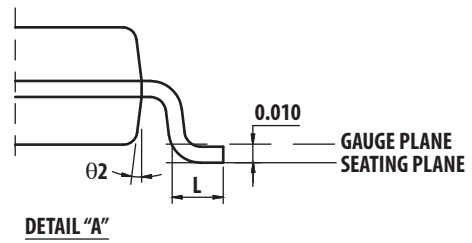
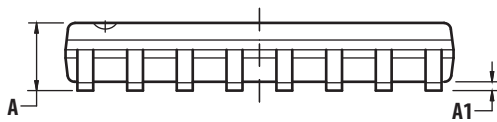
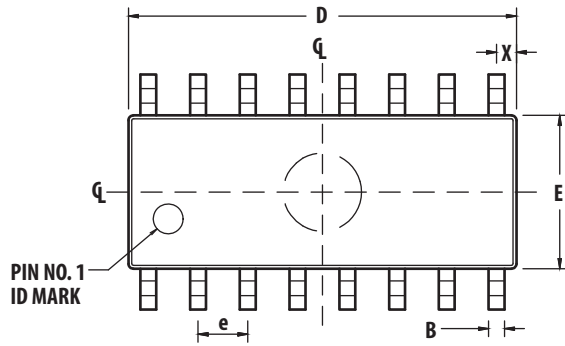
1. This is not a test parameter, but for information only.

Table 3. AC Switching Characteristics

Values given at V_{CCB} = 5 V, V_{CCD} = 24 V, T_A = 25° C, C_L = 1000 pF on all outputs, and EN- < 0.8 V.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay, rising input 50% point to zero crossing of differential outputs	T _{PLH}	-	450	630	ns	See above.
Propagation delay, falling input 50% point to zero crossing of differential outputs	T _{PHL}	-	450	630	ns	See above.
Output Rise Time	T _R	-	700	980	ns	See above.
Output Fall Time	T _F	-	700	980	ns	See above.

Package Drawings (Dimensions in Inches)



Symbol	16 SOIC	
	Min	Max
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.386	0.393
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.020 REF	
$\theta 1$	0°	8°
$\theta 2$	7° BSC	

Notes:

1. Lead coplanarity should be 0 to 0.004" max.
2. Package surface finishing: VD1 24~27 (Dual).
Package surface finishing: VD1 13~15 (16L Soic(NB) Matrix).
3. All dimension excluding mold flashes.
4. The lead width, B to be determined at 0.0075" from the lead tip.

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