GENERAL DESCRIPTION

The SC3500 is a precision clock fan out driver. It requires a 2X frequency clock input from either a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This 2X reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The 20-clock outputs are divided into three groups. The first group of ten (10) outputs are unconditionally at the primary frequency, "Fa" = F input/2. The second group, "Fb", of five outputs can be selected to be either identical to "Fa" or at 1/2 the frequency of "Fa". The third group, "Fc", of five outputs, must be selected to be at either 1/2 or 1/4 of "Fa".

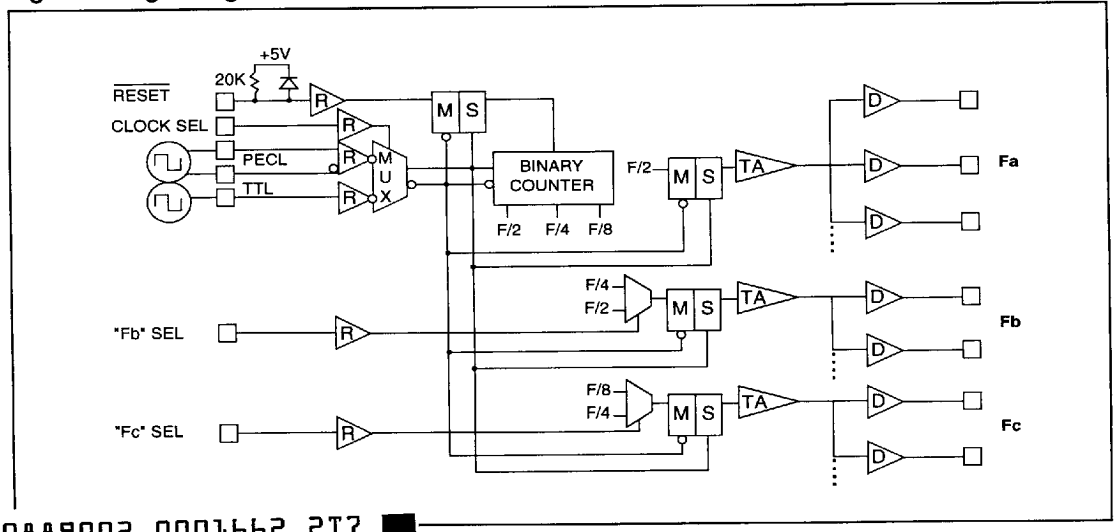
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Twenty (20) clock outputs:**
  - Ten (10) outputs at primary frequency, up to 80 MHz
  - Five (5) outputs at primary or 1/2 primary frequency
  - Five (5) outputs at either 1/2 or 1/4 primary frequency
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground–bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

3

Figure 1. Logic Diagram



0889002 0001662 2T7

Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

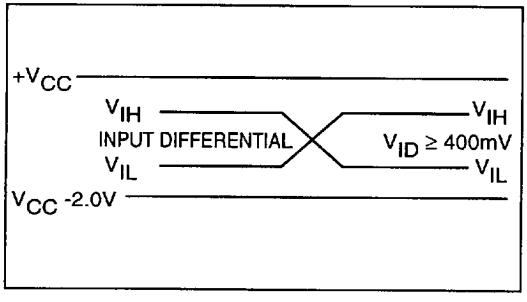
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-11)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL, CSEL, BSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		50	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL, CSEL, BSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 3-9 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3500 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3500 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3500 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

AC Specifications—Using AC Test Circuit (Page 3-11)

V_{CC} = +5.0V ± 5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3500–2	SC3500–1	SC3500	Units
Maximum Skew Across All Outputs	0.5	0.5	1.0	ns
Maximum Skew Chip to Chip	1.0	2.0	—	ns
Maximum Skew Across Fa Outputs	0.25	0.25	0.25	ns
Maximum Skew Across Fb Outputs	0.25	0.25	0.25	ns
Maximum Skew Across Fc Outputs	0.25	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	±1.0	±1.0	±1.0	ns
Maximum TTL Input Frequency	80	80	80	MHz
Maximum PECL Differential Input Frequency	160	160	160	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	ns

Notes:
1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 1.0 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50 ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pf capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip twenty output fan-out device using AMCC's advanced BiCMOS process. This design has optimized the device for clock symmetry and absolute minimum skew across all twenty outputs. Three harmonic clock frequency groups are provided that are user selectable.

For highest performance this approach requires a 2X clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator operating between +5V and ground can provide either differential ECL inputs (referenced to +5V - PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This 2X input clock will be fanned out to a divide down counter and to master-slave flip-flops for synchronization, refer to the logic diagram preceding. Using this methodology the output duty cycle asymmetry becomes largely a function of output driver slew rate into the AC load.

Two user select pins, "B select" and "C select", provide the "Fb" and "Fc" output (sub-harmonic) frequencies by way of multiplexor selection into the final resynchronizing flip-flops. The divide down counter outputs are 50% duty cycle decoded. The output resynchronizing flip-flops are keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source terminated TTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset" — a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following five falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after five falling edge clock inputs, from a high (leading edge) count origin (see "Relative Output Timing", Page 3-10, and "Reset To Output Timing", in Clock Driver Application Note #1).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current.

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Clock Driver Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3500 will exhibit skews less than the specified maximum. A plastic 52 lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Output Clock Frequency Selection

"B" SEL	"C" SEL	XCO FREQ	Fa	Fb	Fc
LO	LO	F	F/2	F/4	F/8
HI	LO	F	F/2	F/2	F/8
LO	HI	F	F/2	F/4	F/4
HI	HI	F	F/2	F/2	F/4

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non–crystal oscillator sources may be used at the user's discretion. See Application Note #1.

Power Management

The overall goal of managing the power dissipated by the SC3500 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3500 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-11 for complete load definition).

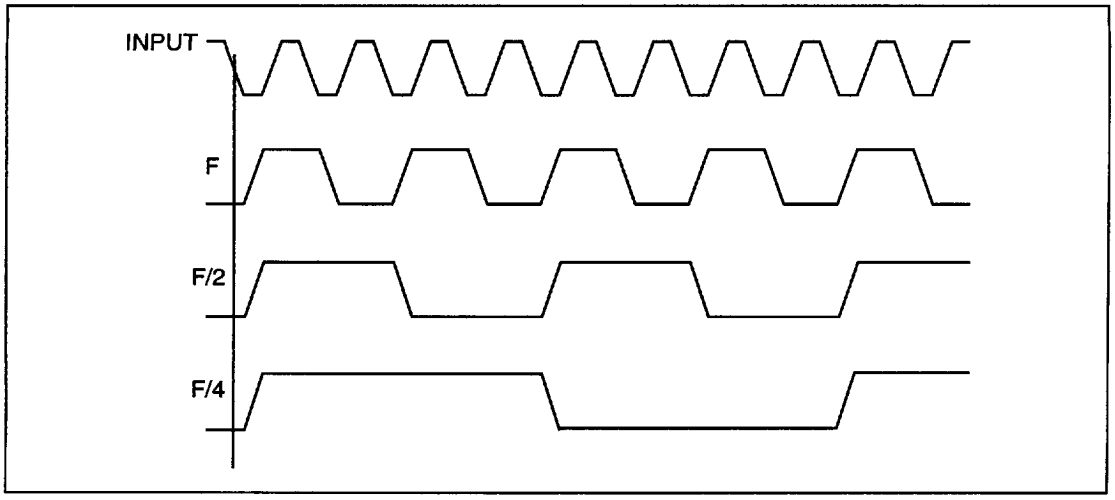
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (400 mW) of the SC3500 to determine the total power being dissipated by the SC3500. This total power is then multiplied by the SC3500's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3500. For greatest reliability, this junction temperature should not exceed 140°C.

	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	50°C/WATT	40°C/WATT	35°C/WATT

For example: You have a SC3500 with 8 of the Fa outputs running at 66 MHz with 10 pF loads (8 x 47 = 376 mW + 2 x 16 = 32 mW for an Fa Total of 408 mW), 3 of the Fb outputs are running at 33 MHz with 5 pF loads (3 x 19 = 57 mW + 2 x 12 = 24 mW for an Fb Total of 81 mW), and 2 Fc outputs running at 33 MHz with 15 pF loads (2 x 24 = 48 mW + 3 x 12 = 36 mW for an Fc Total of 84 mW). The Total Chip Power is Core Power (400 mW) + Fa Power (408 mW) + Fb Power (81 mW) + Fc Power (84 mW) = 973 mW. Your design calls for a 70°C Still Air ambient. The SC3500's junction temperature would then be: 70°C + (.973 Watts x 50°C/Watt = 49°C) = 119°C, below the 140°C maximum.

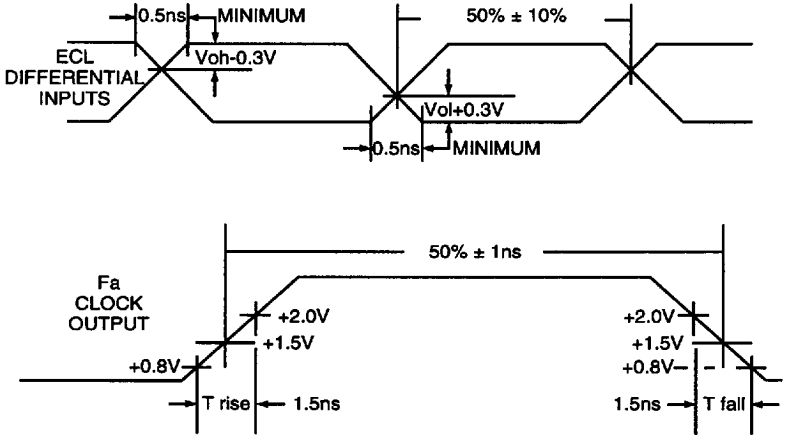
Relative Output Timing



Symmetry

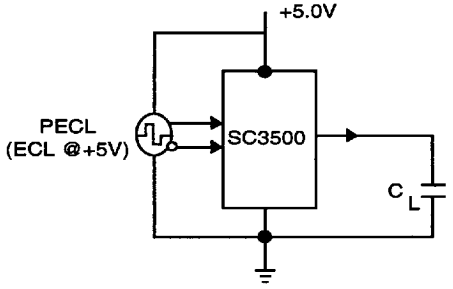
The outputs of the SC3500 are nominally centered to provide a clean 50% duty cycle, symmetrical waveform at the +1.5V threshold reference. (See Threshold Crossing Characteristics diagram below for the conditions.)

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

AC Test Circuit



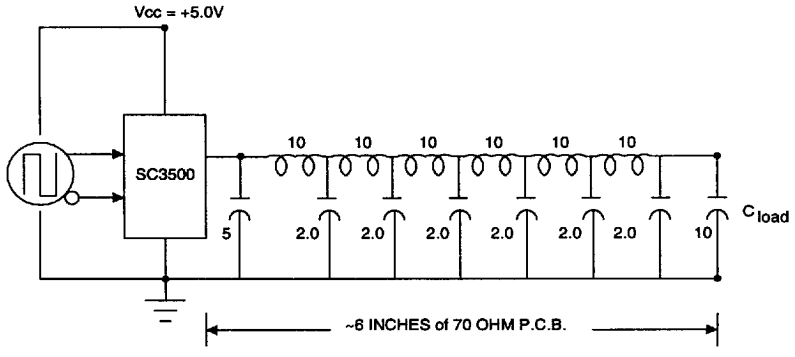
Designing the SC3500 for "Real Loads"

While the AC Test Circuit presented above can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3500 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3500 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz.

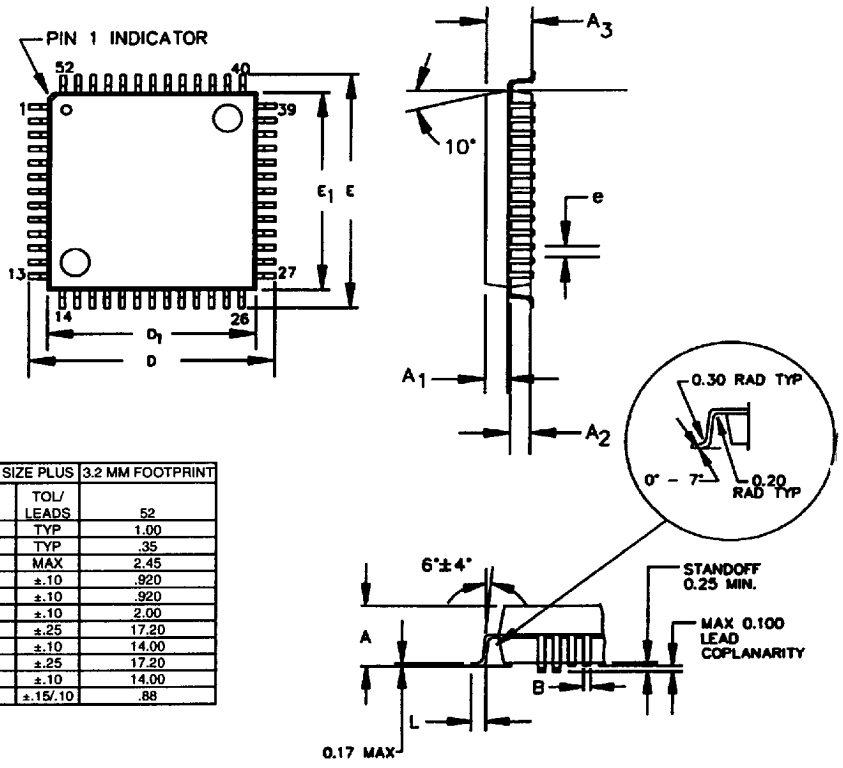
Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

52-Pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT	
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	$\overline{\text{RESET}}$	14	CSEL	27	NC	40	TTL OSC
2	GND	15	GND	28	NC	41	GND
3	FB4	16	FA0	29	FC0	42	FA9
4	GND	17	VCC	30	GND	43	VCC
5	FB3	18	FA1	31	FC1	44	FA8
6	VCC	19	GND	32	VCC	45	GND
7	FB2	20	FA2	33	FC2	46	FA7
8	GND	21	VCC	34	GND	47	VCC
9	FB1	22	FA3	35	FC3	48	FA6
10	VCC	23	GND	36	VCC	49	GND
11	FB0	24	FA4	37	FC4	50	FA5
12	VCC	25	VCC	38	PECL OSCN	51	VCC
13	BSEL	26	NC	39	PECL OSCP	52	CLK SEL

Ordering Information

Package Type	Max Skew Across All Outputs	Max Skew Chip-to-Chip	Part Number
52 Lead Quad Flat Pack	0.5 ns	1.0 ns	SC3500Q-2
52 Lead Quad Flat Pack	0.5 ns		SC3500Q–1
52 Lead Quad Flat Pack	1.0 ns		SC3500Q