IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

BT151X-650C

SCR

16 March 2014 Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance.

2. Features and benefits

- High bidirectional blocking voltage capability
- High thermal cycling performance
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability

3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

4. Quick reference data

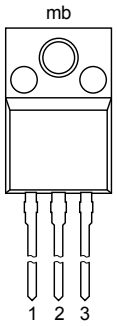
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	650	V
V_{RRM}	repetitive peak reverse voltage			-	-	650	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	100	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 69$ °C; Fig. 1; Fig. 2; Fig. 3		-	-	12	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	2	15	mA

Scan or click this QR code to view the latest information for this product

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 TO-220F (SOT186A)	
2	A	anode		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT151X-650C	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	650	V
V_{RRM}	repetitive peak reverse voltage			-	650	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq 69$ °C		-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 69$ °C; Fig. 1; Fig. 2; Fig. 3		-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	100	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	110	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	50	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	2	A

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

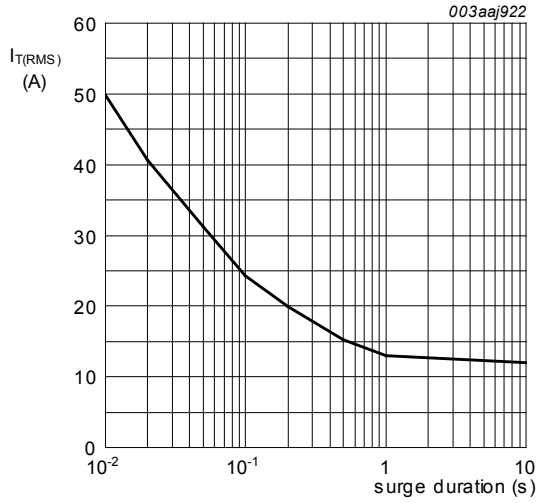


Fig. 1. RMS on-state current as a function of surge duration; maximum values

$f = 50\ Hz;\quad T_h = 69\ °C$

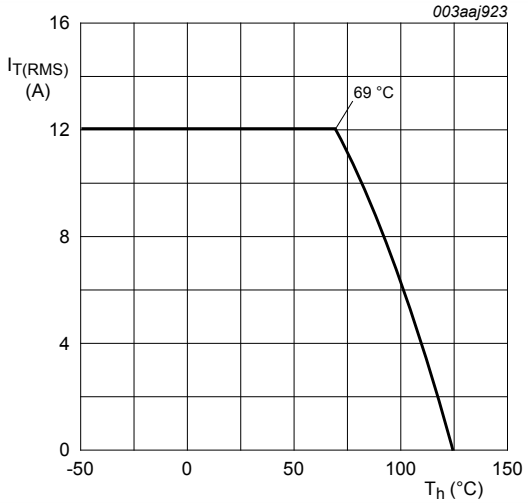


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values

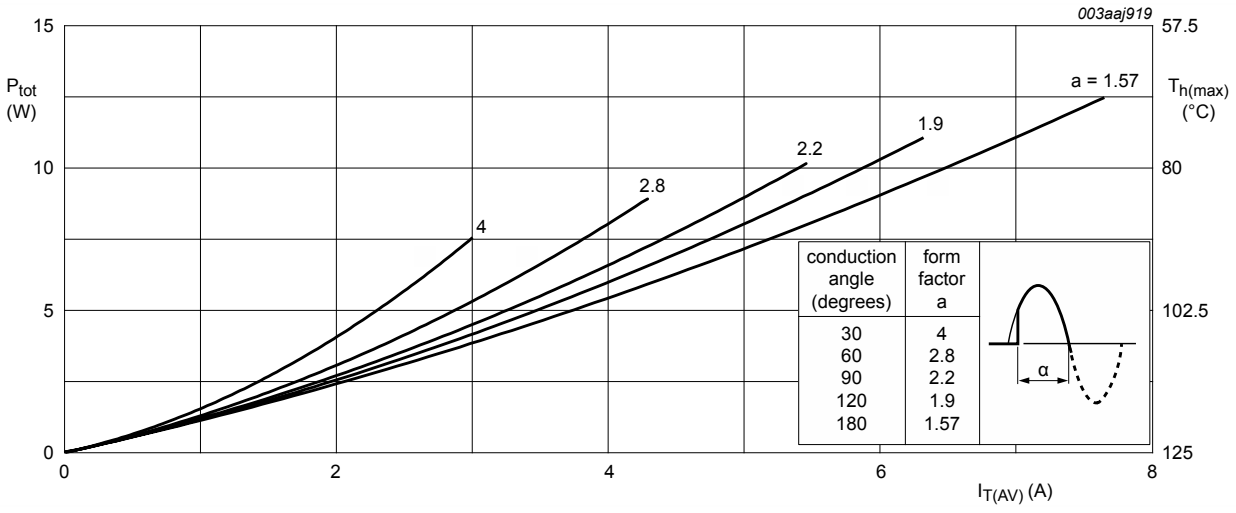


Fig. 3. Total power dissipation as a function of average on-state current; maximum values

α = conduction angle a = form factor = $I_{T(RMS)} / I_{T(AV)}$

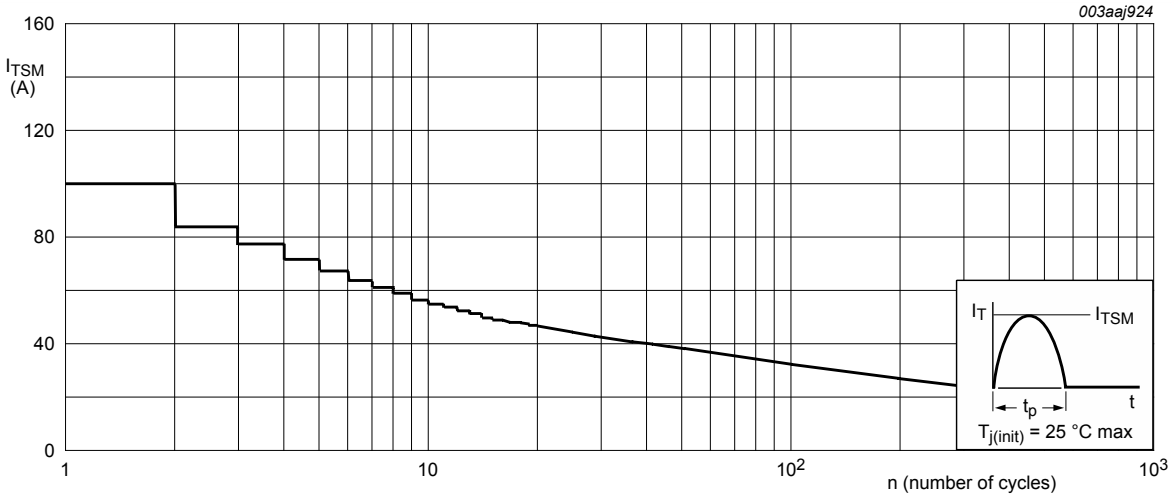


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

f = 50 Hz

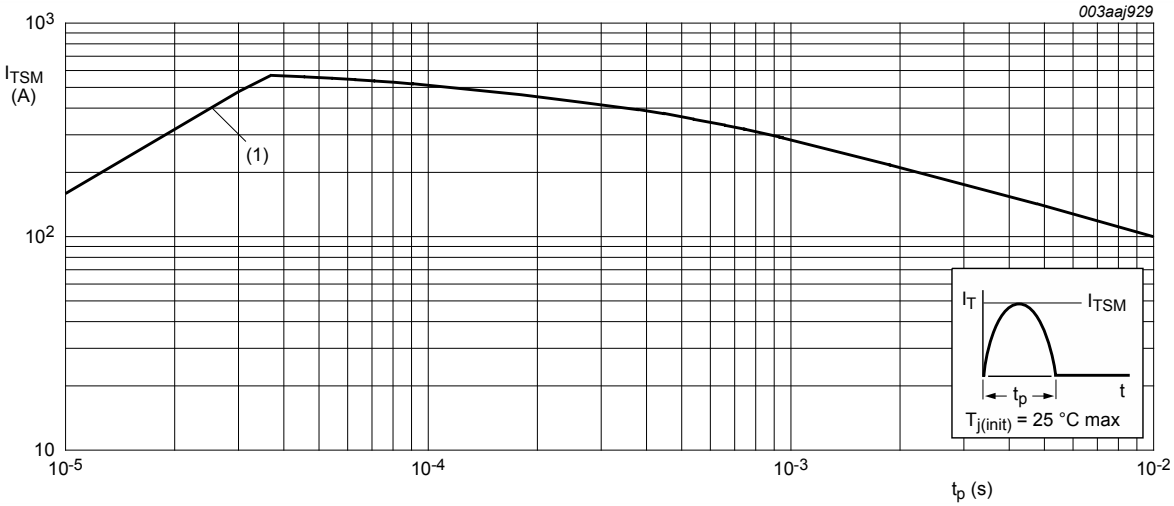


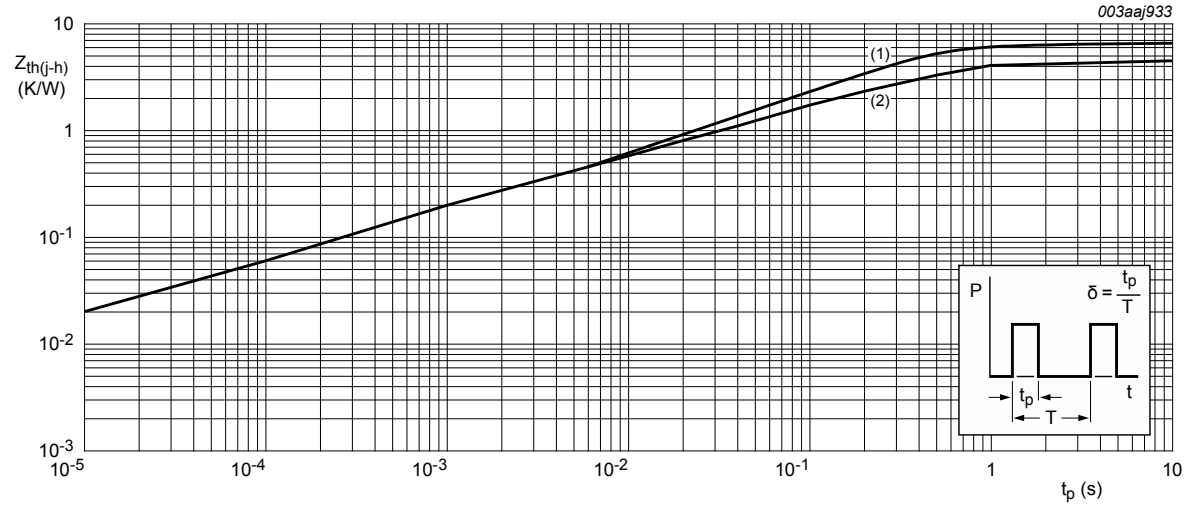
Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

$t_p \leq 10$ ms; (1) dI_T/dt limit

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6		-	-	4.5	K/W
		without heatsink compound; Fig. 6		-	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	55	-	K/W



(1) Without heatsink compound
(2) With heatsink compound

Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse width

9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from anode to external heatsink; f = 1 MHz; T_h = 25 °C		-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	2	15	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	10	40	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	7	20	mA
V_T	on-state voltage	I_T = 23 A; T_j = 25 °C; Fig. 10		-	1.4	1.75	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.6	1	V
		V_D = 650 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.25	0.4	-	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_D	off-state current	V_D = 650 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 650 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 436 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		200	1000	-	V/µs
		V_{DM} = 436 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		50	130	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 650 V; I_G = 100 mA; dI_G/dt = 5 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 436 V; T_j = 125 °C; I_{TM} = 20 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM})		-	70	-	µs

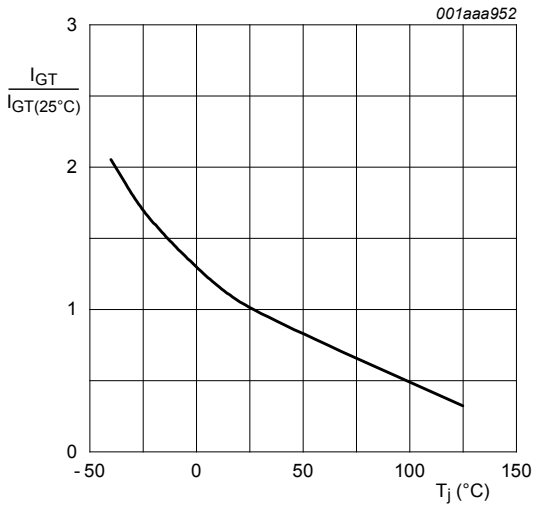


Fig. 7. Normalized gate trigger current as a function of junction temperature

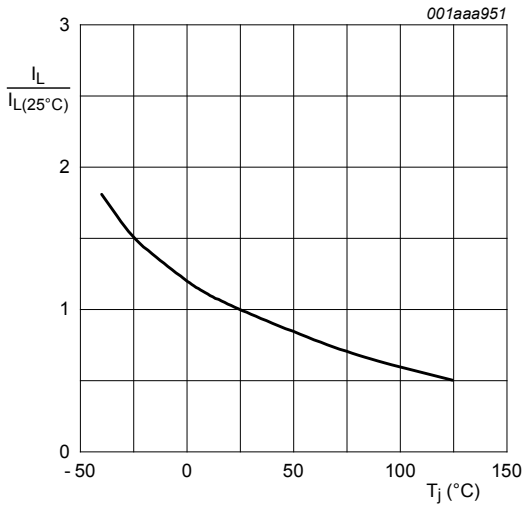


Fig. 8. Normalized latching current as a function of junction temperature

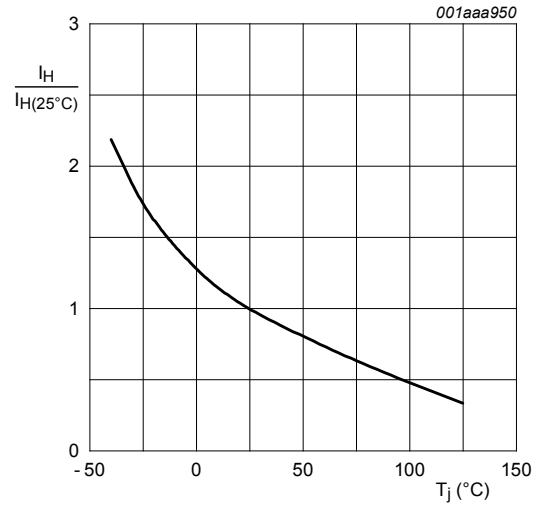
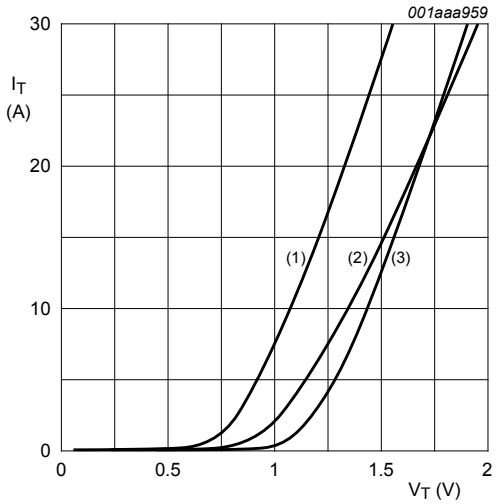


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.06 V; R_s = 0.0304 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

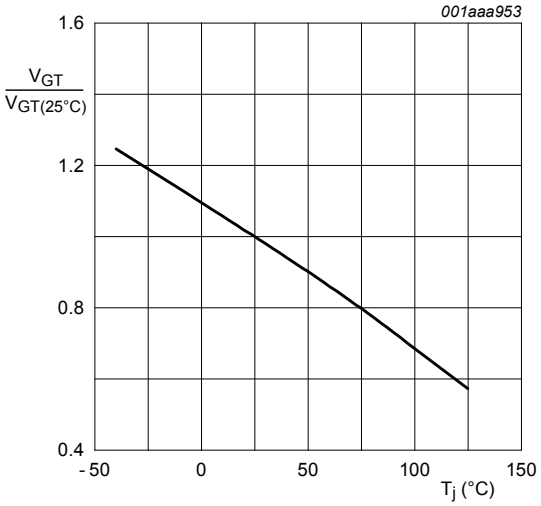
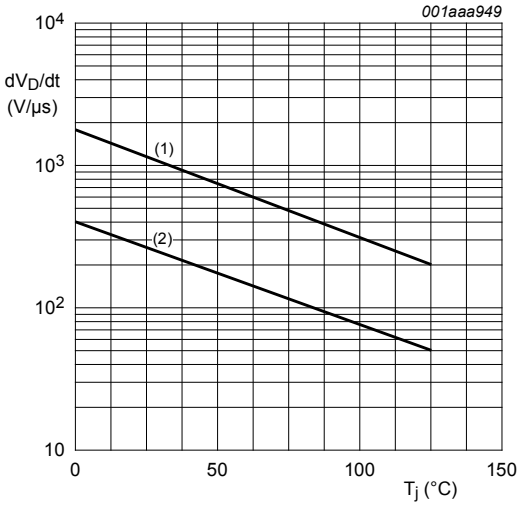


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



(1) R_{GK} = 100 Ω;

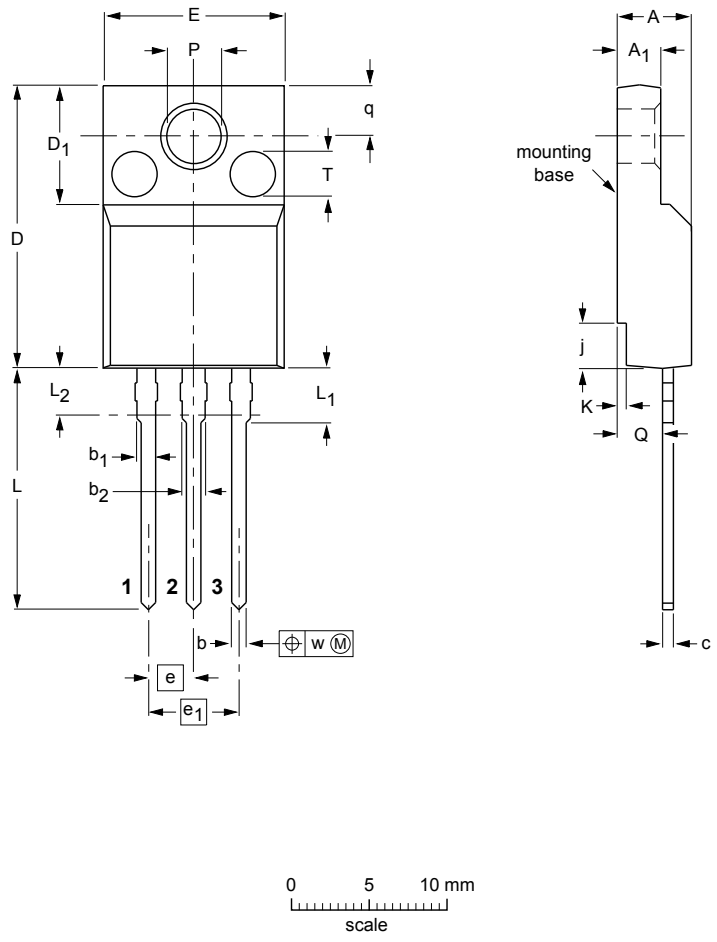
(2) gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

11. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are # 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-04-09~~ 06-02-14

Fig. 13. Package outline TO-220F (SOT186A)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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