

DS90LV001 800 Mbps LVDS Buffer

Check for Samples: [DS90LV001](#)

FEATURES

- Single +3.3 V Supply
- LVDS Receiver Inputs Accept LVPECL Signals
- TRI-STATE Outputs
- Receiver Input Threshold $< \pm 100$ mV
- Fast Propagation Delay of 1.4 ns (Typ)
- Low Jitter 800 Mbps Fully Differential Data Path
- 100 ps (Typ) of pk-pk Jitter with PRBS = $2^{23}-1$ Data Pattern at 800 Mbps
- Compatible with ANSI/TIA/EIA-644-A LVDS Standard
- 8 pin SOIC and Space Saving (70%) WSON Package
- Industrial Temperature Range

DESCRIPTION

The DS90LV001 LVDS-LVDS Buffer takes an LVDS input signal and provides an LVDS output signal. In many large systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns often make it difficult to make the stubs as short as the designer would like.

The DS90LV001, available in the WSON package, will allow the receiver to be placed very close to the main transmission line, thus improving system performance.

A wide input dynamic range will allow the DS90LV001 to receive differential signals from LVPECL as well as LVDS sources. This will allow the device to also fill the role of an LVPECL-LVDS translator.

An output enable pin is provided, which allows the user to place the LVDS output in TRI-STATE.

The DS90LV001 is offered in two package options, an 8 pin WSON and SOIC.

Connection Diagram

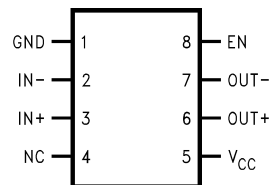
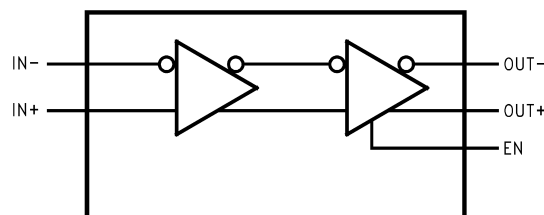


Figure 1. Top View
See Package Number D (R-PDSO-G8), NGK0008A

Block Diagram



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Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})		-0.3V to +4V
LVCMOS/LVTTL Input Voltage (EN)		-0.3V to ($V_{CC} + 0.3V$)
LVDS Receiver Input Voltage (IN+, IN-)		-0.3V to +4V
LVDS Driver Output Voltage (OUT+, OUT-)		-0.3V to +4V
LVDS Output Short Circuit Current		Continuous
Junction Temperature		+150°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature Range Soldering (4 sec.)		+260°C
Maximum Package Power Dissipation at 25°C	D Package	726 mW
	Derate D Package	5.8 mW/°C above +25°C
	NGK Package	2.44 W
	Derate NGK Package	19.49 mW/°C above +25°C
ESD Ratings	(HBM, 1.5k Ω , 100pF)	$\geq 2.5kV$
	(EIAJ, 0 Ω , 200pF)	$\geq 250V$

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Input Voltage	0		V_{CC}	V
Operating Free Air Temperature	-40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
LVCMOS/LVTTL DC SPECIFICATIONS (EN)							
V _{IH}	High Level Input Voltage		2.0		V _{CC}	V	
V _{IL}	Low Level Input Voltage		GND		0.8	V	
I _{IH}	High Level Input Current	V _{IN} = 3.6V or 2.0V, V _{CC} = 3.6V		+7	+20	μA	
I _{IL}	Low Level Input Current	V _{IN} = GND or 0.8V, V _{CC} = 3.6V		±1	±10	μA	
V _{CL}	Input Clamp Voltage	I _{CL} = -18 mA		-0.6	-1.5	V	
LVDS OUTPUT DC SPECIFICATIONS (OUT)							
V _{OD}	Differential Output Voltage	R _L = 100Ω	250	325	450	mV	
ΔV _{OD}	Change in Magnitude of V _{OD} for Complimentary Output States	Figure 2 and Figure 3			20	mV	
V _{OS}	Offset Voltage	R _L = 100Ω	1.080	1.19	1.375	V	
ΔV _{OS}	Change in Magnitude of V _{OS} for Complimentary Output States	Figure 2			20	mV	
I _{OZ}	Output TRI-STATE Current	EN = 0V, V _{OUT} = V _{CC} or GND		±1	±10	μA	
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0V, V _{OUT} = 3.6V or GND		±1	±10	μA	
I _{OS}	Output Short Circuit Current ⁽³⁾	EN = V _{CC} , V _{OUT+} and V _{OUT-} = 0V		-16	-24	mA	
I _{OSD}	Differential Output Short Circuit Current ⁽³⁾	EN = V _{CC} , V _{OD} = 0V		-7	-12	mA	
LVDS RECEIVER DC SPECIFICATIONS (IN)							
V _{TH}	Differential Input High Threshold	V _{CM} = +0.05V, +1.2V or +3.25V		0	+100	mV	
V _{TL}	Differential Input Low Threshold		-100	0		mV	
V _{CMR}	Common Mode Voltage Range	V _{ID} = 100mV, V _{CC} = 3.3V	0.05		3.25	V	
I _{IN}	Input Current	V _{IN} = +3.0V	V _{CC} = 3.6V or 0V		±1	±10	μA
		V _{IN} = 0V			±1	±10	μA
ΔI _{IN}	Change in Magnitude of I _{IN}	V _{IN} = +3.0V	V _{CC} = 3.6V or 0V		1	6	μA
		V _{IN} = 0V			1	6	μA
SUPPLY CURRENT							
I _{CCD}	Total Supply Current	EN = V _{CC} , R _L = 100Ω, C _L = 5 pF		47	70	mA	
I _{CCZ}	TRI-STATE Supply Current	EN = 0V		22	35	mA	

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
- (2) All typical are given for V_{CC} = +3.3V and T_A = +25°C, unless otherwise stated.
- (3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, $C_L = 5pF$ Figure 4 and Figure 5	1.0	1.4	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	1.4	2.0	ns
t_{SKD1}	Pulse Skew $ t_{PLHD} - t_{PHLD} $ ⁽²⁾⁽³⁾			20	200	ps
t_{SKD3}	Part to Part Skew ⁽²⁾⁽⁴⁾			0	60	ps
t_{SKD4}	Part to Part Skew ⁽²⁾⁽⁵⁾				400	ps
t_{LHT}	Rise Time ⁽²⁾	$R_L = 100\Omega$, $C_L = 5pF$ Figure 4 and Figure 6	200	320	450	ps
t_{HLT}	Fall Time ⁽²⁾		200	310	450	ps
t_{PHZ}	Disable Time (Active High to Z)	$R_L = 100\Omega$, $C_L = 5pF$ Figure 7 and Figure 8		3	25	ns
t_{PLZ}	Disable Time (Active Low to Z)			3	25	ns
t_{PZH}	Enable Time (Z to Active High)			25	45	ns
t_{PZL}	Enable Time (Z to Active Low)			25	45	ns
t_{DJ}	LVDS Data Jitter, Deterministic (Peak-to-Peak) ⁽⁶⁾	$V_{ID} = 300mV$; PRBS = $2^{23} - 1$ data; $V_{CM} = 1.2V$ at 800Mbps (NRZ)		100	135	ps
t_{RJ}	LVDS Clock Jitter, Random ⁽⁶⁾	$V_{ID} = 300mV$; $V_{CM} = 1.2V$ at 400MHz clock		2.2	3.5	ps

- (1) All typical are given for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise stated.
- (2) The parameters are ensured by design. The limits are based on statistical analysis of the device performance over the PVT (process, voltage and temperature) range.
- (3) t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (4) t_{SKD3} , Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within $5^\circ C$ of each other within the operating temperature range.
- (5) t_{SKD4} , Part to Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as $|Max - Min|$ differential propagation delay.
- (6) The parameters are ensured by design. The limits are based on statistical analysis of the device performance over the PVT range with the following test equipment setup: HP8133A (pattern pulse generator), 5 feet of RG142B cable with DUT test board and HP83480A (digital scope mainframe) with HP83484A (50GHz scope module). The HP8133A with RG142B cable exhibit a $t_{DJ} = 21ps$ and $t_{RJ} = 1.8ps$.

DC Test Circuits

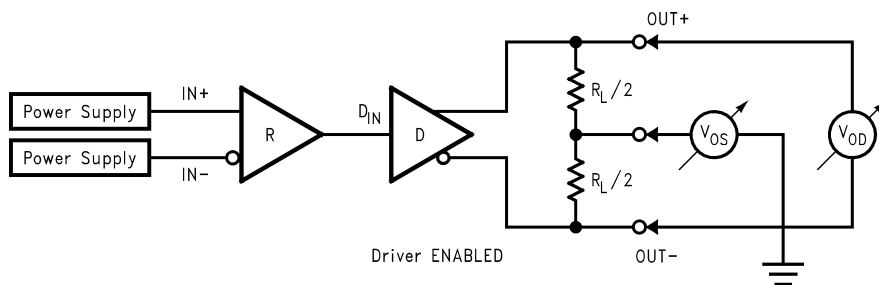


Figure 2. Differential Driver DC Test Circuit

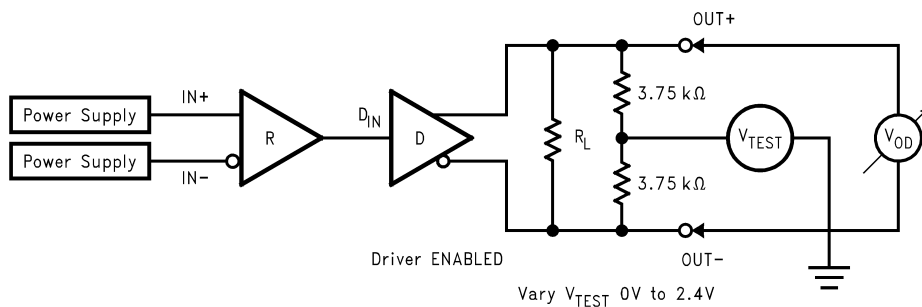


Figure 3. Differential Driver Full Load DC Test Circuit

AC Test Circuits and Timing Diagrams

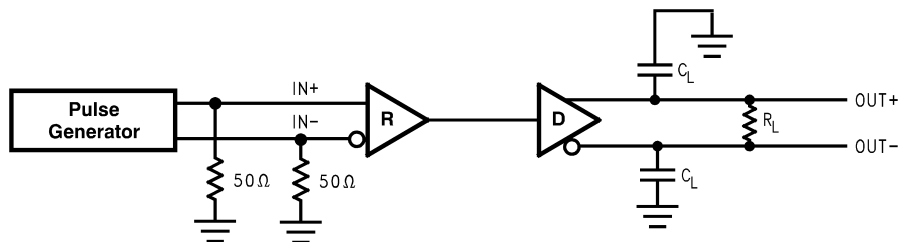


Figure 4. LVDS Output Load

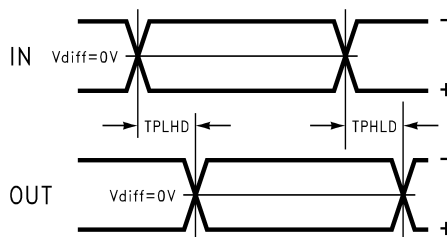


Figure 5. Propagation Delay Low-to-High and High-to-Low

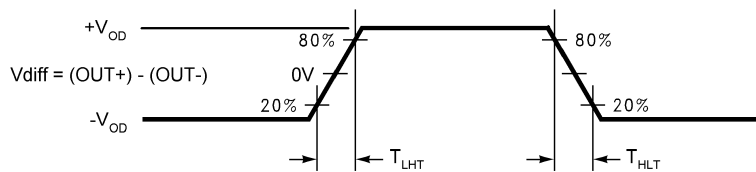


Figure 6. LVDS Output Transition Time

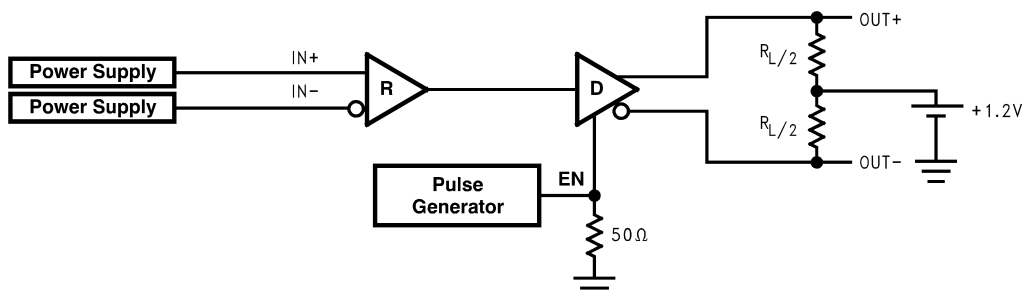


Figure 7. TRI-STATE Delay Test Circuit

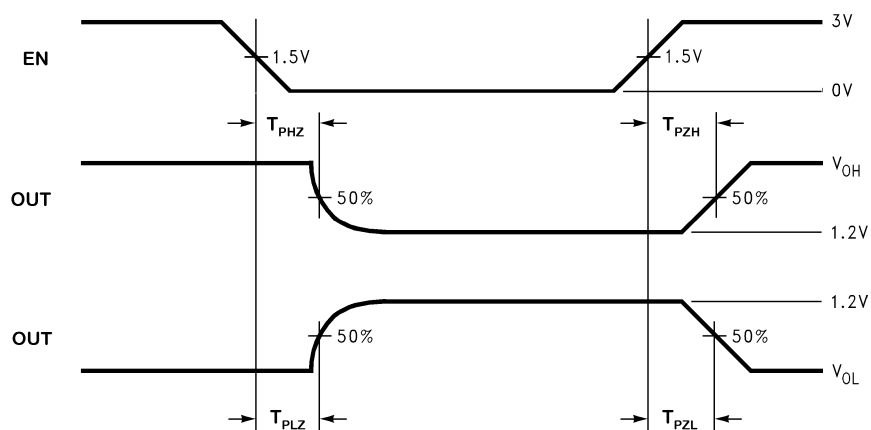


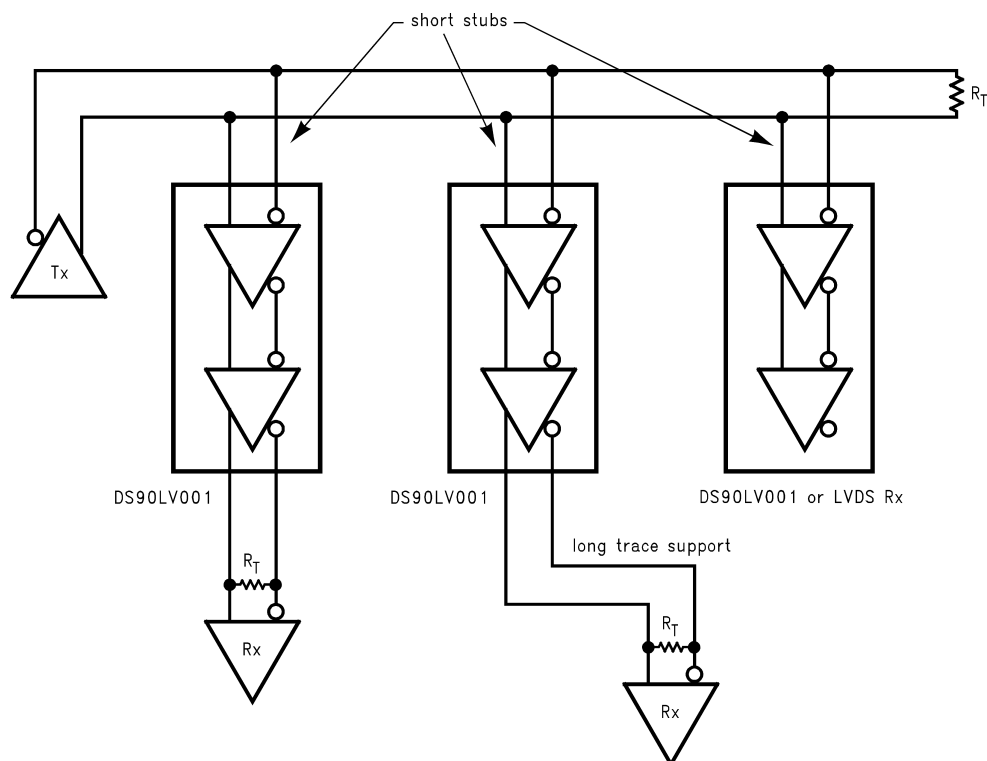
Figure 8. Output active to TRI-STATE and TRI-STATE to active output time

DS90LV001 Pin Descriptions (SOIC and WSON)

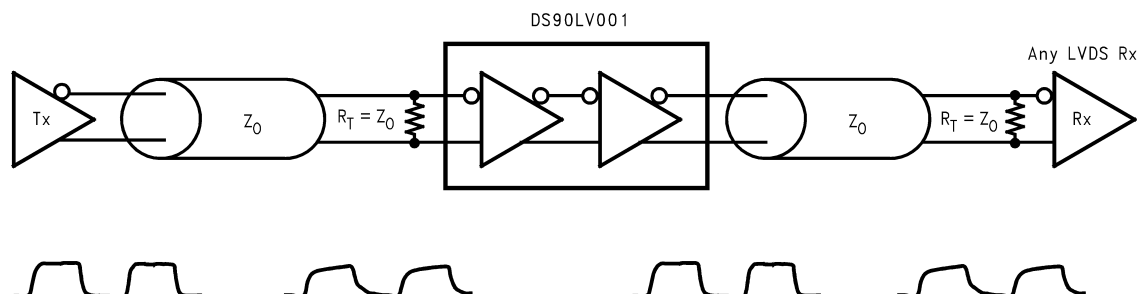
Pin Name	Pin #	Input/Output	Description
GND	1	P	Ground
IN -	2	I	Inverting receiver LVDS input pin
IN+	3	I	Non-inverting receiver LVDS input pin
NC	4		No Connect
V _{CC}	5	P	Power Supply, 3.3V ± 0.3V.
OUT+	6	O	Non-inverting driver LVDS output pin
OUT -	7	O	Inverting driver LVDS output pin
EN	8	I	Enable pin. When EN is LOW, the driver is disabled and the LVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTL levels.
DAP	NA	NA	Die Attach Pad or DAP (WSON Package only). The DAP is NOT connected to the device GND nor any other pin. It is still recommended to connect the DAP to a GND plane of a PCB for enhanced heat dissipation.

TYPICAL APPLICATIONS

Backplane Stub-Hider Application



Cable Repeater Application



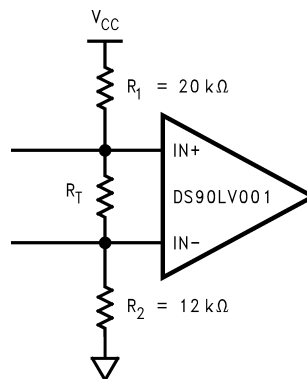
APPLICATION INFORMATION

MODE OF OPERATION

The DS90LV001 can be used as a "stub-hider." In many systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on the individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns and PCB designs often make it difficult to make the stubs as short as the designer would like. The DS90LV001, available in the WSON package, can improve system performance by allowing the receiver to be placed very close to the main transmission line either on the backplane itself or very close to the connector on the card. Longer traces to the LVDS receiver may be placed after the DS90LV001. This very small WSON package is a 75% space savings over the SOIC package.

INPUT FAILSAFE

The receiver inputs of the DS90LV001 do not have internal failsafe biasing. For point-to-point and multidrop applications with a single source, failsafe biasing may not be required. When the driver is off, the link is in-active. If failsafe biasing is required, this can be accomplished with external high value resistors. Using the equations in the LVDS Owner's Manual Chapter 4, the IN+ should be pull to V_{CC} (3.3V) with 20k Ω and the IN- should be pull to GND with 12k Ω . This provides a slight positive differential bias, and sets a known HIGH state on the link with a minimum amount of distortion.



PCB LAYOUT AND POWER SYSTEM BYPASS

Circuit board layout and stack-up for the DS90LV001 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 μ F to 0.1 μ F. Tantalum capacitors may be in the range 2.2 μ F to 10 μ F. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the DS90LV001 as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

There are more common practices which should be followed when designing PCBs for LVDS signaling. Please see application note [AN-1108](#) for guidelines. In addition, application note [AN-1187](#) has additional information specifically related to WSON recommendations.

Typical Performance Curves

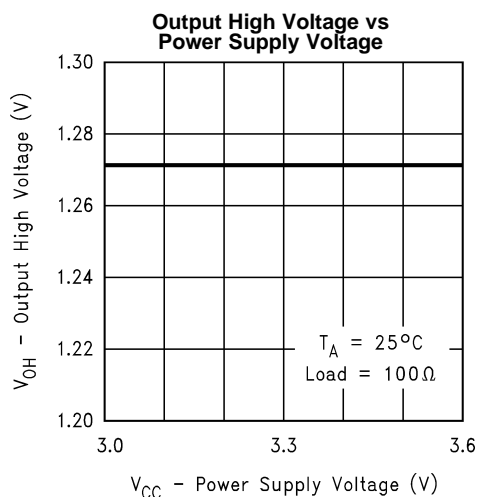


Figure 9.

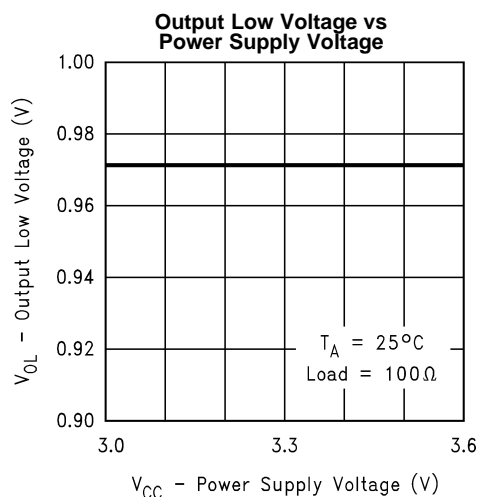


Figure 10.

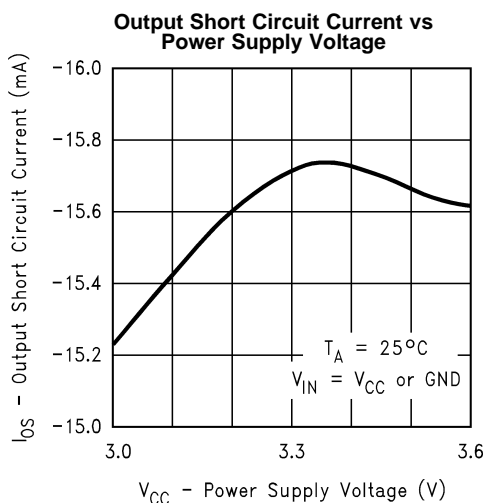


Figure 11.

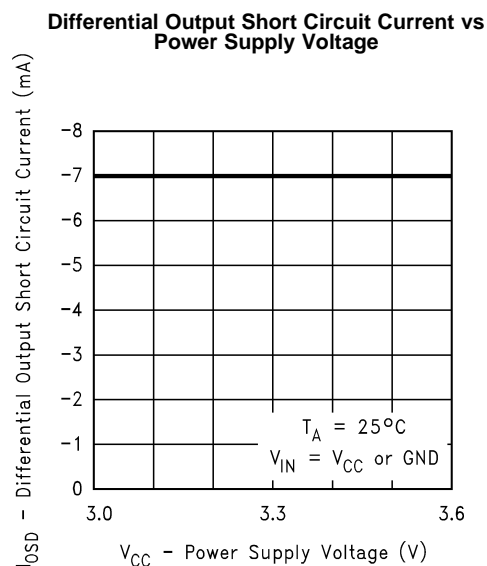


Figure 12.

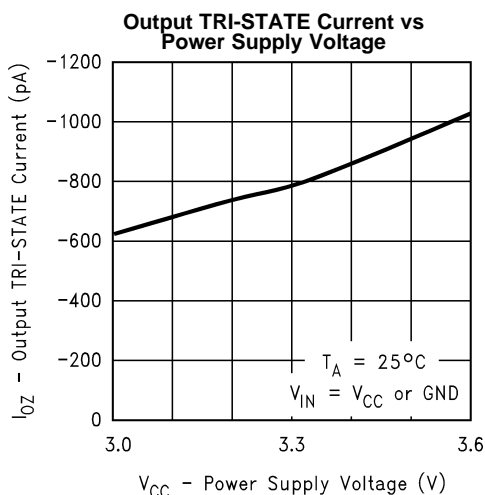


Figure 13.

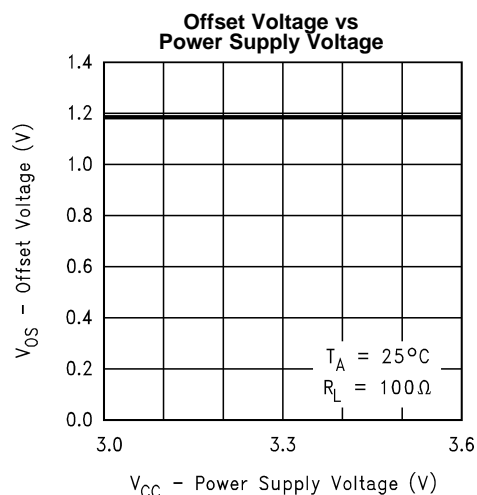


Figure 14.

Typical Performance Curves (continued)

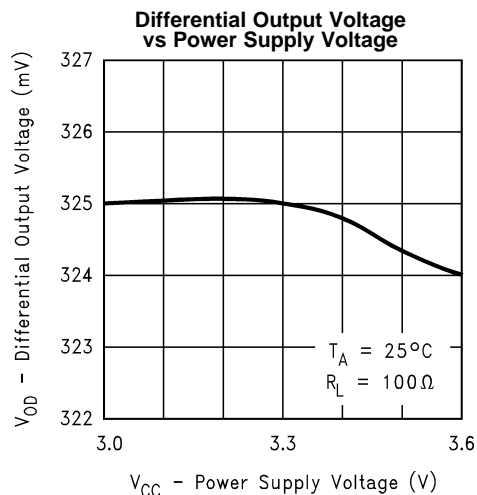


Figure 15.

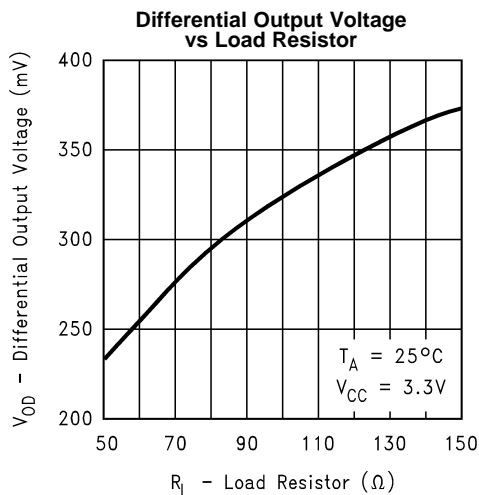


Figure 16.

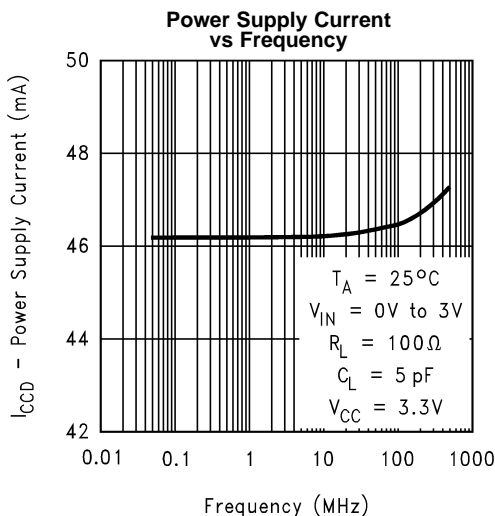


Figure 17.

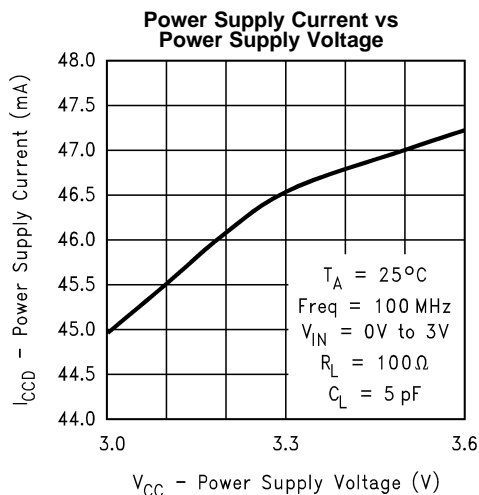


Figure 18.

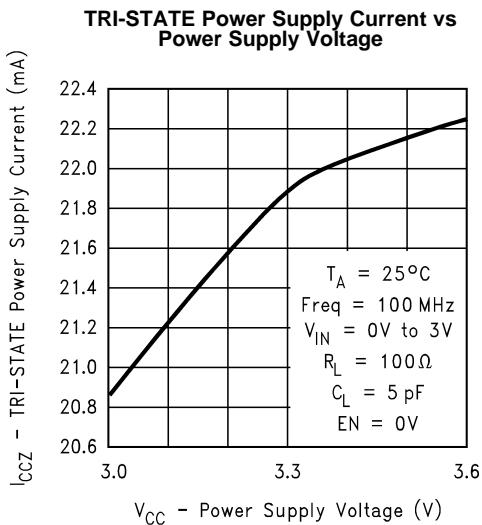


Figure 19.

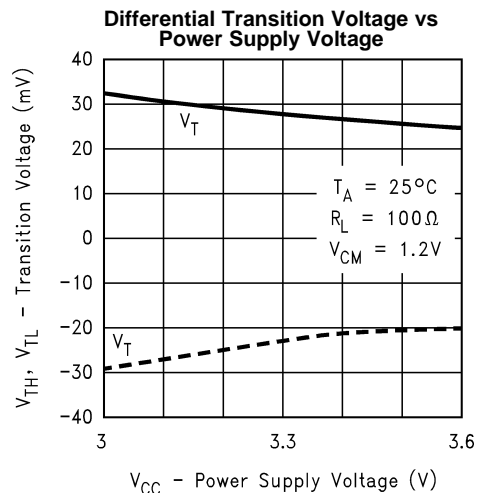


Figure 20.

Typical Performance Curves (continued)

**Differential Propagation Delay vs
Power Supply Voltage**

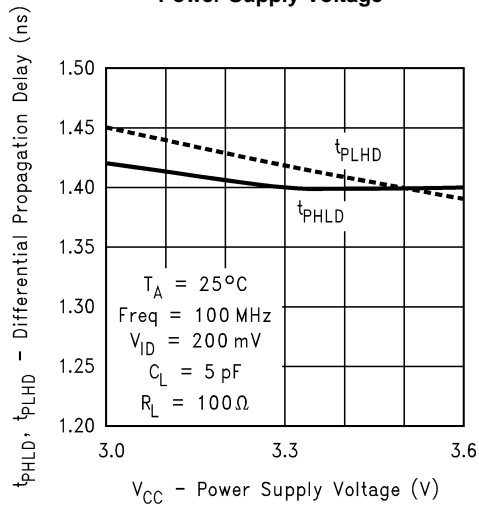


Figure 21.

**Differential Propagation Delay vs
Ambient Temperature**

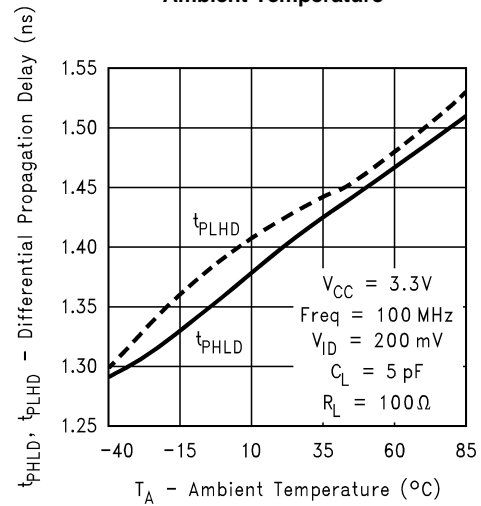


Figure 22.

**Differential Skew vs
Power Supply Voltage**

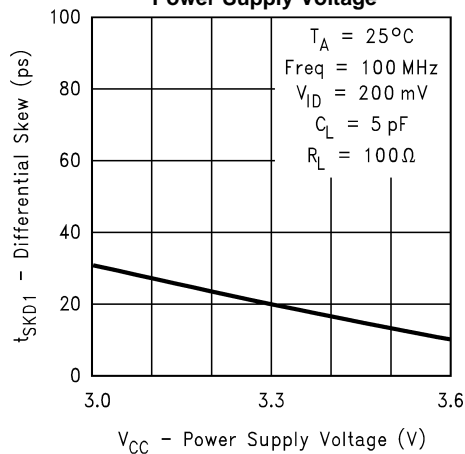


Figure 23.

**Differential Skew vs
Ambient Temperature**

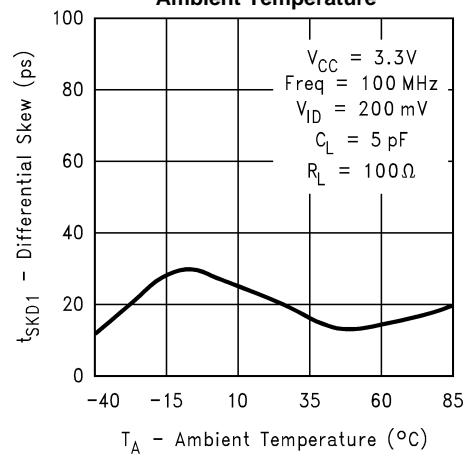


Figure 24.

**Transition Time vs
Power Supply Voltage**

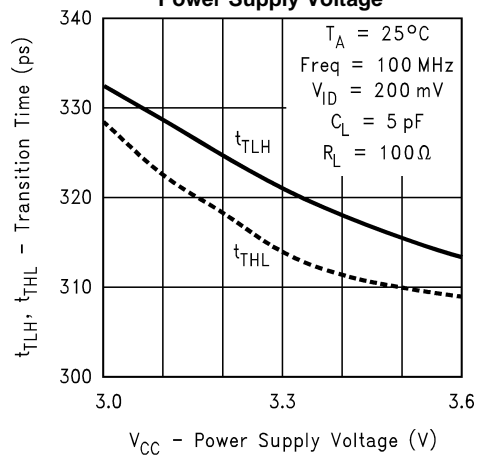


Figure 25.

**Transition Time vs
Ambient Temperature**

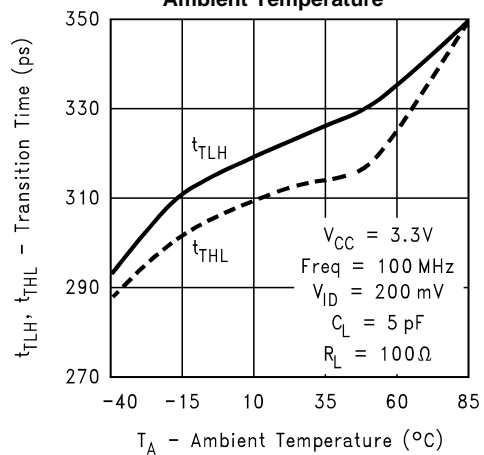


Figure 26.

Typical Performance Curves (continued)

**Differential Propagation Delay vs
Differential Input Voltage**

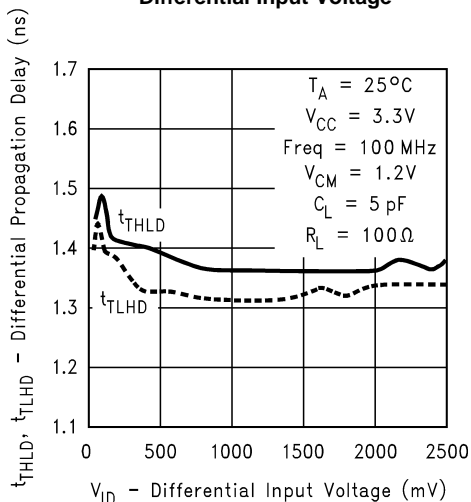


Figure 27.

**Differential Propagation Delay vs
Common-Mode Voltage**

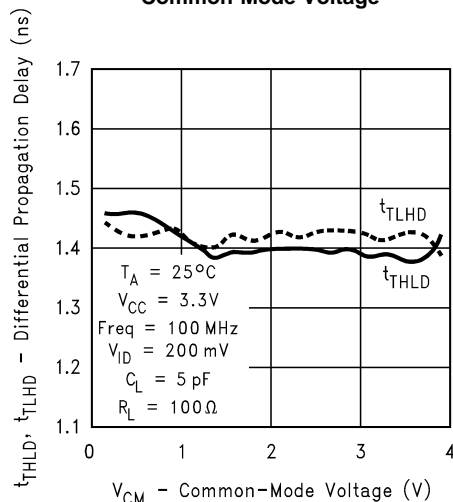


Figure 28.

**Peak-to-Peak Output Jitter at $V_{CM} = 0.4\text{V}$ vs
Differential Input Voltage**

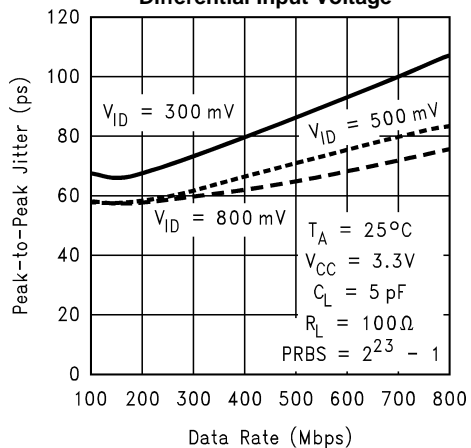


Figure 29.

**Peak-to-Peak Output Jitter at $V_{CM} = 2.9\text{V}$ vs
Differential Input Voltage**

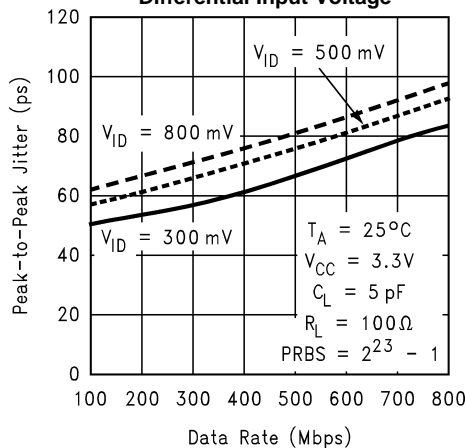


Figure 30.

**Peak-to-Peak Output Jitter at $V_{CM} = 1.2\text{V}$ vs
Differential Input Voltage**

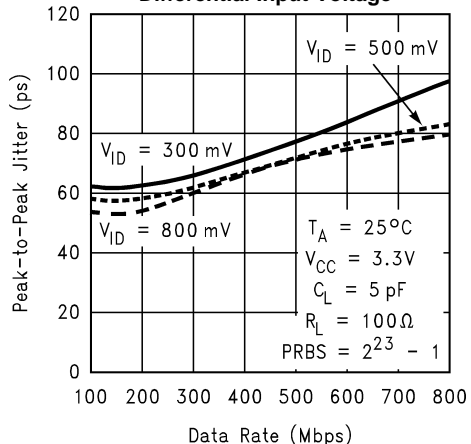


Figure 31.

**Peak-to-Peak Output Jitter at $V_{CM} = 1.2\text{V}$ vs
Ambient Temperature**

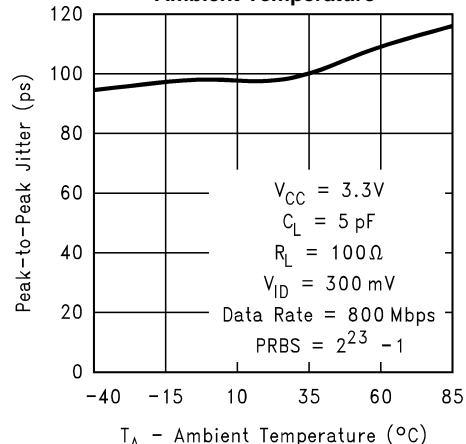


Figure 32.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90LV001TLD/NOPB	Active	Production	WSO (NGK) 8	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	001
DS90LV001TLD/NOPB.A	Active	Production	WSO (NGK) 8	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	001
DS90LV001TLDX/NOPB	Active	Production	WSO (NGK) 8	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	001
DS90LV001TLDX/NOPB.A	Active	Production	WSO (NGK) 8	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	001
DS90LV001TM/NOPB	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV001 TM
DS90LV001TM/NOPB.A	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV001 TM
DS90LV001TM/NOPB.B	Active	Production	SOIC (D) 8	95 TUBE	-	SN	Level-1-260C-UNLIM	-40 to 85	LV001 TM
DS90LV001TMX/NOPB	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV001 TM
DS90LV001TMX/NOPB.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV001 TM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV001TLD/NOPB	WSO	NGK	8	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS90LV001TLDX/NOPB	WSO	NGK	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS90LV001TMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV001TLD/NOPB	WSO	NGK	8	1000	367.0	367.0	35.0
DS90LV001TLDX/NOPB	WSO	NGK	8	4500	356.0	356.0	36.0
DS90LV001TMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

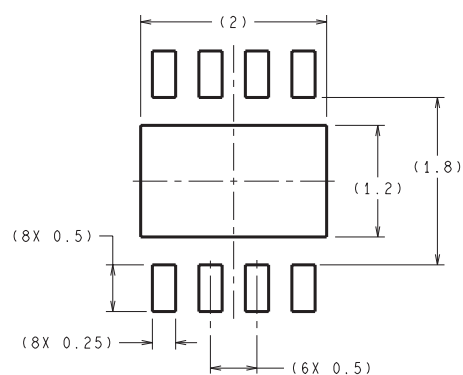
TUBE



*All dimensions are nominal

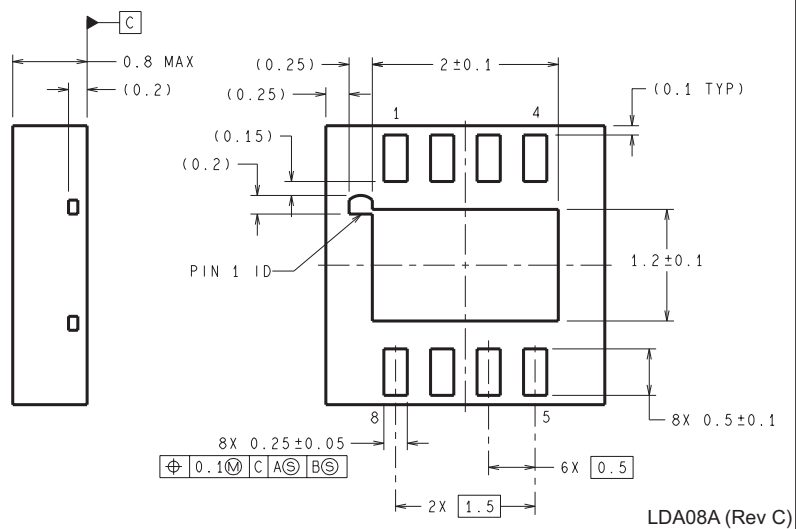
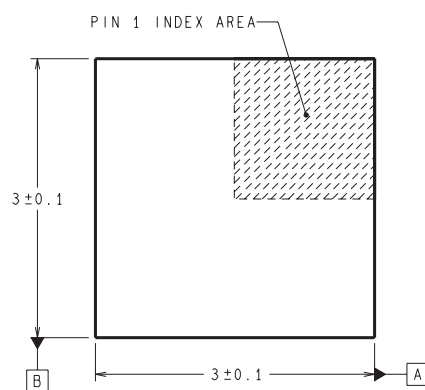
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS90LV001TM/NOPB	D	SOIC	8	95	495	8	4064	3.05
DS90LV001TM/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
DS90LV001TM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

NGK0008A



DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



LDA08A (Rev C)



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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