BENCHMARQ

bq2202

SRAM NV Controller With Reset

Features

- Power monitoring and switching for nonvolatile control of SRAMs
- Write-protect control
- Input decoder allows control of up to 2 banks of SRAM
- 3-volt primary cell input
- 3-volt rechargeable battery input/output
- Reset output for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation

General Description

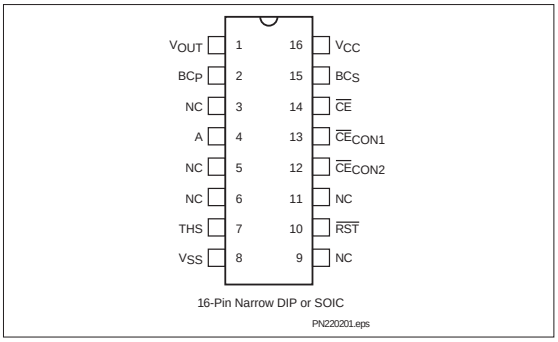
The CMOS bq2202 SRAM Nonvolatile Controller With Reset provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out-of-tolerance is detected, the two conditioned chip-enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the V_{CC} supply to the battery-backup supply as V_{CC} decays. On a subsequent power--up, the V_{OUT} supply is automatically switched from the backup supply to the V_{CC} supply. The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

Pin Connections



Pin Names

V_{OUT}	Supply output
$\overline{RST}$	Reset output
THS	Threshold select input
$\overline{CE}$	Chip enable active low input
$\overline{CE}_{CON1}$, $\overline{CE}_{CON2}$	Conditioned chip enable outputs
A	Bank select input
BC_P	3V backup supply input
BC_S	3V rechargeable backup supply input/output
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip-enable output pins from the bq2202. As the voltage input V_{CC} slews down during a power failure, the two conditioned chip enable outputs, $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$, are forced inactive independent of the chip enable input $\overline{CE}$.

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PFD}. V_{PFD} is selected by the threshold select input pin, THS. If THS is tied to V_{SS}, the power-fail detection occurs at 4.62V typical for 5% supply operation.

If THS is tied to V_{CC}, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{CC} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150µsec maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

Sept. 1997 D

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. Outputs $\overline{CE}_{CON1}$ and $\overline{CE}_{CON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}$ input is passed through to one of the two $\overline{CE}_{CON}$ outputs with a propagation delay of less than 10ns. The $\overline{CE}$ input is output on one of the two $\overline{CE}_{CON}$ output pins; depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ($\overline{RST}$) goes active within t_{PFD} (150µsec maximum) after V_{PFD}, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The $\overline{RST}$ output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when $\overline{RST}$ returns inactive.

Energy Cell Inputs—BC_P, BC_S

Two backup energy source inputs are provided on the bq2202—a primary cell BC_P and a secondary cell BC_S. The primary cell input is designed to accept any 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If a primary cell is not to be used, the BC_P pin should be grounded. The secondary cell input BC_S is designed to accept constant-voltage current-limited rechargeable cells.

During normal 5V power valid operation, 3.3V is output on the BC_S pin and is current-limited internally.

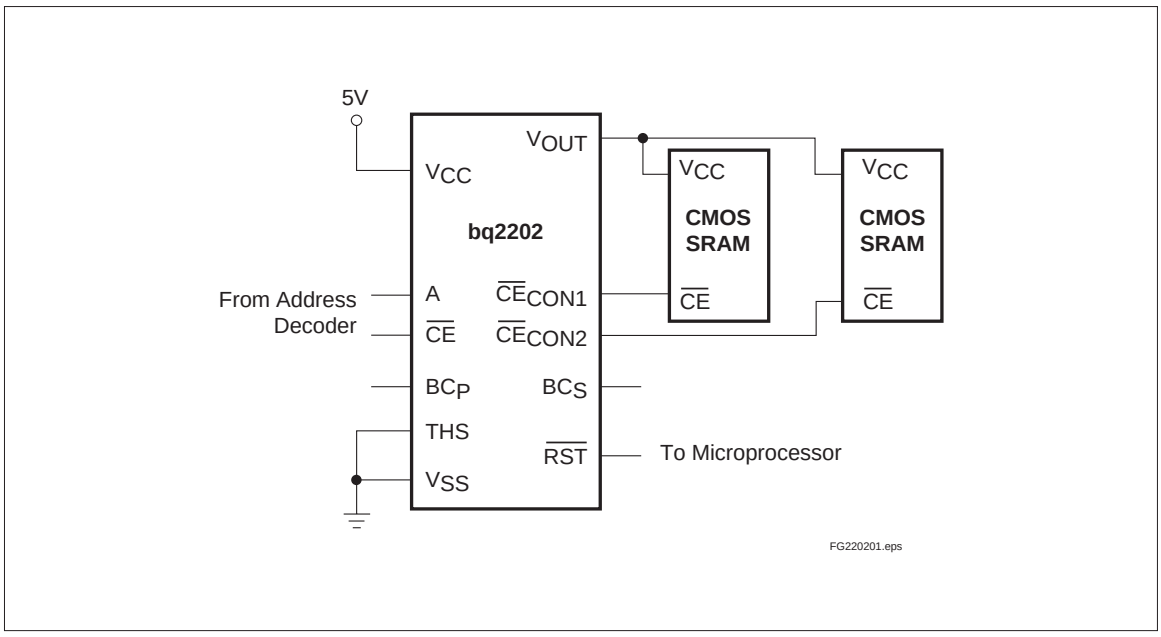


Figure 1. Hardware Hookup (5% Supply Operation)

If a secondary cell is not to be used, the BC_S pin must be tied directly to V_{SS}. If both inputs are used, during power failure the V_{OUT} and $\overline{CE}_{CON}$ outputs are forced high by the secondary cell so long as it is greater than 2.5V. Only the secondary cell is loaded by the data retention current of the SRAM until the voltage at the BC_S pin falls below 2.5V. When and if the voltage at BC_S falls below 2.5V, an internal isolation switch automatically transfers the load from the secondary cell to the primary cell.

To prevent battery drain when there is no valid data to retain, V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ are internally isolated from BC_P and BC_S by either:

- Initial connection of a battery to BC_P or BC_S or
- Presentation of an isolation signal on $\overline{CE}$.

A valid isolation signal requires $\overline{CE}$ low as V_{CC} crosses both V_{PFD} and V_{SO} during a power-down. See Figure 2. Between these two points in time, $\overline{CE}$ must be brought to V_{CC} * (0.48 to 0.52) and held for at least 700ns. The isolation signal is invalid if $\overline{CE}$ exceeds V_{CC} * 0.54 at any point between V_{CC} crossing V_{PFD} and V_{SO}.

The battery is connected to V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$ immediately on subsequent application and removal of V_{CC}.

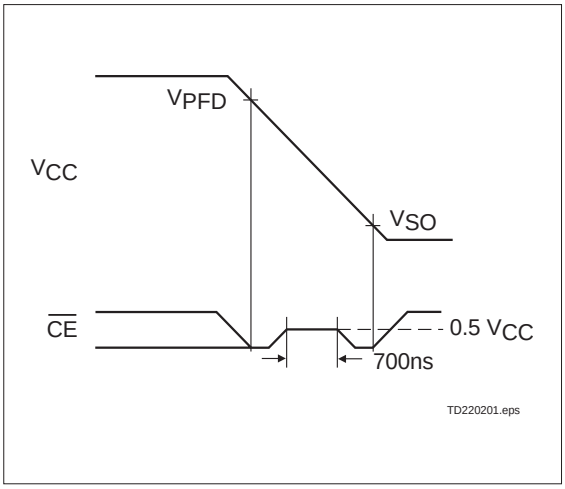


Figure 2. Battery Isolation Signal

Truth Table

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to +7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to +7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{OUT}	V_{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V_{SS}
		4.50	5.0	5.5	V	THS = V_{CC}
V_{BCP}	Backup cell input voltage	2.0	-	4.0	V	$V_{CC} < V_{BC}$
V_{BCS}		2.5	-	4.0		
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	
THS	Threshold select	-0.3	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0mA
V_{OHB}	V_{OH}, backup supply	V_{BC} - 0.3	-	-	V	$V_{BC} > V_{CC}$, I_{OH} = -10µA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0mA
I_{CC}	Operating supply current	-	3	6	mA	No load on V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$
V_{PFD}	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V_{SS}
		4.30	4.37	4.50	V	THS = V_{CC}
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCDR}	Data-retention mode current	-	-	100	nA	No load on V_{OUT}, $\overline{CE}_{CON1}$, and $\overline{CE}_{CON2}$
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.2	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 100mA
		V_{CC} - 0.3	-	-	V	$V_{CC} > V_{BC}$, I_{OUT} = 160mA
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.2	-	-	V	$V_{CC} < V_{BC}$, I_{OUT} = 100µA
V_{BC}	Active backup cell voltage	-	V_{BCS}	-	V	V_{BCS} > 2.5V
		-	V_{BCP}	-	V	V_{BCS} < 2.5V
R_{BCS}	BC_S charge output internal resistance	500	1000	1750	Ω	$V_{BCSO} \geq$ 3.0V
V_{BCSO}	BC_S charge output voltage	3.0	3.3	3.6	V	$V_{CC} > V_{PFD}$, $\overline{RST}$ inactive, full charge or no load
I_{OUT1}	V_{OUT} current	-	-	160	mA	$V_{OUT} \geq V_{CC}$ - 0.3V
I_{OUT2}	V_{OUT} current	-	100	-	µA	$V_{OUT} \geq V_{BC}$ - 0.2V

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C_{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)

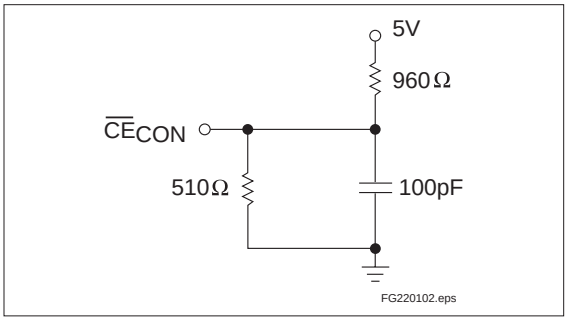


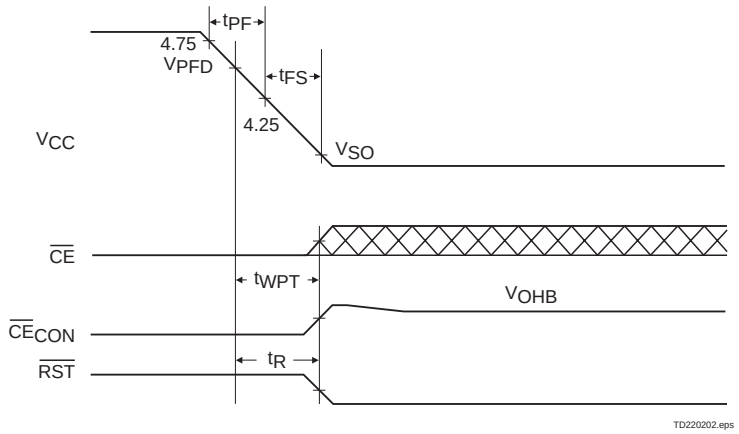
Figure 3. Output Load

Power-Fail Control ($T_A = T_{OPR}$)

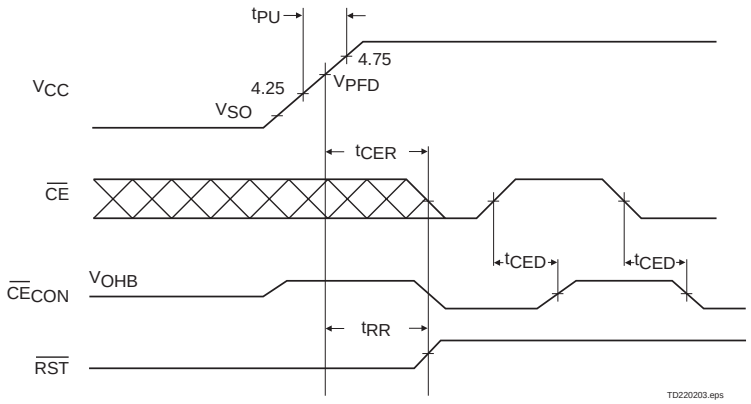
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PF}	V_{CC} slew 4.75 to 4.25V	300	-	-	µs	
t_{FS}	V_{CC} slew 4.25 V to V_{SO}	10	-	-	µs	
t_{PU}	V_{CC} slew 4.25 to 4.75V	0	-	-	µs	
t_{CED}	Chip-enable propagation delay	-	7	10	ns	
t_{CER}	Chip-enable recovery time	t_{RR}	-	t_{RR}	ms	Time during which SRAM is write-protected after V_{CC} passes V_{PFD} on power-up
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	40	80	120	ms	Time, after V_{CC} becomes valid, before $\overline{RST}$ is cleared
t_{AS}	Input A set up to $\overline{CE}$	0	-	-	ns	
t_{WPT}	Write-protect time	t_R	-	t_R	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before $\overline{RST}$ is active

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.

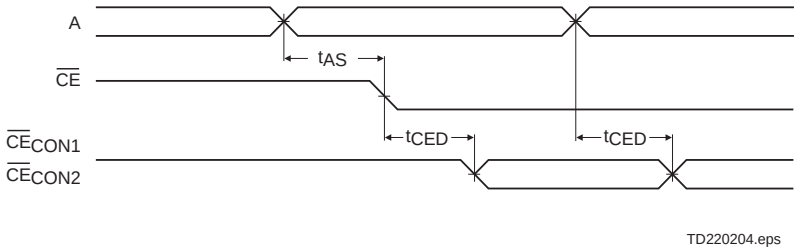
Power-Down Timing



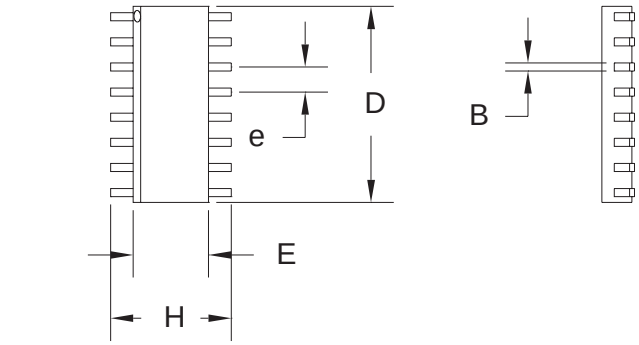
Power-Up Timing

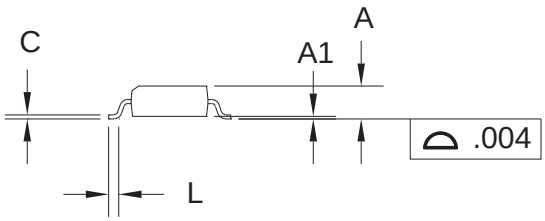


Address-Decode Timing



16-Pin SOIC Narrow



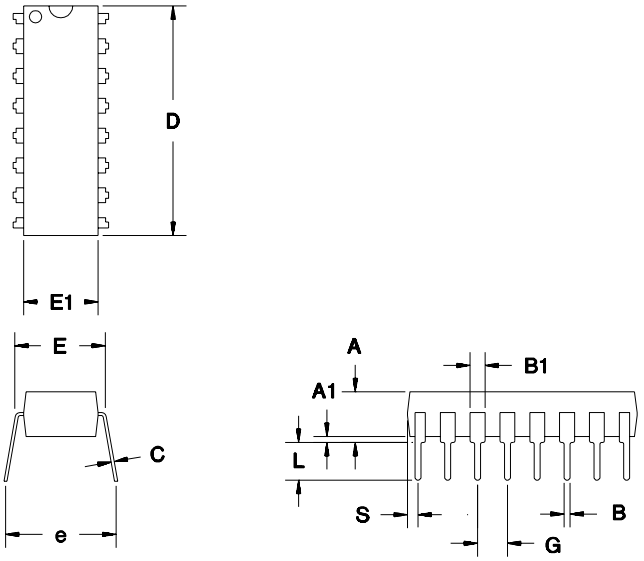


16-Pin SOIC Narrow (SN)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.

16-Pin DIP Narrow



16-Pin DIP Narrow (PN)

Dimension	Minimum	Maximum
A	0.160	0.180
A1	0.015	0.040
B	0.015	0.022
B1	0.055	0.065
C	0.008	0.013
D	0.740	0.770
E	0.300	0.325
E1	0.230	0.280
e	0.300	0.370
G	0.090	0.110
L	0.115	0.150
S	0.020	0.040

All dimensions are in inches.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2	Deleted last sentence	Clarification
1	5	V_{BCSO}—BC_S charge output voltage	Was: 3.15 min, 3.3 typ, 3.45 max Is: 3.0 min, 3.3 typ, 3.6 max
2	5	Changed maximum charge output internal resistance (R_{BCS})	Was: 1500Ω Is: 1750Ω
3	1, 4, 5	10% supply operation	Was: THS tied to V_{OUT} Is: THS tied to V_{CC}

Note: Change 1 = Dec. 1992 B changes from Sept. 1991 A.
Change 2 = Nov. 1994 C changes from Dec. 1992 B.
Change 3 = Sept. 1997 D changes from Nov. 1994 C.

Ordering Information

bq2202

Temperature Range:
blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)

Package Option:
PN = 16-pin narrow plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2202 SRAM Nonvolatile Controller With Reset

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.