# SC194A
# 1A Synchronous Buck Converter with Integrated Power Devices



## Description

The SC194A is a synchronous step-down converter with integrated power devices. The SC194A is designed for single-cell Li-Ion battery applications, but can also be used in fixed 3.3V or 5V applications. The switching frequency is nominally set to 1MHz, allowing the use of small inductors and capacitors. The 1.3A maximum current rating of the internal MOSFET switches allows a DC output current of 1A.

The SC194A has a flexible clocking methodology that allows it to be synchronized to an external oscillator or controlled by the internal oscillator. The device can operate in either forced PWM mode or in PSAVE mode. If PSAVE mode is enabled the part will automatically enter PFM at light loads to maintain maximum efficiency across the full load range.

For noise sensitive applications, PSAVE mode can be disabled by synchronizing to an external oscillator, or pulling the SYNC/PWM pin high. Shutdown turns off all the control circuitry to achieve a typical shutdown current of 0.1µA.

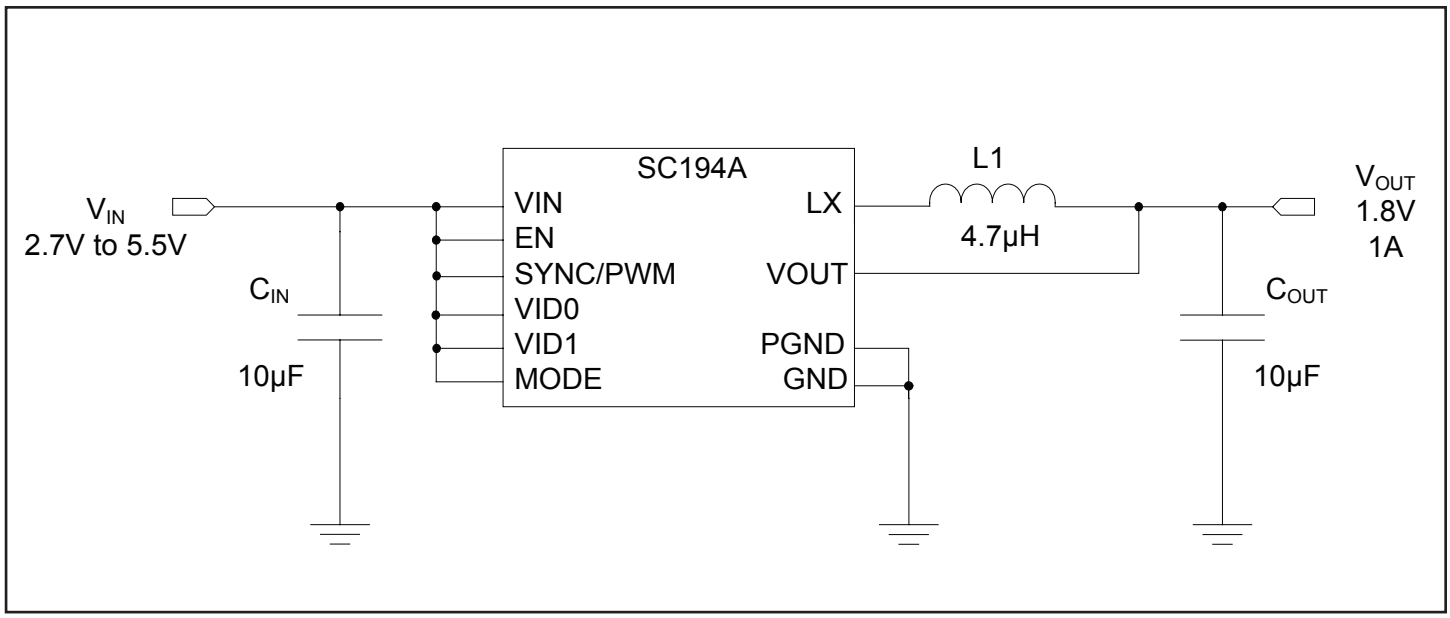
## Features

- Up to 93% efficiency
- Output current - 1A
- Input range - 2.7V to 5.5V
- Quiescent current - 17µA
- Four selectable output voltages
- Dynamic voltage positioning capability
- Fixed 1MHz frequency or 750kHz to 1.25MHz synchronized operation
- PSAVE operation to maximize efficiency at light loads
- Minimal external components
- Fast transient response
- 100% duty cycle in dropout
- Soft-start
- Over-temperature and short-circuit protection
- Space-saving lead-free package - MLP-10, 3 x 3mm

## Applications

- Cell phones
- Wireless communication chipset power
- Personal media player
- Notebook and sub-notebook computers
- PDAs and mobile communicators
- WLAN peripherals

## Typical Application Circuit



## Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

| Parameter | Symbol | Maximum | Units |
|---|---|---|---|
| Input Supply Voltage | $V_{IN}$ | -0.3 to 7 | V |
| Logic Inputs (SYNC/PWM, EN, MODE, VID0, VID1) | $V_N$ | -0.3 to $V_{IN}$+0.3, 7V Max | V |
| Output Voltage | $V_{OUT}$ | -0.3 to $V_{IN}$+0.3, 7V Max | V |
| LX Voltage | $V_{LX}$ | -1 to $V_{IN}$ +1, 7V Max | V |
| Thermal Impedance Junction to Ambient(1) | $\theta_{JA}$ | 40 | °C/W |
| VOUT Short-Circuit to GND | $t_{SC}$ | Continuous | s |
| Operating Ambient Temperature Range | $T_A$ | -40 to +85 | °C |
| Storage Temperature | $T_S$ | -60 to +160 | °C |
| Junction Temperature | $T_{JC}$ | -40 to +150 | °C |
| Peak IR Reflow Temperature | $T_{LEAD}$ | 260 | °C |
| ESD Protection Level (2) | $V_{ESD}$ | 2 | kV |

Note:
1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
2) Tested according to JEDEC standard JESD22-A114-B.

## Electrical Characteristics

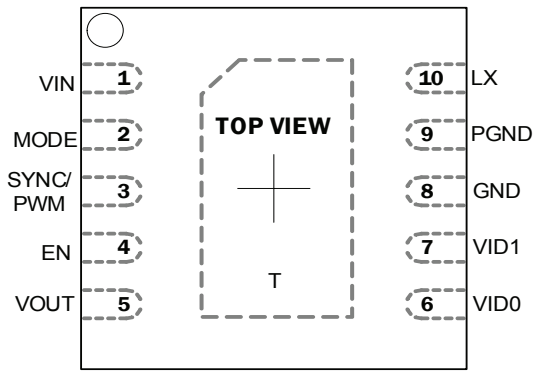
Unless otherwise noted: $V_{IN}$ = 3.6V, EN = $V_{IN}$, SYNC/PWM = $V_{IN}$, MODE = $V_{IN}$, $T_A$ = -40 to 85°C. Typical values are at $T_A$ = 25°C.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 2.7 | | 5.5 | V |
| VOUT Accuracy | $V_{OUT}$ | $I_{OUT}$ = 0.5A, $T_A$ = 25°C | | | ±1 | % |
| VOUT Temperature Accuracy | $V_{OUT(T)}$ | $I_{OUT}$ = 0.5A, $T_A$ = -40 to 85°C | | ±0.3 | ±0.7 | % |
| Line Regulation | $V_{OUT\ LINE}$ | $V_{IN}$ = 2.7V to 5.5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 0.5A, $T_A$ = -40 to 85°C | | ±0.4 | ±0.65 | % |
| Load Regulation (PWM) | $V_{OUT\ LOAD}$ | $I_{OUT}$ = 0A to 1A, $T_A$ = -40 to 85°C | | ±0.3 | ±0.65 | % |
| PSAVE Regulation | $V_{OUT\ PSAVE}$ | SYNC/PWM =GND, $C_{OUT}$=22 µF | | +1.3<br>-0.3 | +1.6<br>-0.6 | % |
| P-Channel On Resistance | $R_{DSP}$ | $I_{LX}$ = 100mA | | 0.275 | | Ω |
| N-Channel On Resistance | $R_{DSN}$ | $I_{LX}$ = 100mA | | 0.165 | | Ω |
| Start-Up Time | $T_{START}$ | | | | 5 | ms |
| P-Channel Current Limit | $I_{LIM(P)}$ | | 1.33 | 1.9 | 2.47 | A |

## Electrical Characteristics (Cont.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Quiescent Current | $I_Q$ | SYNC/PWM = GND, $I_{OUT}$ = 0A, $V_{OUT}$ = 1.04 x $V_{OUT(Programmed)}$ | | 17 | 28 | µA |
| Shutdown Current | $I_{SD}$ | EN = GND, LX = OPEN | | 0.1 | 1 | µA |
| LX Leakage Current PMOS | $I_{LXP}$ | LX = GND, EN = GND | | 0.1 | 2 | µA |
| LX Leakage Current NMOS | $I_{LXN}$ | LX = 3.6V, EN = GND | -2 | 0.1 | | µA |
| Oscillator Frequency | $f_{OSC}$ | | 0.85 | 1.0 | 1.15 | MHz |
| SYNC Frequency (upper) | $f_{SYNCU}$ | | 1.25 | | | MHz |
| SYNC Frequency (lower) | $f_{SYNCL}$ | | | | 750 | kHz |
| UVLO Threshold (upper) | $V_{UVL}$ | | 2.38 | 2.52 | 2.65 | V |
| UVLO Hysteresis | $V_{UVLHYS}$ | | | 50 | | mV |
| Thermal Shutdown | $T_{SD}$ | | | 145 | | °C |
| Thermal Shutdown Hysteresis | $T_{SD-HYS}$ | | | 10 | | °C |
| Logic Input High | $V_{IH}$ | EN, SYNC/PWM, VID0, VID1, MODE | 1.6 | | | V |
| Logic Input Low | $V_{IL}$ | EN, SYNC/PWM, VID0, VID1, MODE | | | 0.6 | V |
| Logic Input Current High | $I_{IH}$ | EN, SYNC/PWM, VID0, VID1, MODE | -2 | 0.1 | 2 | µA |
| Logic Input Current Low | $I_{IL}$ | EN, SYNC/PWM, VID0, VID1, MODE | -2 | 0.1 | 2 | µA |

## Pin Configuration




**MLP10: 3X3 10 LEAD**

## Ordering Information

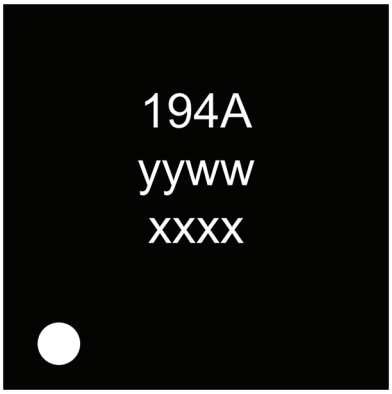
| DEVICE | PACKAGE |
|---|---|
| SC194AMLTRT(1)(2) | MLP 3x3-10 |
| SC194AEVB | Evaluation Board |

Notes:
1) Lead-free packaging only. This product is fully WEEE and RoHS compliant.
2) Available in tape and reel only. A reel contains 3000 devices.

## Programmable Output Voltage

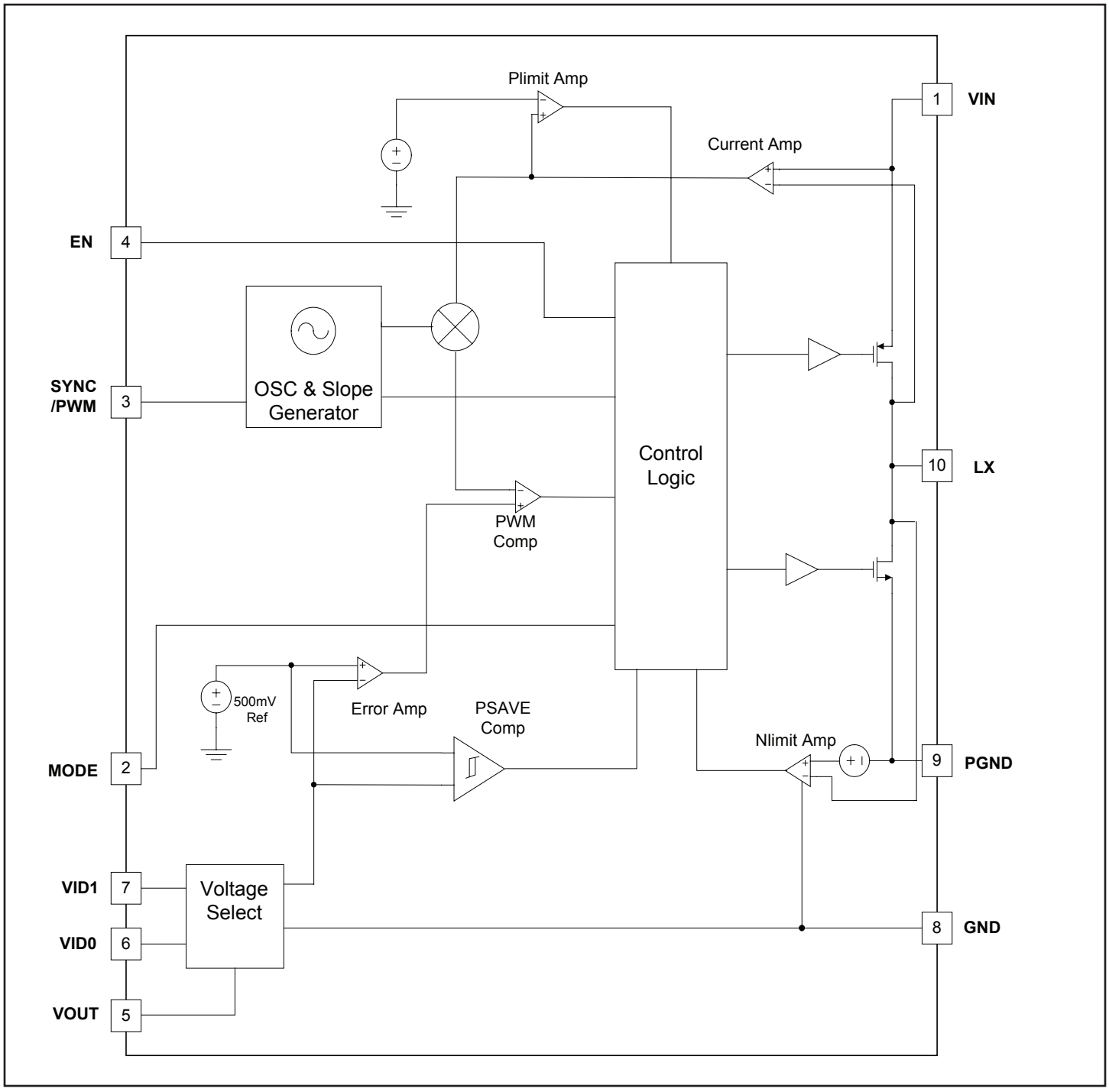
| VID1 | VID0 | SC194A $V_{OUT}$ |
|---|---|---|
| 0 | 0 | 1.0V |
| 0 | 1 | 1.2V |
| 1 | 0 | 1.5V |
| 1 | 1 | 1.8V |

## Marking Information




yy = two digit year of manufacture
ww = two digit week of manufacture
xxxx = lot number

## Block Diagram



## Pin Descriptions

| Pin # | Pin Name | Pin Function |
|---|---|---|
| 1 | VIN | Input power supply voltage |
| 2 | MODE | MODE select pin - MODE = $V_{IN}$ to select 100% duty cycle function, MODE = GND to disable |
| 3 | SYNC/PWM | Oscillator synchronization input - Tie to $V_{IN}$ for forced PWM mode or GND to allow the part to enter PSAVE mode at light loads. Apply an external clock signal for frequency synchronization. |
| 4 | EN | Enable digital input - a high input enables the SC194A, a low disables and reduces quiescent current to less than 1µA. In shutdown, LX becomes high impedance. |
| 5 | VOUT | Regulated output voltage and feedback for SC194A |
| 6 | VID0 | Logic level bit 0 used in conjunction with VID1 to set the output voltage. Connect high or low as required to select the desired output voltage. If not connected, the output voltage will be indeterminate. |
| 7 | VID1 | Logic level bit 1 used in conjunction with VID0 to set the output voltage. Connect high or low as required to select the desired output voltage. If not connected, the output voltage will be indeterminate. |
| 8 | GND | Ground |
| 9 | PGND | Power Ground |
| 10 | LX | Inductor connection to the switching FETs |
| T | THERMAL PAD | Pad for heatsinking purposes - not connected internally. Connects to ground plane using multiple vias. |

## Applications Information

### SC194A Detailed Description

The SC194A is a synchronous step-down Pulse Width Modulated (PWM), DC-DC converter utilizing a 1MHz fixed-frequency current mode architecture. The device is designed to operate in a fixed-frequency PWM mode across the full load range and can enter Power Save Mode (PSAVE) utilizing Pulse Frequency Modulation (PFM) at light loads to maximize efficiency.

### Operation

During normal operation the PMOS MOSFET is activated on each rising edge of the internal oscillator. Current feedback for the switching regulator uses the PMOS current path, and it is amplified and summed with the internal slope compensation network. The voltage feedback loop uses an internal feedback divider. The on-time is determined by comparing the summed current feedback and the output of the error amplifier. The period is set by the onboard oscillator or by an external clock attached to the SYNC/PWM pin.

The SC194A has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin.

### Programmable Output Voltage

The SC194A has four pre-determined output voltage values which can be individually selected by the correct programming of the VID0 and VID1 pins (see Programmable Output Voltage table on Page 4). This eliminates the need for external programming resistors saving PCB area and inventory. The VID pins can be statically tied to GND or VIN for fixed output configurations or they may be driven by a microprocessor enabling the possibility of dynamic voltage adjustment for host equipment "sleep" states.

### Continuous Conduction & Oscillator Synchronization

The SC194A is designed to operate in continuous conduction, fixed-frequency mode. When the SYNC/PWM pin is tied high the part runs in PWM mode using the internal oscillator. The part can be synchronized to an external clock by driving a clock signal into the SYNC/PWM pin. The part synchronizes to the rising edge of the clock.

### Protection Features

The SC194A provides the following protection features:

- Thermal shutdown
- Current limit
- Over-voltage protection
- Soft-start

### Thermal Shutdown

The device has a thermal shutdown feature to protect the SC194A if the junction temperature exceeds 145°C. In thermal shutdown the on-chip power devices are disabled, tri-stating the LX output. Switching will resume when the temperature drops by 10°C. During this time if the output voltage decreases by more than 60% of its programmed value, a soft-start will be invoked.

### Current Limit

The PMOS and NMOS power devices of the buck switcher stage are protected by current limit functions. In the case of a short to ground on the output, the part enters frequency foldback mode, that causes the switching frequency to divide by a factor determined by the output voltage. This prevents the inductor current from "stair-casing".

### Over-Voltage Protection

Over-voltage protection is provided on the SC194A. In the event of an over-voltage on the output in switcher mode, the PWM drive is disabled, tri-stating the LX output. The part will not resume switching until the output voltage has fallen below 2% of the regulation voltage.

### Soft-Start

The soft-start mode is enabled after every shutdown cycle to limit in-rush current. In conjunction with the frequency foldback, this controls the maximum current during start-up. The PMOS current limit is stepped up through seven soft-start levels to the full value by a timer driven from the internal oscillator. During soft-start, the switching frequency is stepped by 1/8, 1/4, and 1/2 of the internal oscillator frequency up to the full value, under control of three output voltage thresholds. As soon as the output voltage is within 2% of the regulation voltage, soft-start mode is disabled.

### Power Save Mode Operation

The PSAVE mode may be selected by tying the SYNC/PWM pin to GND. Selecting PSAVE mode will enable the SC194A to automatically activate/deactivate operation at light loads maximizing efficiency across the full load range. The SC194A automatically detects the load current at which it should enter PSAVE mode. The SC194A is optimized to track maximum efficiency with respect to $V_{IN}$.

## Applications Information (Cont.)

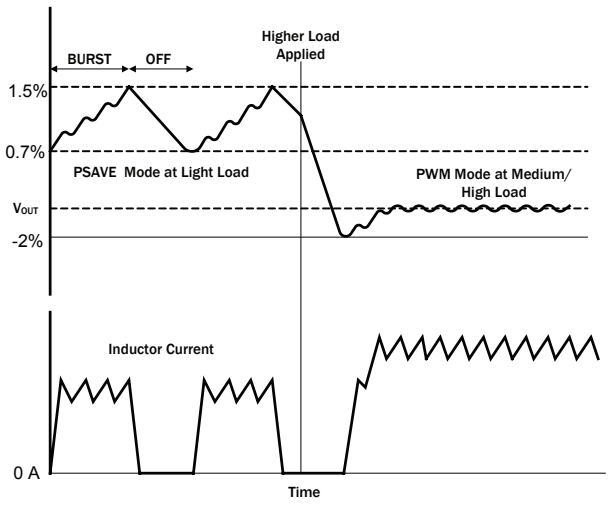
In PSAVE mode $V_{OUT}$ is driven from a lower level to an upper level by a switching burst. Once the upper level has been reached the switching is stopped and the quiescent current is reduced. $V_{OUT}$ falls from the upper to lower levels in this low current state as the load current discharges the output capacitor. The burst-to-off period in PSAVE will decrease as the load current reduces.

The PSAVE switching burst frequency is controlled so that the inductor current ripple is similar to that in PWM mode. The minimum switching frequency during this period is limited to 650kHz.

The SC194A automatically detects when to exit PSAVE mode by monitoring $V_{OUT}$. For the SC194A to exit PSAVE mode, the load must be increased, causing $V_{OUT}$ to decrease until the power save exit threshold is reached. PSAVE levels are set high to minimize the undershoot when exiting PSAVE. The lower PSAVE comparator level is set +0.7% above $V_{OUT}$, and the upper comparator level at +1.5% above $V_{OUT}$, with the exit threshold at -2% below $V_{OUT}$.

If PSAVE operation is required then a 22µF output capacitor must be used.

**Power Save Operation**




**100% Duty Cycle Operation**

The 100% duty cycle mode may be selected by connecting the MODE pin high. This will allow the SC194A to maintain output regulation under low input voltage/high output voltage conditions.

In 100% duty cycle operation, as the input supply drops toward the output voltage, the PMOS on-time increases linearly above the maximum value in fixed-frequency operation until the PMOS is active continuously. Once the PMOS is switched on continuously, the output voltage tracks the input voltage minus the voltage drop across the PMOS power device and inductor according to the following relationship:

$$V_{OUT} = V_{IN} - I_{OUT} \times (R_{DSP} + R_{IND})$$

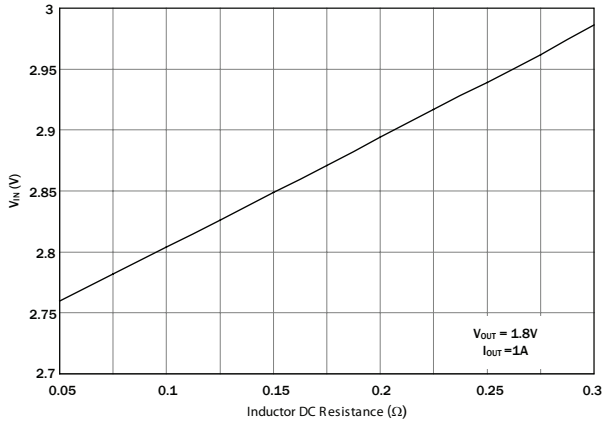
where,

$V_{OUT}$ = Output voltage
$V_{IN}$ = Input voltage
$I_{OUT}$ = Output current
$R_{DSP}$ = PMOS switch ON resistance
$R_{IND}$ = Series resistance of the inductor

The 100% duty cycle can only operate for a programmed output voltage of 1.8V.

With an output voltage of 1.8V, 100% duty cycle mode will only be required to maintain regulation if $V_{IN}$ falls below a minimum value shown in the graph below.

**Minimum $V_{IN}$ for Fixed Frequency Operation Vs. $R_{IND}$**



## Applications Information (Cont.)

The SC194A is designed for use with a 4.7µH inductor. The magnitude of the inductor current ripple is dependent on the inductor value and can be determined by the following equation:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{OSC}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

This equation demonstrates the relationship between input voltage, output voltage, and inductor ripple current.

The inductor should have a low DCR to minimize the conduction losses and maximize efficiency. As a minimum requirement, the DC current rating of the inductor should be equal to the maximum load current plus half of the inductor current ripple as shown by the following equation:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Final inductor selection will depend on various design considerations such as efficiency, EMI, size and cost. Table 1 lists the manufacturers of practical inductor options.

### $C_{IN}$ Selection

The source input current to a buck converter is non-continuous. To prevent large input voltage ripple a low ESR ceramic capacitor is required. A minimum value of 10µF should be used for sufficient input voltage filtering and a 22µF should be used for improved input voltage filtering.

### $C_{OUT}$ Selection

The internal compensation is designed to work with a certain output filter corner frequency defined by the equation:

$$f_c = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

This single pole filter is designed to operate with a minimum output capacitor value of 10µF. Larger output capacitor values will improve transient performance. If PSAVE operation is required the minimum capacitor value is 22µF.

Output voltage ripple is a combination of the voltage ripple from the inductor current charging and discharging the output capacitor and the voltage created from the inductor current ripple through the output capacitor ESR. Selecting an output capacitor with a low ESR will reduce the output voltage ripple component, as can be seen in the following equation:

$$\Delta V_{OUT(ESR)} = \Delta I_{L(ripple)} \times ESR_{COUT}$$

Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application. Table 2 lists the manufacturers of recommended capacitor options.

**Table 1: Recommended Inductors**

| Manufacturer/Part # | Value µH | DCR Ω | Saturation Current A | Tolerance ±% | Dimensions (LxWxH) mm |
|---|---|---|---|---|---|
| BI Technologies HM66304R7 | 4.7 | 0.072 | 1.32 | 20 | 4.7 × 4.7 × 3.0 |
| Coilcraft D01608C-472ML | 4.7 | 0.09 | 1.5 | 20 | 6.6 × 4.5 × 3.0 |
| TDK VLCF4018T- 4R7N1R0-2 | 4.7 | 0.101 | 1.07 | 30 | 4.3 × 4.0 × 1.8 |

**Table 2: Recommended Capacitors**

| Manufacturer/Part # | Value µF | Rated Voltage VDC | Temperature Characteristic | Case Size |
|---|---|---|---|---|
| Murata GRM21BR60J226ME39L | 22 | 6.3 | X5R | 0805 |
| Murata GRM188R60J106 MKE19 | 10 | 6.3 | X5R | 0603 |
| TDK C2012X5R0J106K | 10 | 6.3 | X5R | 0603 |

Note: Where PSAVE operation is required 22µF must be used for $C_{OUT}$.

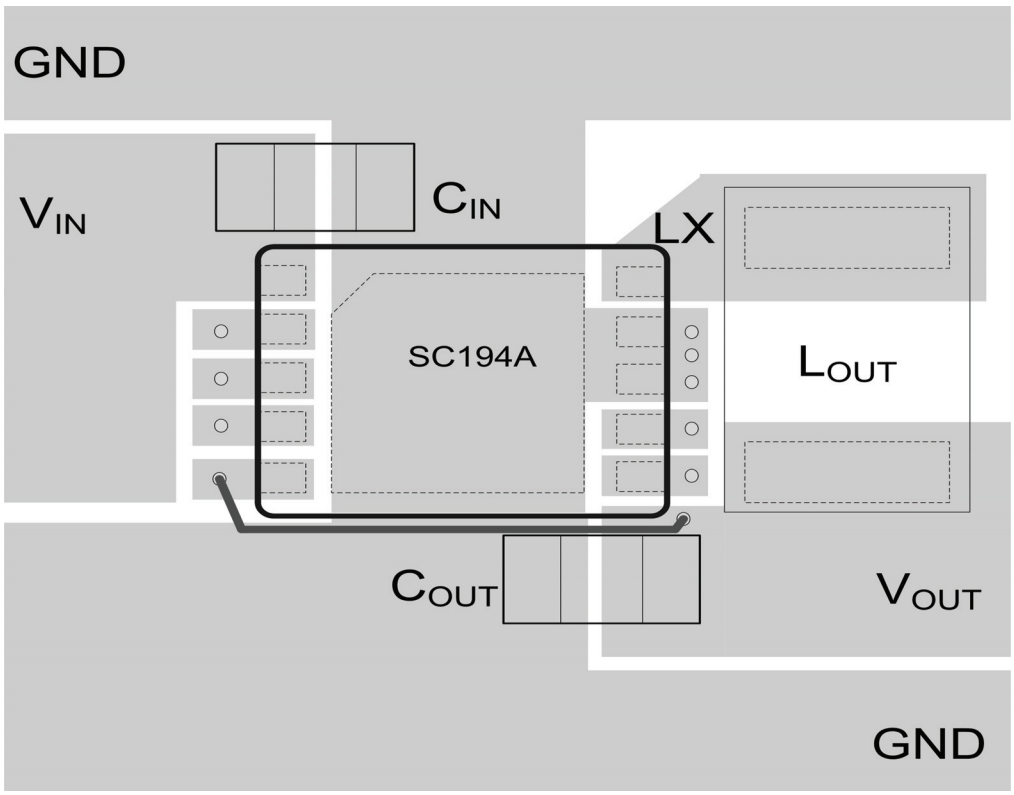
## Applications Information (Cont.)

**PCB Layout Considerations**

Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce and resistive voltage losses. Poor regulation and instability can result.

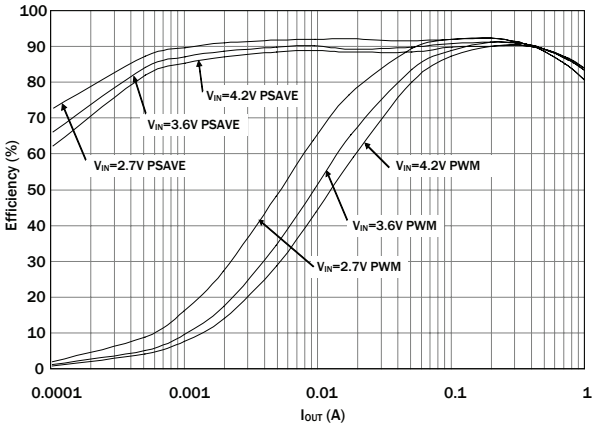
A few simple design rules can be implemented to ensure good layout:

1. Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
2. Route the output voltage feedback path away from the inductor and LX node to minimize noise and magnetic interference.
3. Maximize ground metal on the component side to improve the return connection and thermal dissipation. Separation between the LX node and GND should be maintained to avoid coupling of switching noise to the ground plane.
4. Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

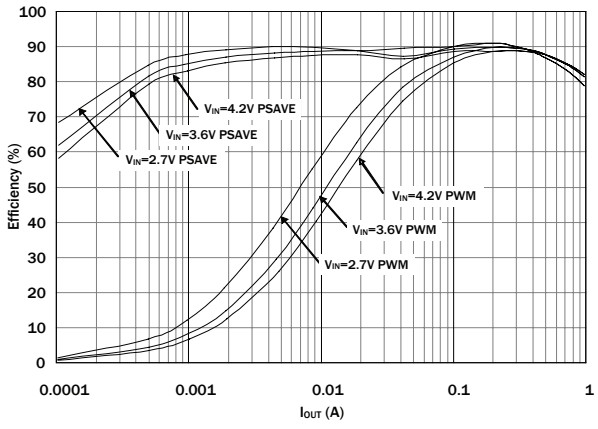


## Typical Characteristics

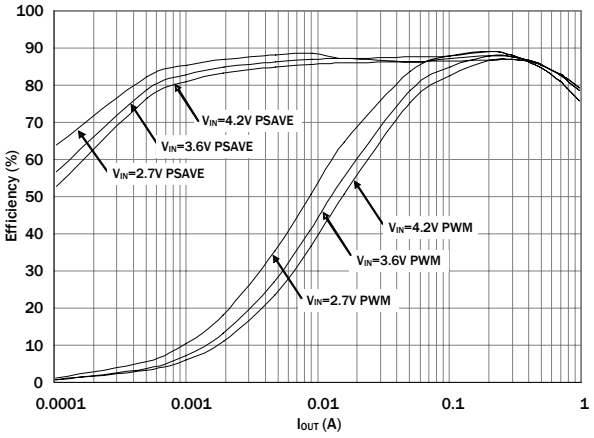
### Efficiency vs. Load Current $V_{OUT}$ = 1.8V



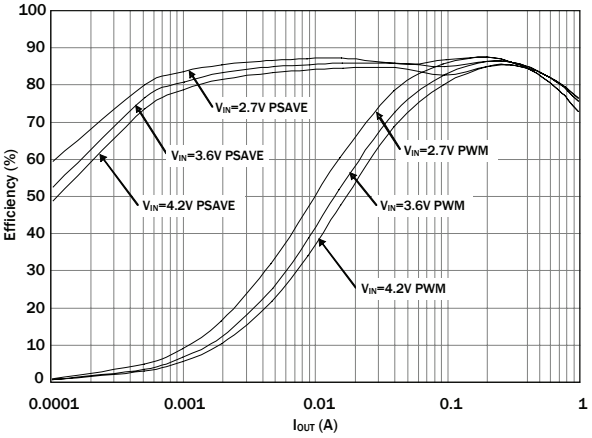

### Efficiency vs. Load Current $V_{OUT}$ = 1.5V



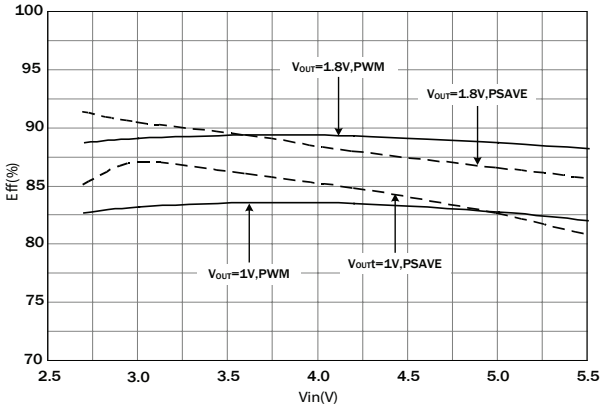

### Efficiency vs. Load Current $V_{OUT}$ = 1.2V




### Efficiency vs. Load Current $V_{OUT}$ = 1.0V

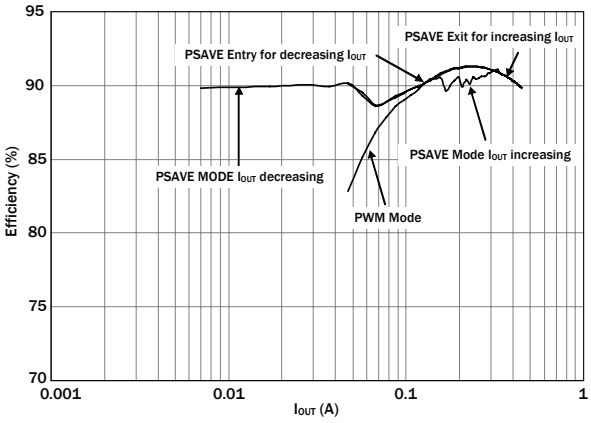



### Efficiency vs. Input Voltage



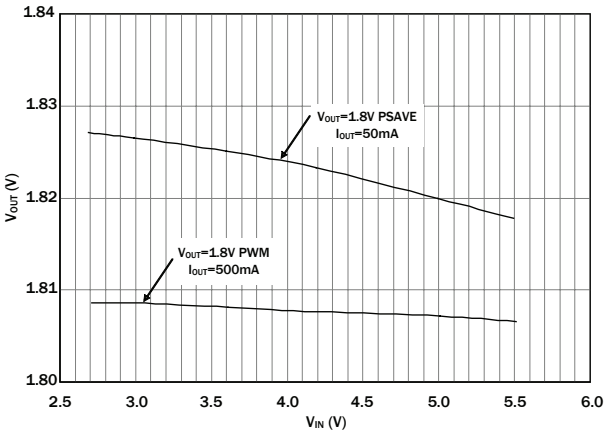

$I_{OUT}$=500 mA(PWM)/50 mA(PSAVE)

### PWM to PSAVE Hysteresis

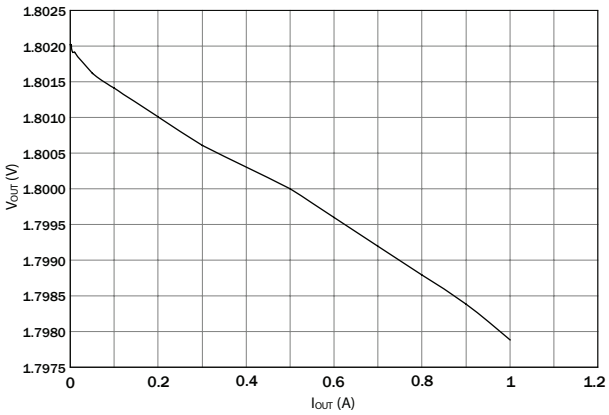


## Typical Characteristics (Cont.)

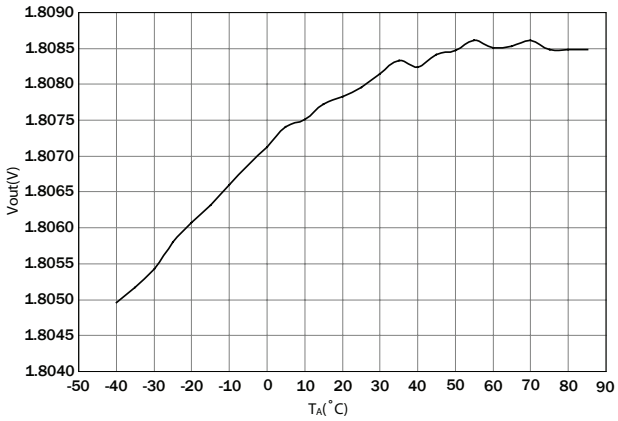
### $V_{OUT}$ vs. $V_{IN}$



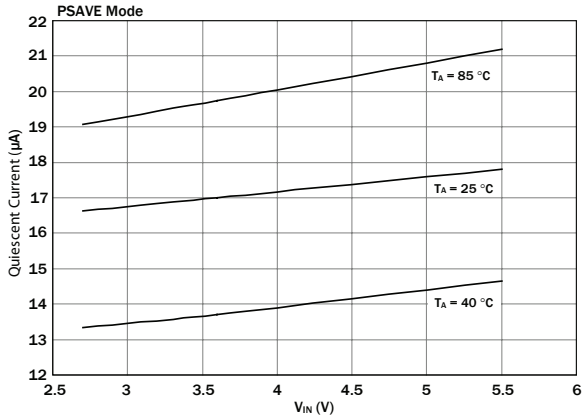

### $V_{OUT}$ vs. $I_{OUT}$, $V_{OUT}$=1.8V, PWM



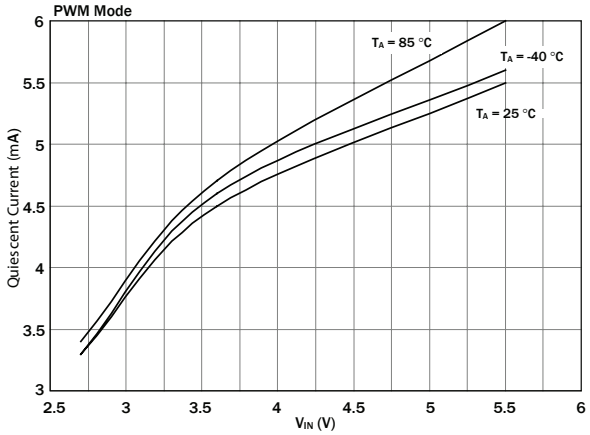

### $V_{OUT}$ vs. Temperature
### $V_{OUT}$=1.8V, PWM



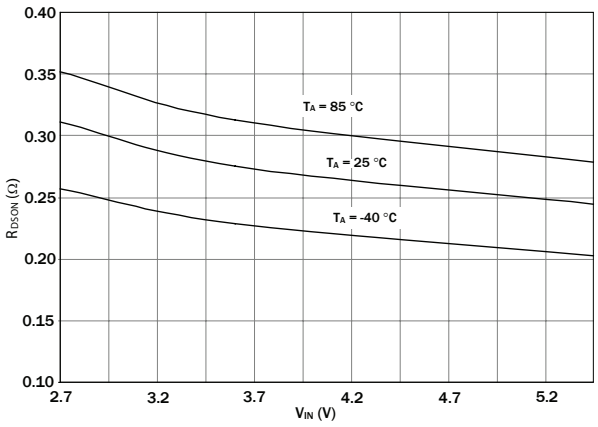

### Quiescent Current vs. Input Voltage




### Quiescent Current vs. Input Voltage

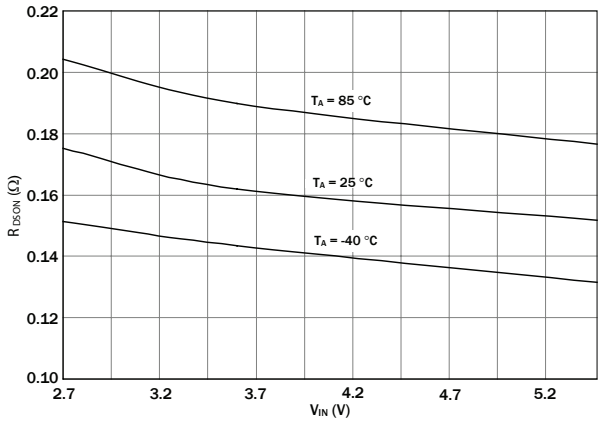



### P-Channel $R_{DSON}$ vs. Input Voltage

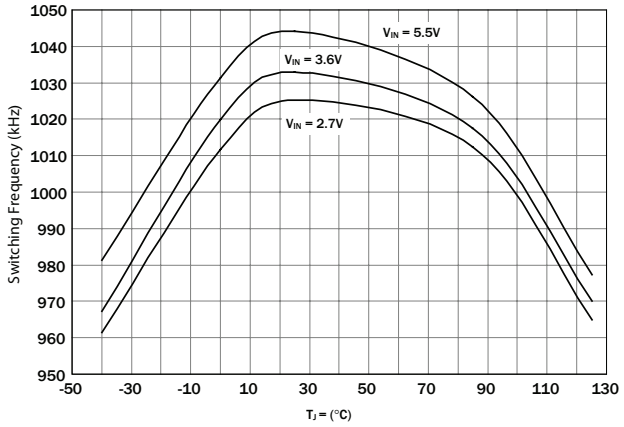


## Typical Characteristics (Cont.)

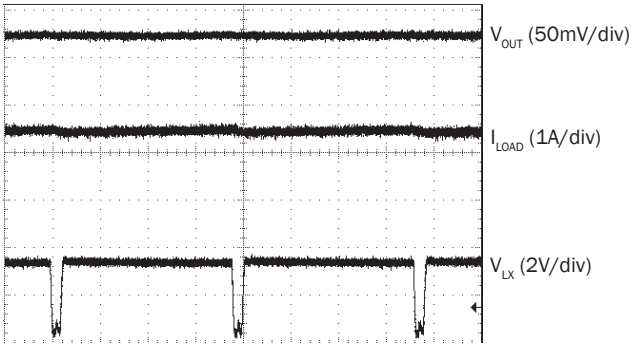
### N-Channel $R_{DSON}$ vs. Input Voltage




### Switching Frequency vs. Temperature

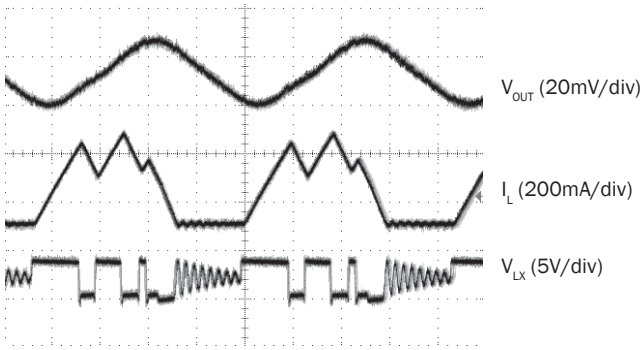



### 100% Duty Cycle Mode



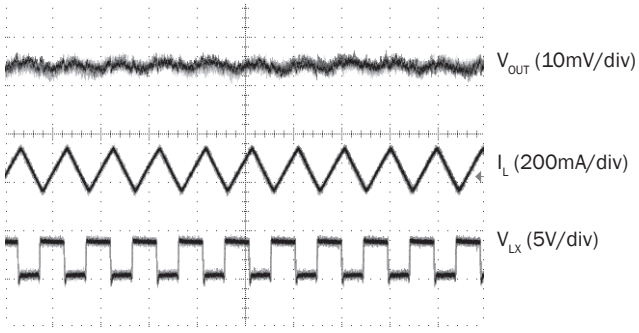

**Time (400ns/div)**
Condition $V_{IN}$=2.6V, $V_{OUT}$=1.8V, $I_{OUT}$=1.4A,
SYNC/PWM=1.15MHz ext clock

### PSAVE Operation



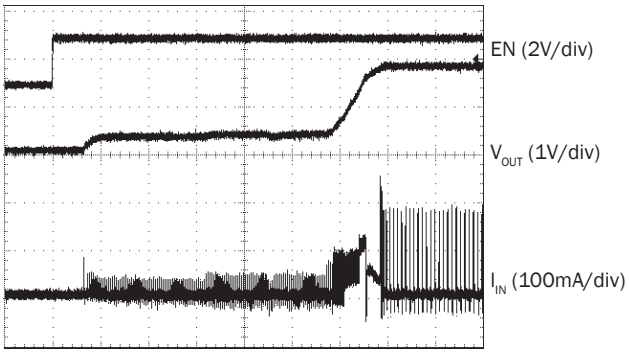

**Time (1us/div)**
Condition $V_{IN}$=3.6V, $V_{OUT}$=1.8V, $I_{OUT}$=150mA,
SYNC/PWM=GND

### PWM Operation




**Time (1us/div)**
Condition $V_{IN}$=3.6V, $V_{OUT}$=1.8V, $I_{OUT}$=150mA,
SYNC/PWM=$V_{IN}$

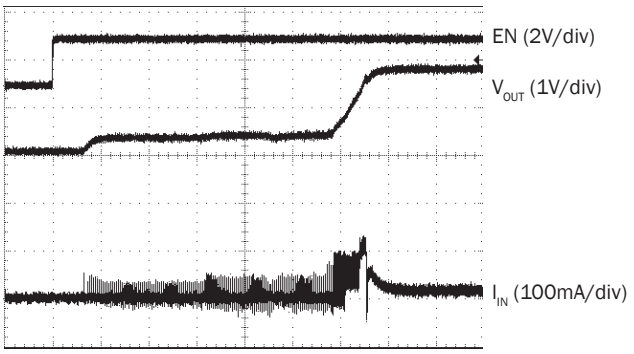
### PSAVE Start up




**Time (200us/div)**
Condition $V_{IN}$=3.6V, $V_{OUT}$=1.8V, $I_{OUT}$=10mA,
SYNC/PWM=GND

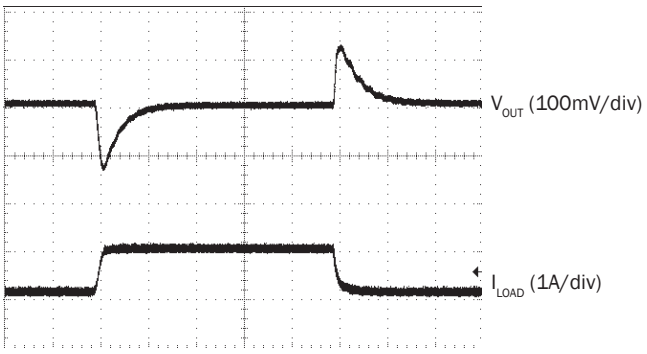
## Typical Characteristics (Cont.)

### PWM Start-up



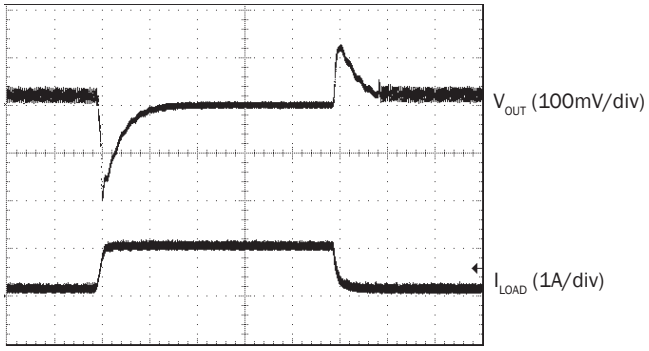

**Time (200us/div)**
Condition $V_{IN}$=3.6V, $V_{OUT}$=1.8V, $I_{OUT}$=10mA, SYNC/PWM=$V_{IN}$

### Load Transient Response PWM



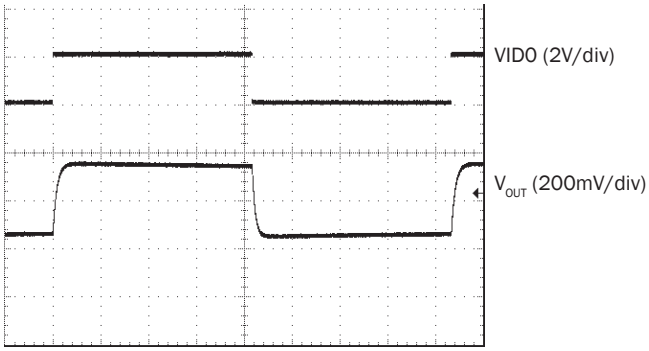

**Time (100us/div)**
Condition $V_{IN}$=3.6V, $V_{OUT}$=1.8V, $I_{OUT}$=1A to 100mA, SYNC/PWM=$V_{IN}$

### Load Transient Response PSAVE




**Time (100us/div)**
Condition $V_{IN}$=3.6V, $V_{OUT}$=1.8V, $I_{OUT}$=1A to 100 mA, SYNC/PWM=GND

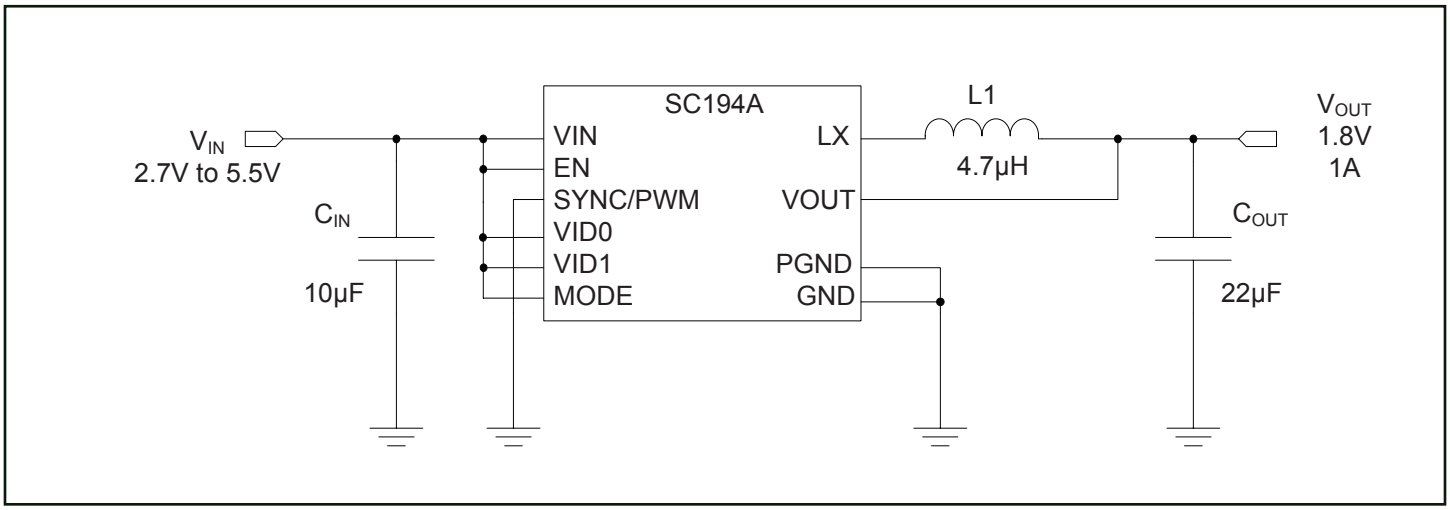
### VID Code Change



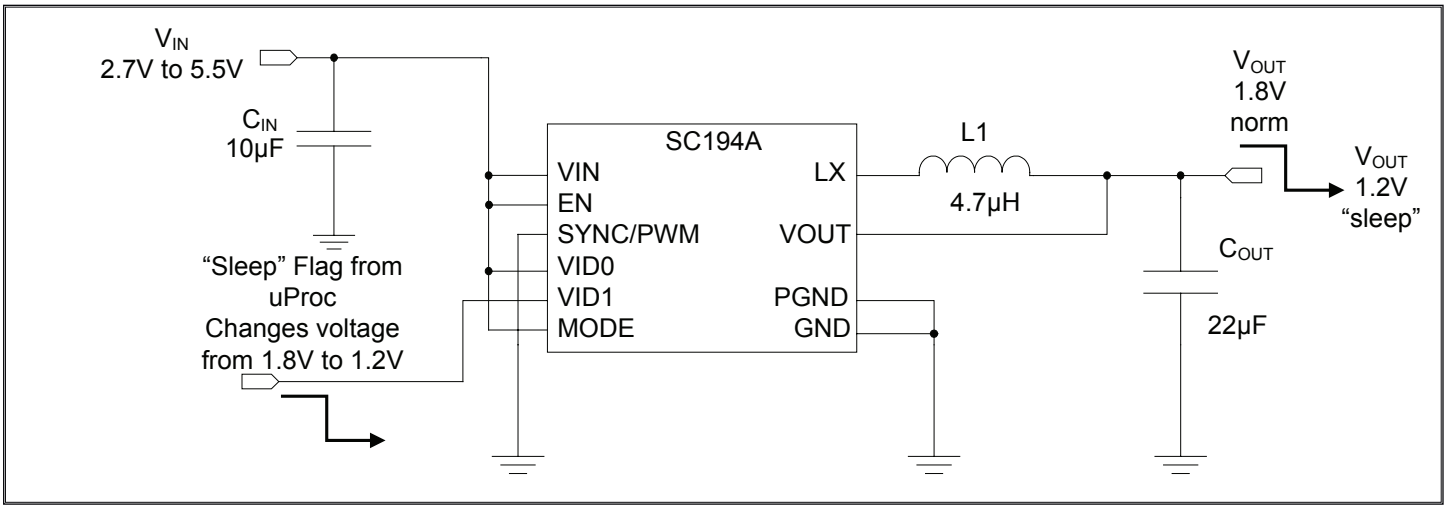

**Time (400us/div)**
Condition $V_{IN}$=3.6V, $V_{OUT}$=1.8V to 1.5V, $I_{OUT}$=1A, SYNC/PWM=$V_{IN}$

## Applications Circuits

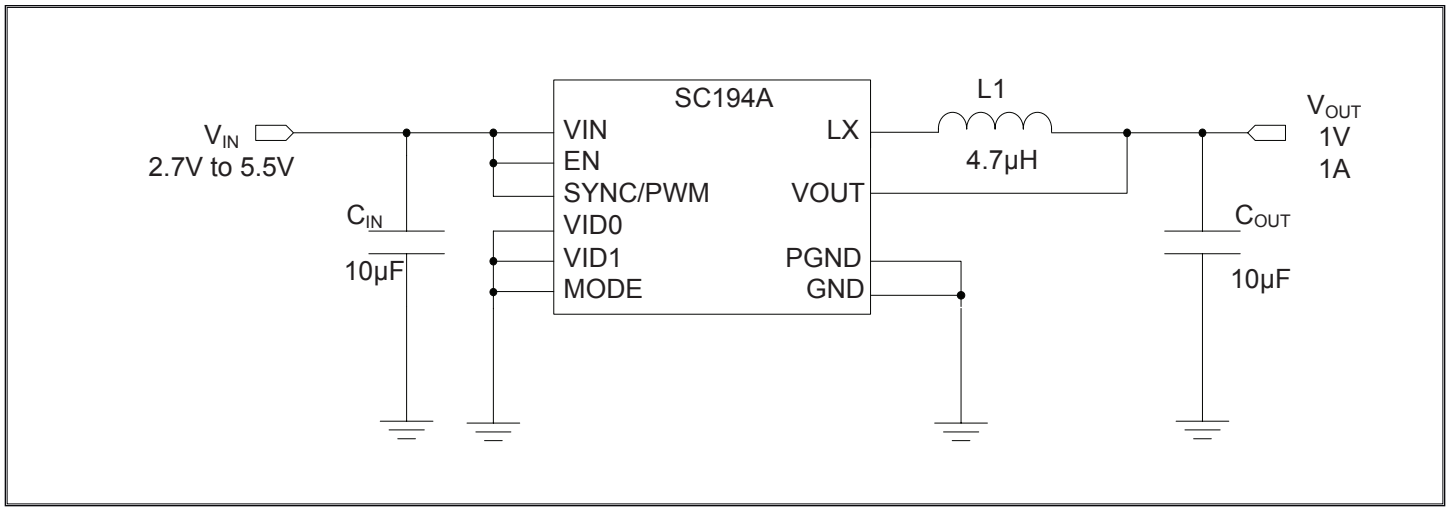
**$V_{OUT}$ = 1.8V with PSAVE and 100% Duty Cycle**



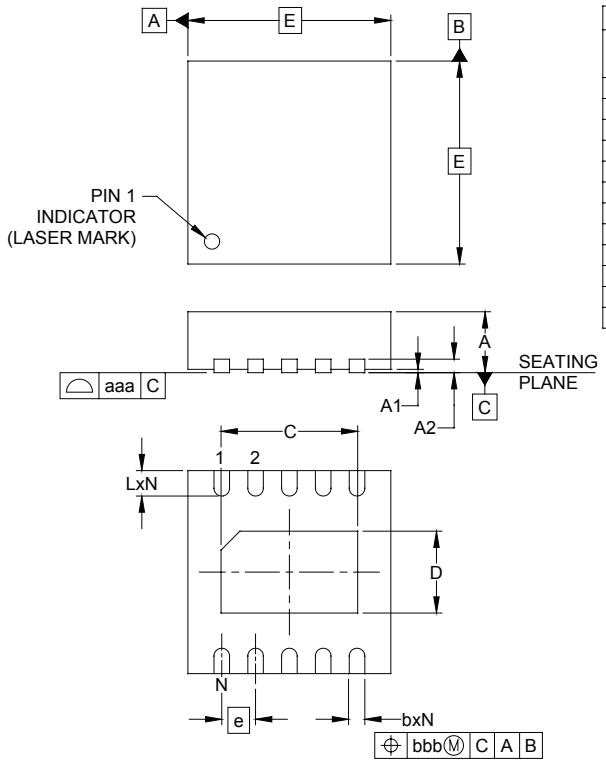

**Mobile Voltage Positioning for Reduced System Dissipation in "Sleep" Modes**




**$V_{OUT}$ = 1.0V with Forced PWM and no 100% Duty Cycle**



## Outline Drawing - MLP-10

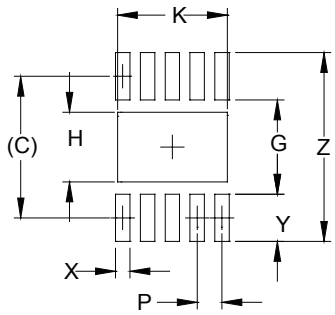



| DIMENSIONS | | | | | | |
|---|---|---|---|---|---|---|
| DIM | INCHES | | | MILLIMETERS | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | .031 | - | .039 | 0.80 | - | 1.00 |
| A1 | .000 | - | .002 | 0.00 | - | 0.05 |
| A2 | - | (.008) | - | - | (0.20) | - |
| b | .007 | .009 | .011 | 0.18 | 0.23 | 0.30 |
| C | .074 | .079 | .083 | 1.87 | 2.02 | 2.12 |
| D | .042 | .048 | .052 | 1.06 | 1.21 | 1.31 |
| E | .114 | .118 | .122 | 2.90 | 3.00 | 3.10 |
| e | .020 BSC | | | 0.50 BSC | | |
| L | .012 | .016 | .020 | 0.30 | 0.40 | 0.50 |
| N | 10 | | | 10 | | |
| aaa | .003 | | | 0.08 | | |
| bbb | .004 | | | 0.10 | | |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

## Land Pattern - MLP-10




| DIMENSIONS | | |
|---|---|---|
| DIM | INCHES | MILLIMETERS |
| C | (.112) | (2.85) |
| G | .075 | 1.90 |
| H | .055 | 1.40 |
| K | .087 | 2.20 |
| P | .020 | 0.50 |
| X | .012 | 0.30 |
| Y | .037 | 0.95 |
| Z | .150 | 3.80 |

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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