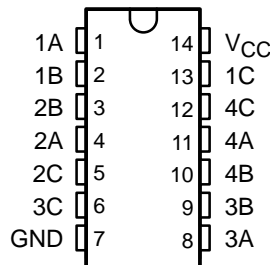


SN74HC4066 QUADRUPLE BILATERAL ANALOG SWITCH

SCLS325G – MARCH 1996 – REVISED JULY 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Typical Switch Enable Time of 18 ns
- Low Power Consumption, 20- μ A Max I_{CC}
- Low Input Current of 1 μ A Max
- High Degree of Linearity
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance . . .
50- Ω TYP at $V_{CC} = 6$ V
- Individual Switch Controls

D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74HC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC4066N | SN74HC4066N |
| | SOIC – D | Tube of 50 | SN74HC4066D | HC4066 |
| | | Reel of 2500 | SN74HC4066DR | |
| | | Reel of 250 | SN74HC4066DT | |
| | SOP – NS | Reel of 2000 | SN74HC4066NSR | HC4066 |
| | SSOP – DB | Reel of 2000 | SN74HC4066DBR | HC4066 |
| | TSSOP – PW | Tube of 90 | SN74HC4066PW | HC4066 |
| | | Reel of 2000 | SN74HC4066PWR | |
| | | Reel of 250 | SN74HC4066PWT | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each switch)

| INPUT CONTROL (C) | SWITCH |
|-------------------|--------|
| L | OFF |
| H | ON |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

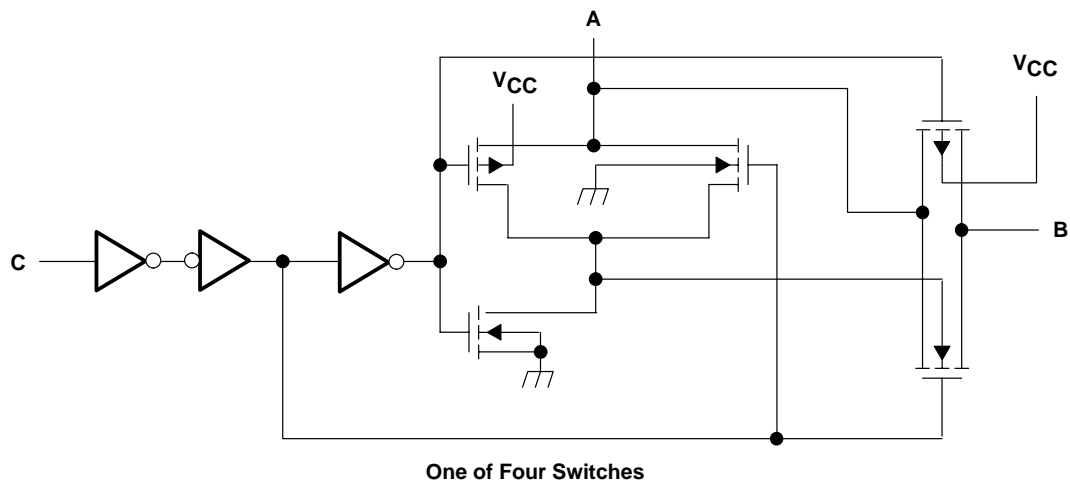
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SN74HC4066
QUADRUPLE BILATERAL ANALOG SWITCH

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logic diagram, each switch (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range, V_{CC} (see Note 1) | –0.5 V to 7 V |
| Control-input diode current, I_I ($V_I < 0$ or $V_I > V_{CC}$) | ± 20 mA |
| I/O port diode current, I_I ($V_I < 0$ or $V_{I/O} > V_{CC}$) | ± 20 mA |
| On-state switch current ($V_{I/O} = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| DB package | 96°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74HC4066

QUADRUPLE BILATERAL ANALOG SWITCH

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recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|------------------|--|-------------------------|------|-----------------|------|
| V _{CC} | Supply voltage | 2 [†] | 5 | 6 | V |
| V _{I/O} | I/O port voltage | 0 | | V _{CC} | V |
| V _{IH} | High-level input voltage, control inputs | V _{CC} = 2 V | 1.5 | V _{CC} | V |
| | | V _{CC} = 4.5 V | 3.15 | V _{CC} | |
| | | V _{CC} = 6 V | 4.2 | V _{CC} | |
| V _{IL} | Low-level input voltage, control inputs | V _{CC} = 2 V | 0 | 0.3 | V |
| | | V _{CC} = 4.5 V | 0 | 0.9 | |
| | | V _{CC} = 6 V | 0 | 1.2 | |
| Δt/Δv | Input transition rise/fall time | V _{CC} = 2 V | | 1000 | ns |
| | | V _{CC} = 4.5 V | | 500 | |
| | | V _{CC} = 6 V | | 400 | |
| T _A | Operating free-air temperature | –40 | | 85 | °C |

[†] With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|--------------------|----------------------------------|--|-----------------|-----------------------|------|------|-----|-------|------|
| | | | | MIN | TYP | MAX | | | |
| r _{on} | On-state switch resistance | I _T = –1 mA, V _I = 0 to V _{CC} , V _C = V _{IH} (see Figure 1) | 2 V | | 150 | | | | Ω |
| | | | 4.5 V | | 50 | 85 | | 106 | |
| | | | 6 V | | 30 | | | | |
| r _{on(p)} | Peak on-state resistance | V _I = V _{CC} or GND, V _C = V _{IH} , I _T = –1 mA | 2 V | | 320 | | | | Ω |
| | | | 4.5 V | | 70 | 170 | | 215 | |
| | | | 6 V | | 50 | | | | |
| I _I | Control input current | V _C = 0 or V _{CC} | 6 V | | ±0.1 | ±100 | | ±1000 | nA |
| I _{soff} | Off-state switch leakage current | V _I = V _{CC} or 0, V _O = V _{CC} or 0, V _C = V _{IL} (see Figure 2) | 6 V | | | ±0.1 | | ±5 | μA |
| I _{son} | On-state switch leakage current | V _I = V _{CC} or 0, V _C = V _{IH} (see Figure 3) | 6 V | | | ±0.1 | | ±5 | μA |
| I _{CC} | Supply current | V _I = 0 or V _{CC} , I _O = 0 | 6 V | | | 2 | | 20 | μA |
| C _i | Input capacitance | A or B | 5 V | | 9 | | | | pF |
| | | C | | | 3 | 10 | | 10 | |
| C _f | Feed-through capacitance | A to B | | | 0.5 | | | | pF |
| C _O | Output capacitance | A or B | 5 V | | 9 | | | | pF |



SN74HC4066

QUADRUPLE BILATERAL ANALOG SWITCH

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switching characteristics over recommended operating free-air temperature range

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|--|-----------------|----------------|---|-----------------|-----------------------|-----|-----|-----|-----|-------------|
| | | | | | MIN | TYP | MAX | | | |
| t _{PLH} , t _{PHL} Propagation delay time | A or B | B or A | C _L = 50 pF (see Figure 4) | 2 V | | 10 | 60 | | 75 | ns |
| | | | | 4.5 V | | 4 | 12 | | 15 | |
| | | | | 6 V | | 3 | 10 | | 13 | |
| t _{PZH} , t _{PZL} Switch turn-on time | C | A or B | R _L = 1 kΩ, C _L = 50 pF (see Figure 5) | 2 V | | 70 | 180 | | 225 | ns |
| | | | | 4.5 V | | 21 | 36 | | 45 | |
| | | | | 6 V | | 18 | 31 | | 38 | |
| t _{PLZ} , t _{PHZ} Switch turn-off time | C | A or B | R _L = 1 kΩ, C _L = 50 pF (see Figure 5) | 2 V | | 50 | 200 | | 250 | ns |
| | | | | 4.5 V | | 25 | 40 | | 50 | |
| | | | | 6 V | | 22 | 34 | | 43 | |
| f _I Control input frequency | C | A or B | C _L = 15 pF, R _L = 1 kΩ, V _C = V _{CC} or GND, V _O = V _{CC} /2 (see Figure 6) | 2 V | | 15 | | | | MHz |
| | | | | 4.5 V | | 30 | | | | |
| | | | | 6 V | | 30 | | | | |
| Control feed-through noise | C | A or B | C _L = 50 pF, R _{in} = R _L = 600 Ω, V _C = V _{CC} or GND, f _{in} = 1 MHz (see Figure 7) | 4.5 V | | 15 | | | | mV (rms) |
| | | | | 6 V | | 20 | | | | |

operating characteristics, V_{CC} = 4.5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|---|-------|------|
| C _{pd} Power dissipation capacitance per gate | C _L = 50 pF, f = 1 MHz | 45 | pF |
| Minimum through bandwidth, A to B or B to A [†] [20 log (V _O /V _I)] = -3 dB | C _L = 50 pF, V _C = V _{CC} , R _L = 600 Ω, (see Figure 8) | 30 | MHz |
| Crosstalk between any switches [‡] | C _L = 10 pF, f _{in} = 1 MHz, R _L = 50 Ω, (see Figure 9) | 45 | dB |
| Feed through, switch off, A to B or B to A [‡] | C _L = 50 pF, f _{in} = 1 MHz, R _L = 600 Ω, (see Figure 10) | 42 | dB |
| Amplitude distortion rate, A to B or B to A | C _L = 50 pF, f _{in} = 1 kHz, R _L = 10 kΩ, (see Figure 11) | 0.05% | |

[†] Adjust the input amplitude for output = 0 dBm at f = 1 MHz. Input signal must be a sine wave.

[‡] Adjust the input amplitude for input = 0 dBm at f = 1 MHz. Input signal must be a sine wave.



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PARAMETER MEASUREMENT INFORMATION

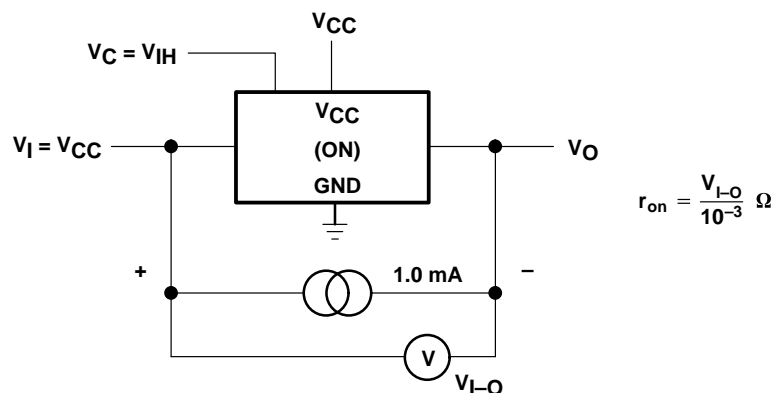


Figure 1. On-State Resistance Test Circuit

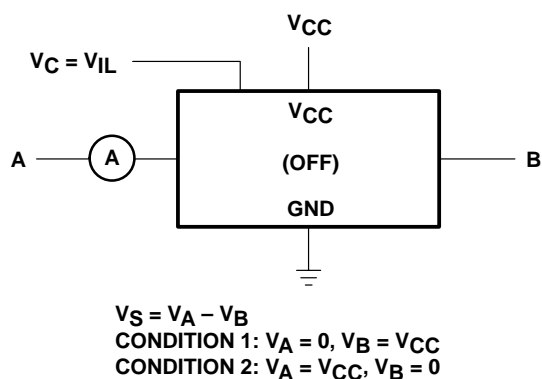


Figure 2. Off-State Switch Leakage-Current Test Circuit

SN74HC4066 QUADRUPLE BILATERAL ANALOG SWITCH

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PARAMETER MEASUREMENT INFORMATION

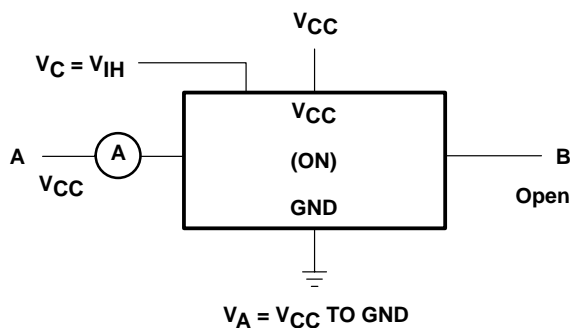


Figure 3. On-State Leakage-Current Test Circuit

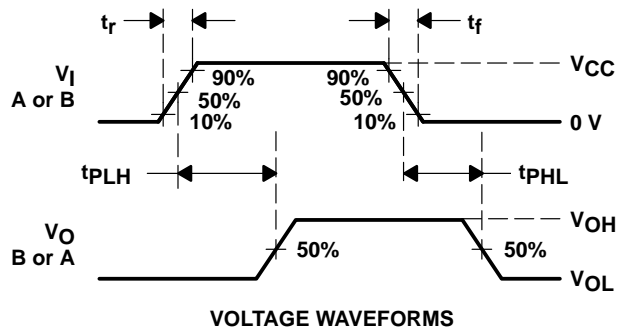
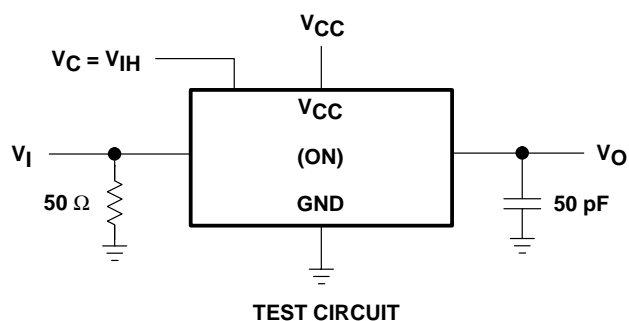
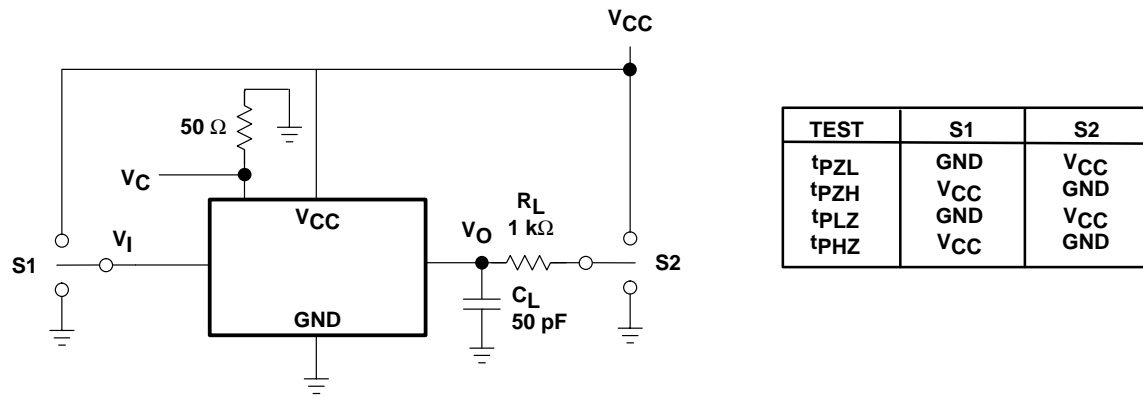
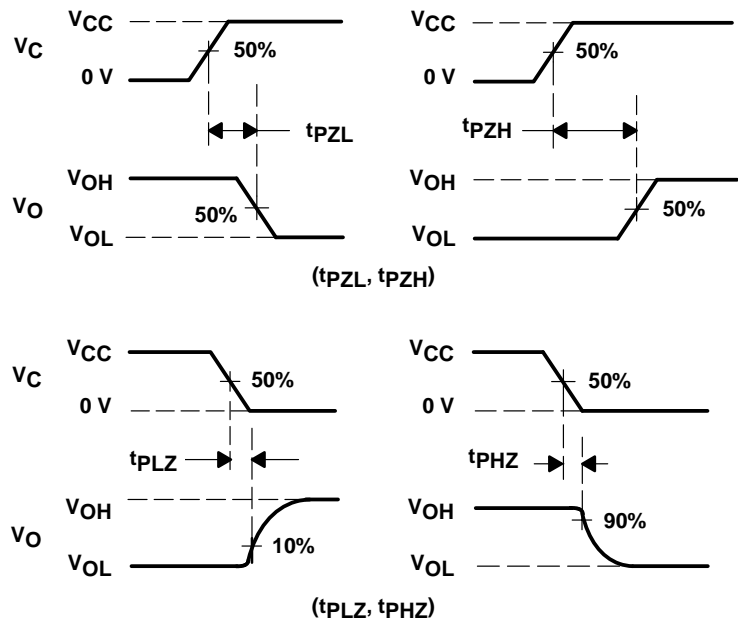


Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (tPZL, tPLZ, tPZH, tPHZ), Control to Signal Output

SN74HC4066 QUADRUPLE BILATERAL ANALOG SWITCH

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PARAMETER MEASUREMENT INFORMATION

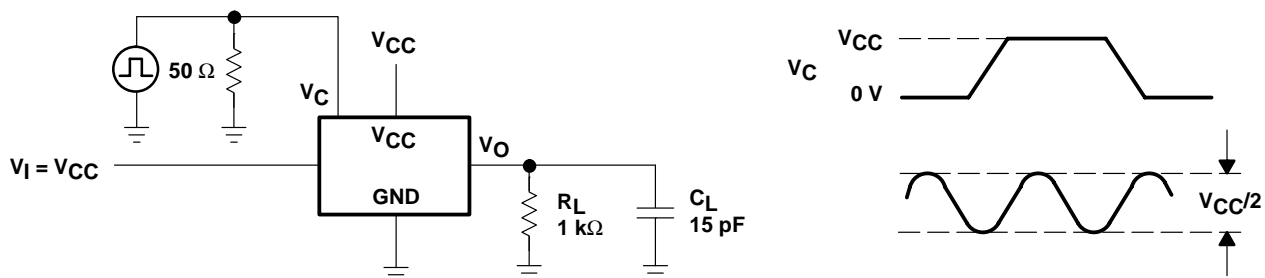


Figure 6. Control-Input Frequency

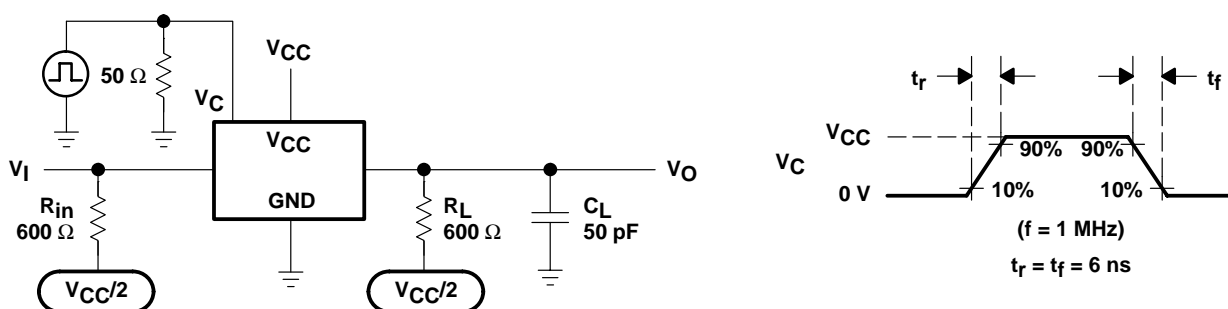


Figure 7. Control Feed-Through Noise

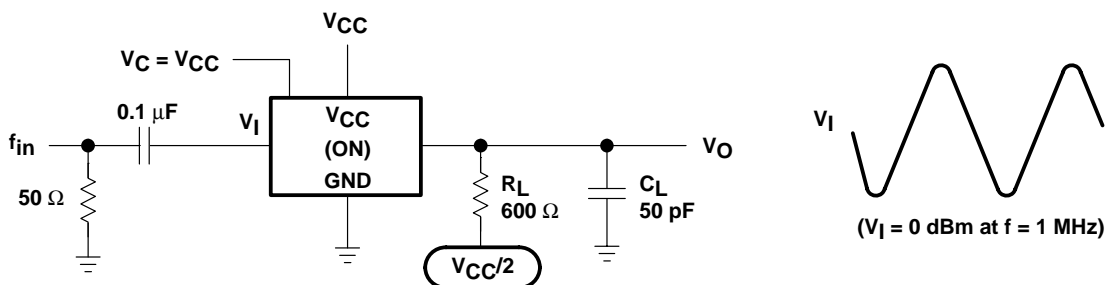


Figure 8. Minimum Through Bandwidth

PARAMETER MEASUREMENT INFORMATION

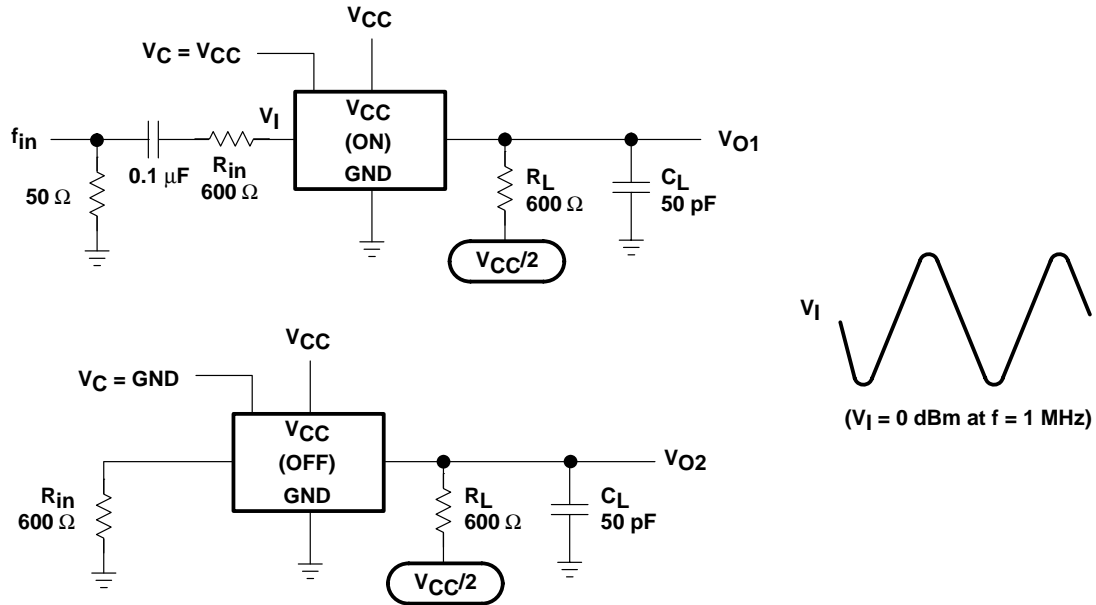


Figure 9. Crosstalk Between Any Two Switches

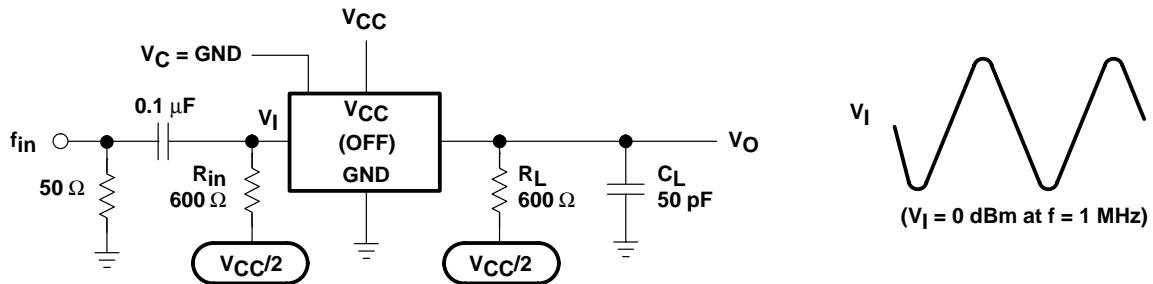


Figure 10. Feed Through, Switch Off

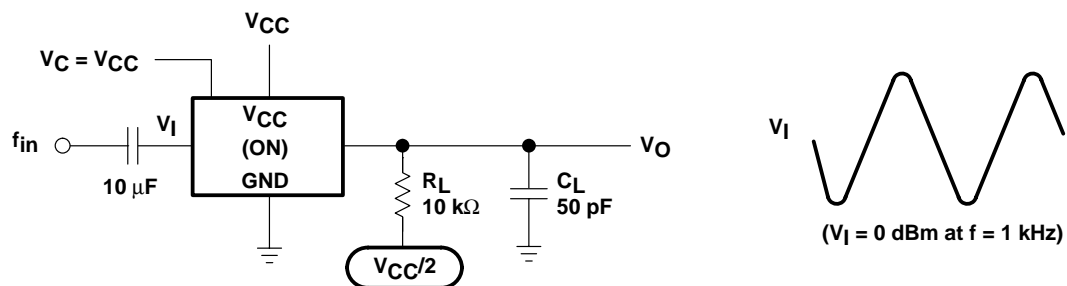


Figure 11. Amplitude-Distortion Rate

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74HC4066D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066DBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HC4066DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066DBRE4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066DT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC4066N | Samples |
| SN74HC4066NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC4066N | Samples |
| SN74HC4066NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066PWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066PWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HC4066PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |
| SN74HC4066PWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC4066 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC4066DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC4066DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC4066DT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC4066NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC4066PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC4066PWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC4066DBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC4066DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74HC4066DT | SOIC | D | 14 | 250 | 367.0 | 367.0 | 38.0 |
| SN74HC4066NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC4066PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HC4066PWT | TSSOP | PW | 14 | 250 | 367.0 | 367.0 | 35.0 |

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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