

TC74HC174AFN

Hex D-Type Flip Flop with Clear

The TC74HC174A is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

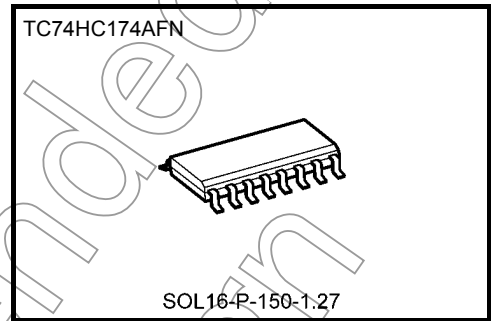
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Information signals applied to the D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{\text{CLR}}$ input is held low, the Q outputs are in the low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Note: xxxFN (JEDEC SOP) is not available in Japan.

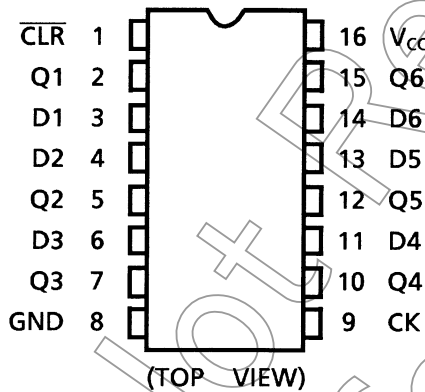


Weight
SOL16-P-150-1.27 : 0.13 g (typ.)

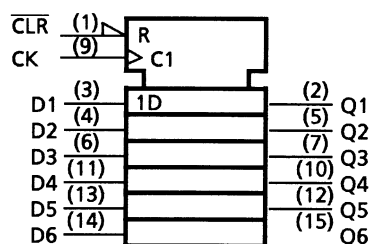
Features

- High speed: $f_{\text{max}} = 71 \text{ MHz (typ.)}$ at $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation: $I_{\text{CC}} = 4 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (min)
- Symmetrical output impedance: $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA (min)}$
- Balanced propagation delays: $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range: $V_{\text{CC (opr)}} = 2\sim 6 \text{ V}$
- Pin and function compatible with 74LS174




Pin Assignment



IEC Logic Symbol

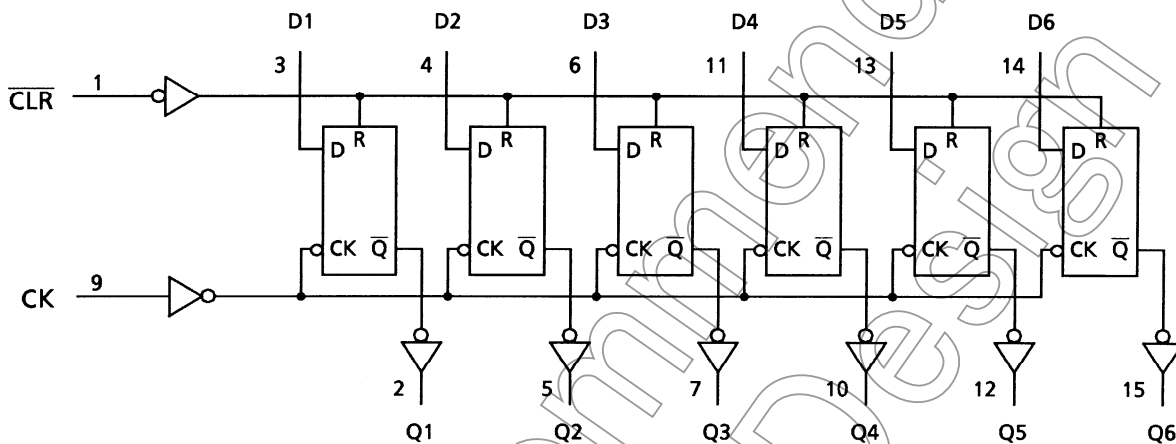


Truth Table

Inputs			Output	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L		L	—
H	H		H	—
H	X		Q_n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5~7	V
DC input voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65~150	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2~6	V
Input voltage	V_{IN}	0~ V_{CC}	V
Output voltage	V_{OUT}	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	t_r, t_f	0~1000 ($V_{CC} = 2.0$ V)	ns
		0~500 ($V_{CC} = 4.5$ V)	
		0~400 ($V_{CC} = 6.0$ V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit		
			V_{CC} (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V_{IH}	—	2.0	1.50	—	—	1.50	V		
			4.5	3.15	—	—	3.15			
			6.0	4.20	—	—	4.20			
Low-level input voltage	V_{IL}	—	2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu\text{A}$	2.0	1.9	2.0	—	1.9	V	
			4.5	4.4	4.5	—	4.4	—		
			6.0	5.9	6.0	—	5.9	—		
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	—	4.13		—
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80	—	5.63		—
			—	6.0	—	—	—	—		—
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
			4.5	—	0.0	0.1	—	0.1		
			6.0	—	0.0	0.1	—	0.1		
			$I_{OL} = 4 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
			$I_{OL} = 5.2 \text{ mA}$	6.0	—	0.18	0.26	—	0.33	
			—	6.0	—	—	—	—	—	
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0	μA	

Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~85°C	Unit
			VCC (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_W (L)$ $t_W (H)$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{\text{CLR}}$)	$t_W (L)$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ($\overline{\text{CLR}}$)	t_{rem}	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	4	5	
Clock frequency	f	—	2.0	—	6	4	MHz
			4.5	—	33	26	
			6.0	—	38	30	

AC Characteristics ($C_L = 15 \text{ pF}$, $V_{CC} = 5 \text{ V}$, $T_a = 25^\circ\text{C}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	—	14	26	ns
Propagation delay time ($\overline{\text{CLR}}$ -Q)	t_{pHL}	—	—	15	26	ns
Maximum clock frequency	f_{max}	—	39	71	—	MHz

AC Characteristics ($C_L = 50 \text{ pF}$, input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	27	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	2.0	—	68	150	—	190	ns
			4.5	—	17	30	—	38	
			6.0	—	14	26	—	32	
Propagation delay time ($\overline{\text{CLR}}-Q$)	t_{pHL}	—	2.0	—	72	150	—	190	ns
			4.5	—	18	30	—	38	
			6.0	—	15	26	—	32	
Maximum clock frequency	f_{max}	—	2.0	6	15	—	4	—	MHz
			4.5	33	59	—	26	—	
			6.0	38	71	—	30	—	
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance	C_{PD} (Note)	—	—	40	—	—	—	pF	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per flip flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

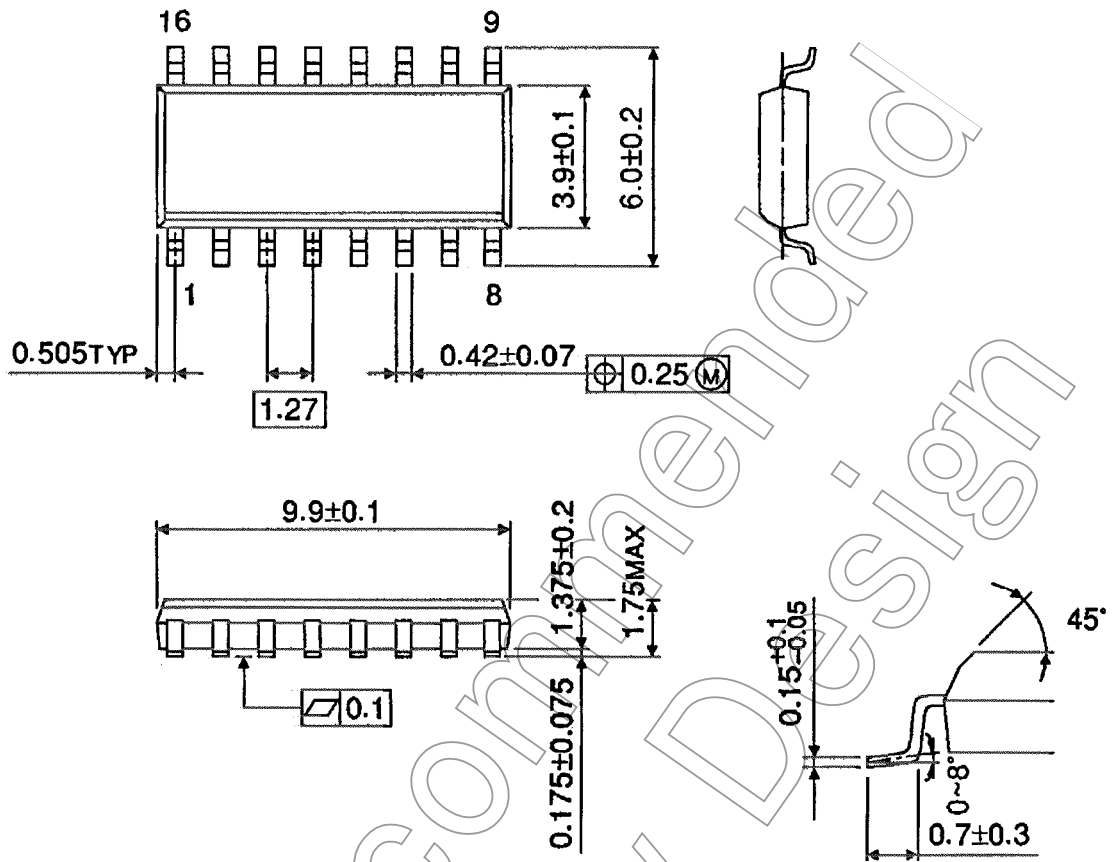
$$C_{PD}(\text{total}) = 28 + 12 \cdot n$$

Not Recommended for New Design

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Not Recommended for New Design

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