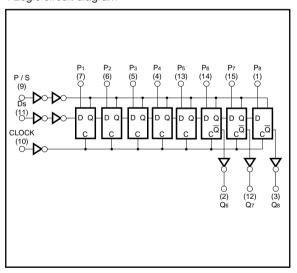
8-bit static shift register BU4021B / BU4021BF

The BU4021B and BU4021BF are 8-bit static shift registers consisting of 8 register cells, each of which has parallel input. Control of the parallel / serial control input (P / S) enables serial input / serial output with clock synchronization, as well as parallel input / serial output conversions.

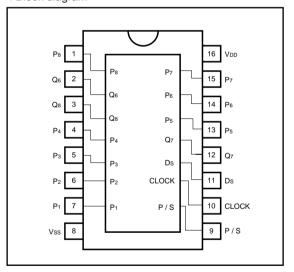
●Absolute maximum ratings (Vss = 0V, Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD}	- 0.3 ~ + 18	V
Power dissipation	Pd	1000 (DIP), 500 (SOP)	mW
Operating temperature	Topr	- 40 ~ + 85	°C
Storage temperature	Tstg	- 55 ~ + 150	°C
Input voltage	Vin	- 0.3 ~ VDD + 0.3	V

■Logic circuit diagram



●Block diagram



Truth tableSerial operation

t	CLOCK	Ds	P/S	$Q_6 $ (t = n + 6)	Q_7 $(t = n + 7)$	$Q_8 $ $(t = n + 8)$
n	<u>_</u>	L	L	0	?	?
n + 1		Н	L	1	0	?
n + 2		L	L	0	1	0
n + 3		Н	L	1	0	1
	_ T _	Х	L	Q ₆	Q ₇	Q ₈

Parallel operation

CLOCK	Ds	P/S	Dm	Q _m *
	Χ	Н	L	L
	Χ	Н	Н	Н

X. Irrelevant

^{*:} Q6, Q7, and Q8 are external

Electrical characteristics

DC characteristics (unless otherwise noted, Ta = 25°C, Vss = 0V)

	Symbol	Min.	Тур.	Max.	Unit	- "	
Parameter						V _{DD} (V)	Conditions
Input high level voltage	ViH	3.5	_	_	V	5	
		7.0	_	_		10	_
		11.0	_	_		15	
		_	_	1.5	V	5	
Input low level voltage	VIL	_	_	3.0		10	_
		_	_	4.0		15	
Input high level current	Iн	_	_	0.3	μΑ	15	V _{IH} = 15V
Input low level current	lı∟	_	_	- 0.3	μΑ	15	VIL = 0V
	Vон	4.95	_	_	V	5	
Output high level voltage		9.95	_	_		10	lo = 0mA
		14.95	_	_		15	
	Vol	_	_	0.05	V	5	Io = 0mA
Output low level voltage		_	_	0.05		10	
		_	_	0.05		15	
	Іон	- 0.16	_	_	mA	5	Voн = 4.6V
Output high level current		- 0.4	_	_		10	Vон = 9.5V
		- 1.2	_	_		15	Vон = 13.5V
Output low level current	loL	0.44	_	_	mA	5	Vol = 0.4V
		1.1	_	_		10	Vol = 0.5V
		3.0	_	_		15	Vol = 1.5V
Static current dissipation	lob	_	_	20	μΑ	5	
		_	_	40		10	Vı = VDD, GND
		_	_	80		15	

Switching characteristics (unless otherwise noted, Vss = 0V, Ta = 25°C, CL = 50pF)

Parameter	Symbol	Min.	Тур.	Max.	Unit	V _{DD} (V)	Conditions	Measurement circuit
Output rise time	t т∟н		180	_	ns	5		Fig.1
		_	90	_		10	_	
		_	65	_		15		
	t _{THL}	_	100	_	ns	5		Fig.1
Output fall time		_	50	_		10	_	
		_	40	_	-	15		
"L" to "H"		_	400	_		5		Fig.1
propagation delay time	t PLH	_	170	_	ns	10	_	
CLOCK to Q, P / S to Q		_	115	_	1	15		
"Ll" to "L "	tрнL	_	400	_		5		Fig.1
"H" to "L" propagation delay time		_	170	_	ns	10	_	
CLOCK to Q, P / S to Q		_	115	_	1	15		
	tsu	_	150	_	ns	5		Fig.1
Setup time		_	50	_		10	<u> </u>	
		_	30	_		15		
	tw (CLK)	_	150	_	ns	5	_	Fig.1
Minimum clock pulse width		_	75	_		10		
paide maii.		_	40	_		15		
	f (CLK) Max.	_	3.0	_	MHz	5	_	Fig.1
Maximum clock frequency		_	6.0	_		10		
noquonoy		_	8.0	_		15		
	tr (CLK) tr (CLK)	_	_	15		5		Fig.1
Maximum clock rise / fall time		_	_	5.0	μs	10	_	
		_	_	4.0		15		
Minimum P / S control pulse width	tw (P/S)	_	150	_	ns	5	_	_
		_	75	_		10		
		_	40	_		15		
Input capacitance	Cin	_	5	_	pF	_		_

Measurement circuit

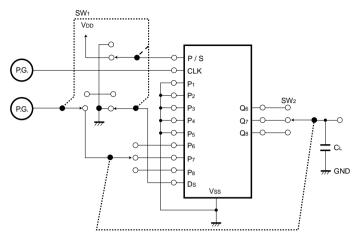


Fig.1 Switching characteristics measurement circuit

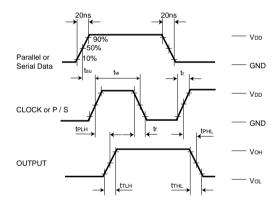


Fig.2 Switching characteristics waveform

•Electrical characteristic curve

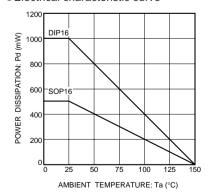
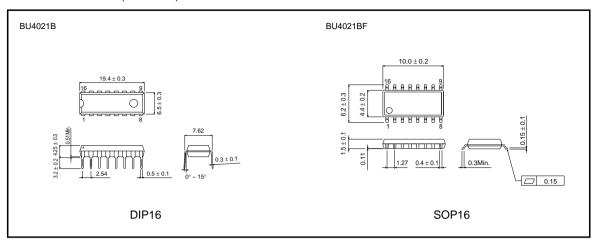


Fig.3 Power dissipation vs. ambient temperature

●External dimensions (Units: mm)



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