

SN54AS194, SN74AS194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

SDAS212A – DECEMBER 1983 – REVISED DECEMBER 1994

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data-Latching Capability
- Package Options Include Plastic Small-Outline Packages (D), Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

These 4-bit bidirectional universal shift registers feature parallel outputs, right-shift and left-shift serial (SR SER, SL SER) inputs, operating-mode-control (S0, S1) inputs, and a direct overriding clear (CLR) line. The registers have four distinct modes of operation:

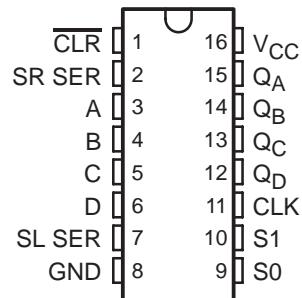
- Inhibit clock (temporary data latch/do nothing)
- Shift right (in the direction QA toward QD)
- Shift left (in the direction QD toward QA)
- Parallel (broadside) load

Parallel synchronous loading is accomplished by applying the four bits of data and taking both S0 and S1 high. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock (CLK) input. During loading, serial data flow is inhibited.

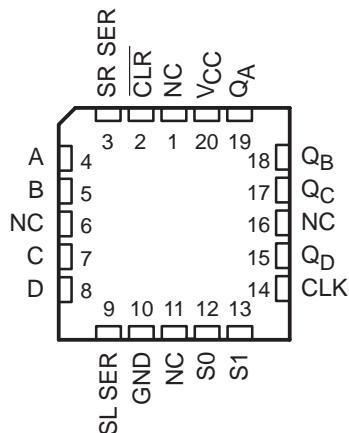
Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode-control inputs are low.

The SN54AS194 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS194 is characterized for operation from 0°C to 70°C .

SN54AS194 . . . J PACKAGE
SN74AS194 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS194 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54AS194, SN74AS194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

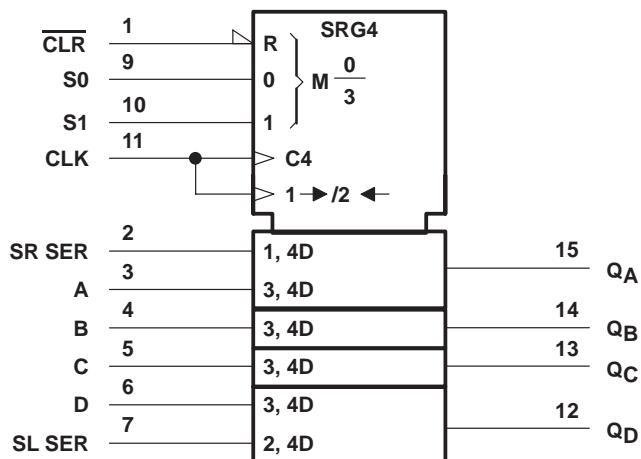
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FUNCTION TABLE

CLR	INPUTS				OUTPUTS								
	MODE		CLK	SERIAL		PARALLEL		QA	QB	QC	QD		
	S1	S0		LEFT	RIGHT	A	B						
L	X	X	X	X	X	X	X	X	L	L	L	L	
H	X	X	L	X	X	X	X	X	QA0	QB0	QC0	QD0	
H	H	H	↑	X	X	a	b	c	a	b	c	d	
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0	

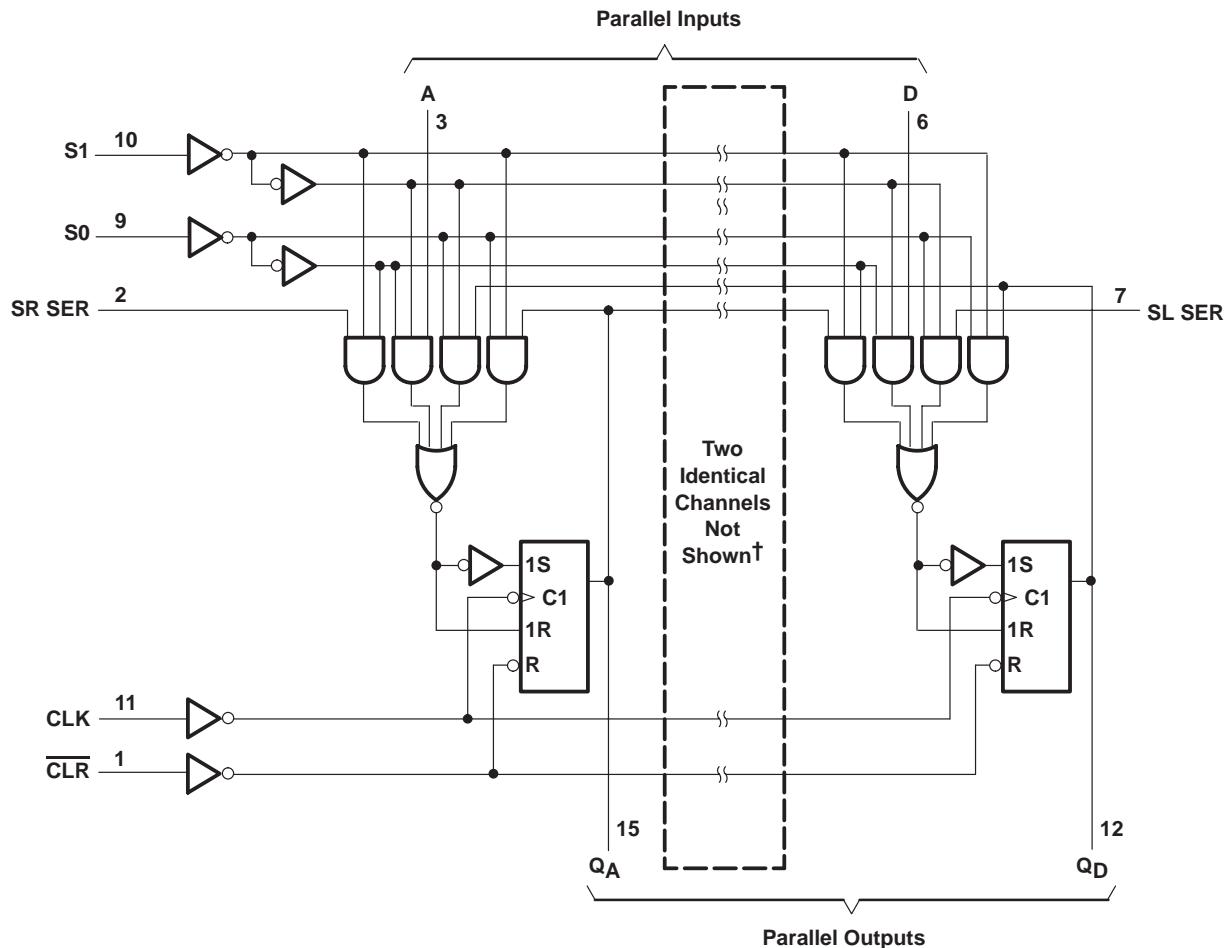
H = high level (steady state); L = low level (steady state); X = irrelevant (any input, including transitions); ↑ = transition from low to high level; a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively; QA0, QB0, QC0, QD0 = the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established; QAn, QBn, QCn, QDn = the level of QA, QB, QC, respectively, before the most recent ↑ transition of the clock.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



† I/O ports not shown: Q_B (14) and Q_C (13)
 Pin numbers shown are for the D, J, and N packages.

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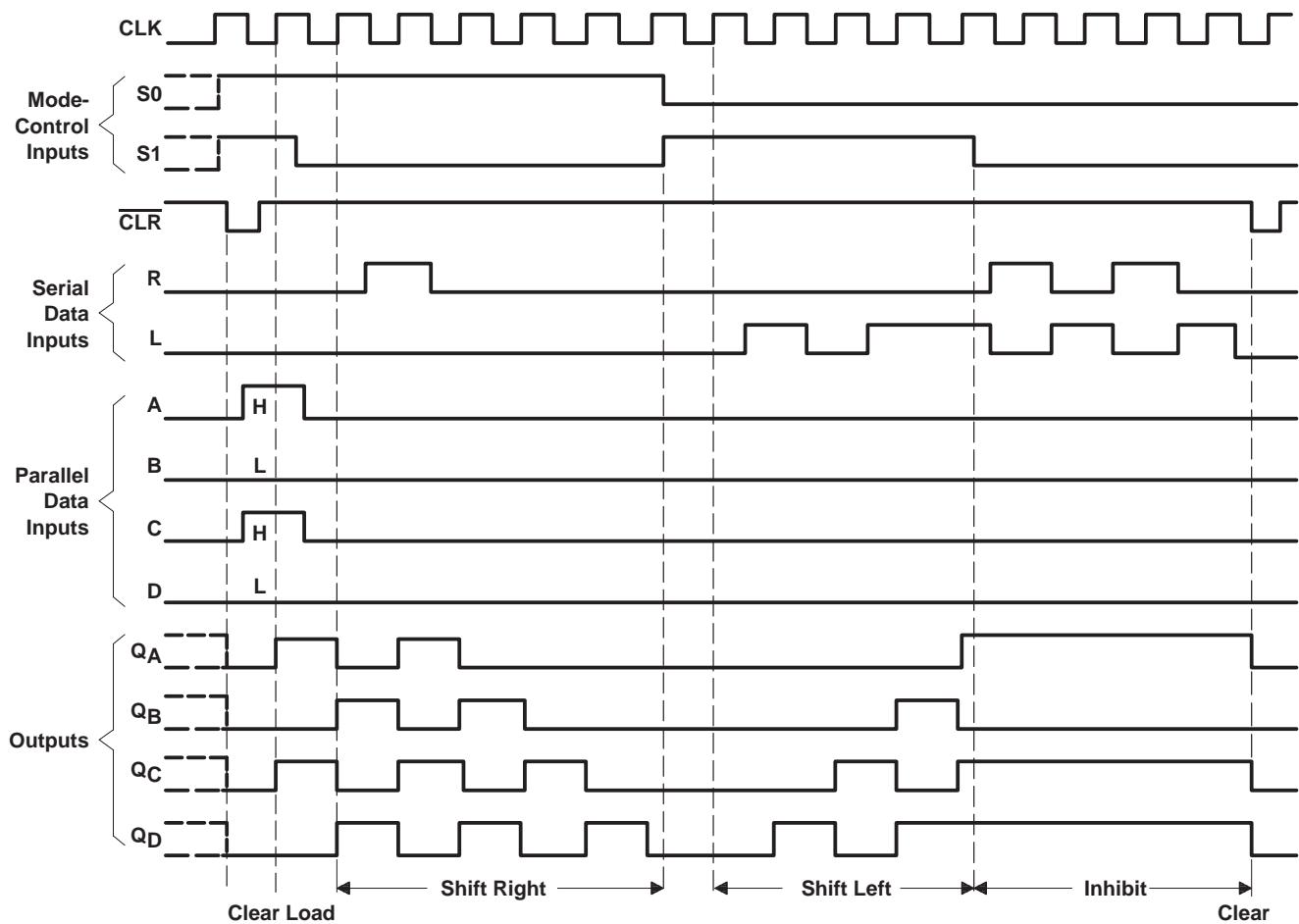


Figure 1. Typical Clear, Load, Right-Shift, and Clear Sequences

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54AS194	-55°C to 125°C
SN74AS194	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

			SN54AS194			SN74AS194			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{OH}	High-level output current				-2			-2	mA
I _{OL}	Low-level output current				20			20	mA
f _{clock} *	Clock frequency		0	75	0	0	75	80	MHz
t _w *	Pulse duration	CLR	4			4.5			ns
		CLK high	4			4			
		CLK low	6			7			
t _{su} *	Setup time before CLK↑	Select	9			9.5			ns
		Data	3.5			4			
		Clear inactive state	6			6			
t _h *	Hold time, data after CLK↑		0.5			0.5			ns
T _A	Operating free-air temperature		-55	125	0	0	70	70	°C

* On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data, but are not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS194			SN74AS194			UNIT
		MIN	TYPT†	MAX	MIN	TYPT†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA	0.35	0.5		0.35	0.5		V
I _I	Data, CLK, CLR Mode, SL, SR	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1	mA
				0.2			0.2	
I _{IH}	Data, CLK, CLR Mode, SL, SR	V _{CC} = 5.5 V, V _I = 2.7 V		20			20	μA
				40			40	
I _{IL}	Data, CLK, CLR Mode, SL, SR	V _{CC} = 5.5 V, V _I = 0.4 V		-0.5			-0.5	mA
				-1			-1	
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112	-30	-112		mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	30	49	30	43	mA	
		Outputs low	38	60	38	53		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R_L = 500\text{ }\Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN54AS194		SN74AS194			
			MIN	MAX	MIN	MAX		
f_{max}^*			75	80			MHz	
t_{PLH}	CLK	Any Q	2.5	8	3	7	ns	
t_{PHL}			2.5	8	3	7		
t_{PHL}	CLR	Any Q	3.5	13	4	12	ns	

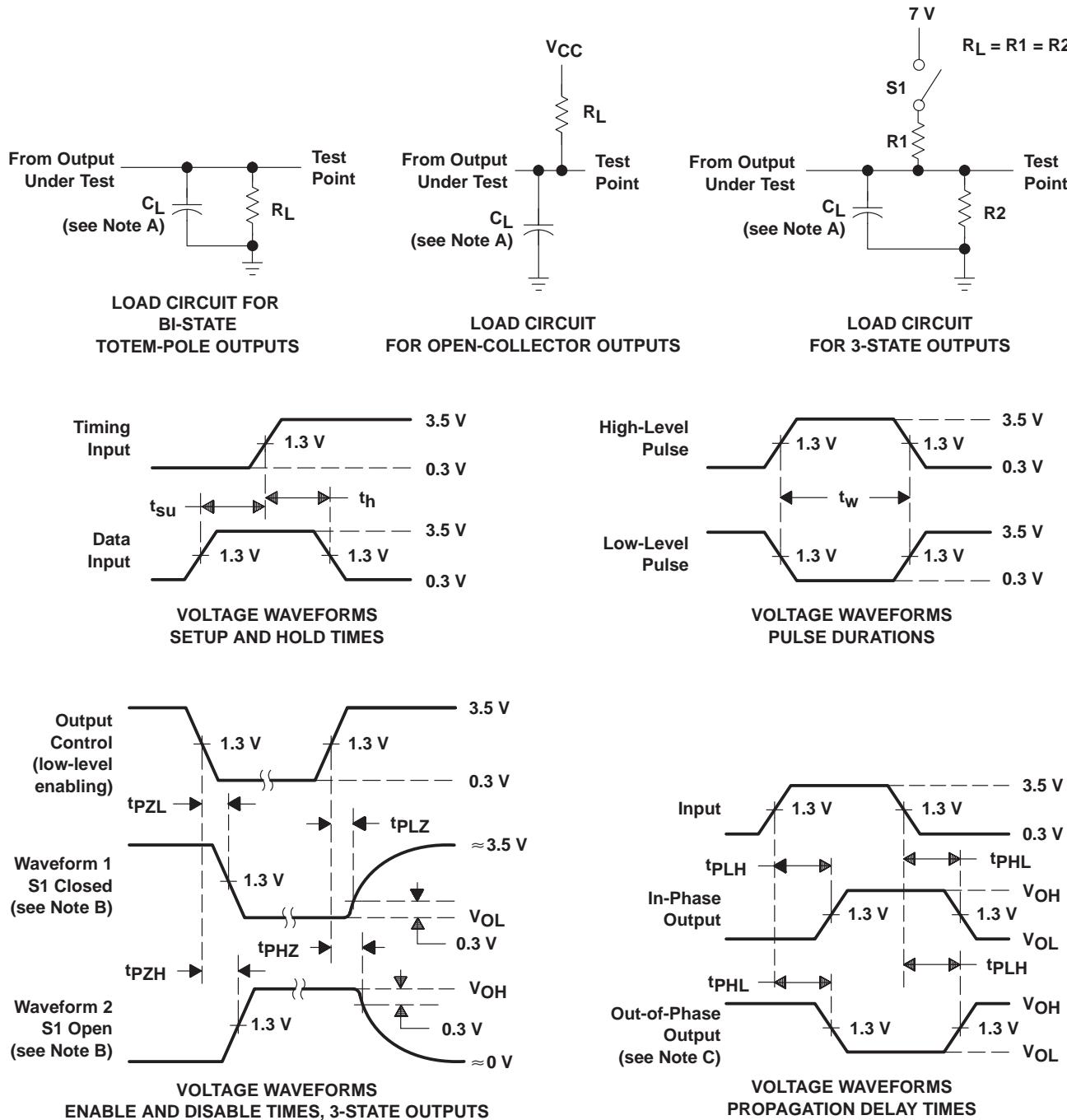
* On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data, but are not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AS194D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS194DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS194DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS194DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS194DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS194DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS194N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS194NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54AS194FK	OBsolete	LCCC	FK	20		TBD	Call TI	Call TI	
SNJ54AS194J	OBsolete	CDIP	J	16		TBD	Call TI	Call TI	
SNJ54AS194W	OBsolete	CFP	W	16		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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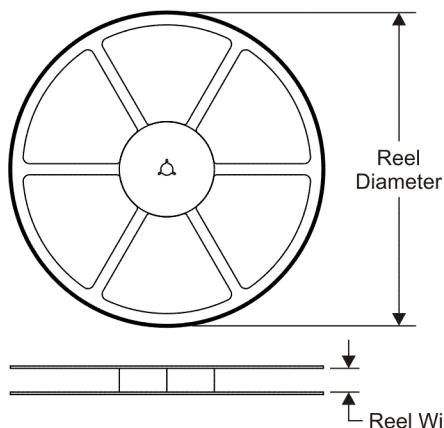
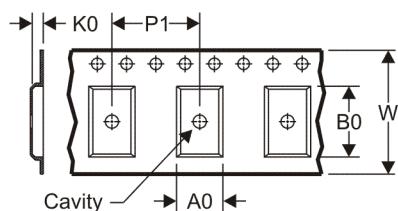
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OTHER QUALIFIED VERSIONS OF SN54AS194, SN74AS194 :

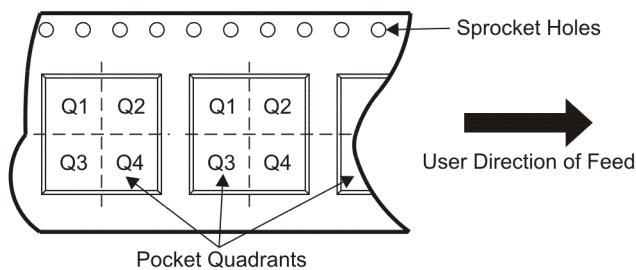
- Catalog: [SN74AS194](#)
- Military: [SN54AS194](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


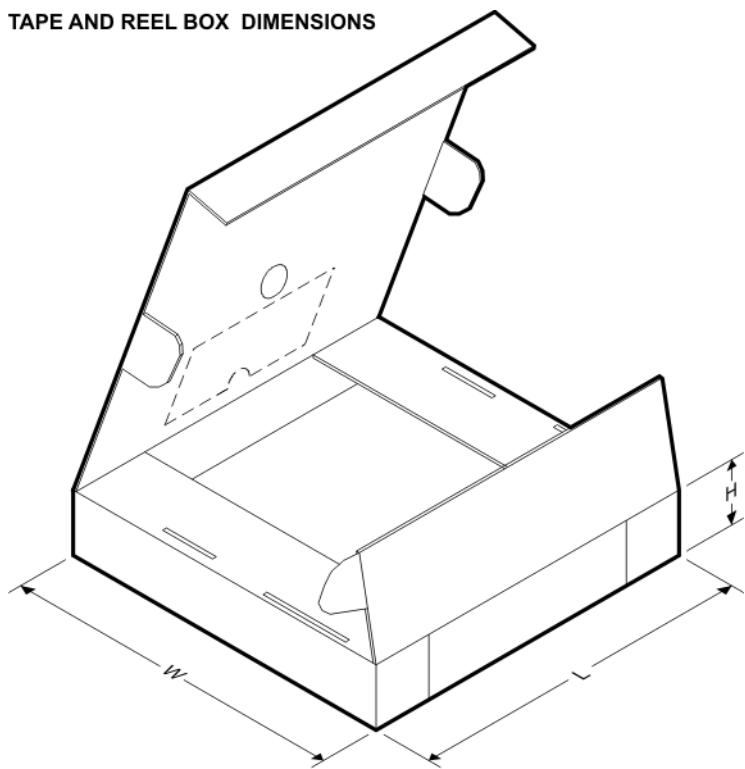
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS194DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



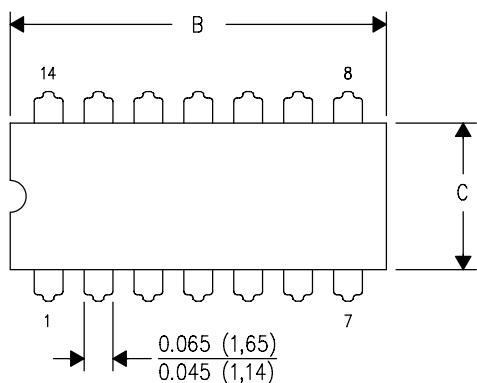
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AS194DR	SOIC	D	16	2500	333.2	345.9	28.6

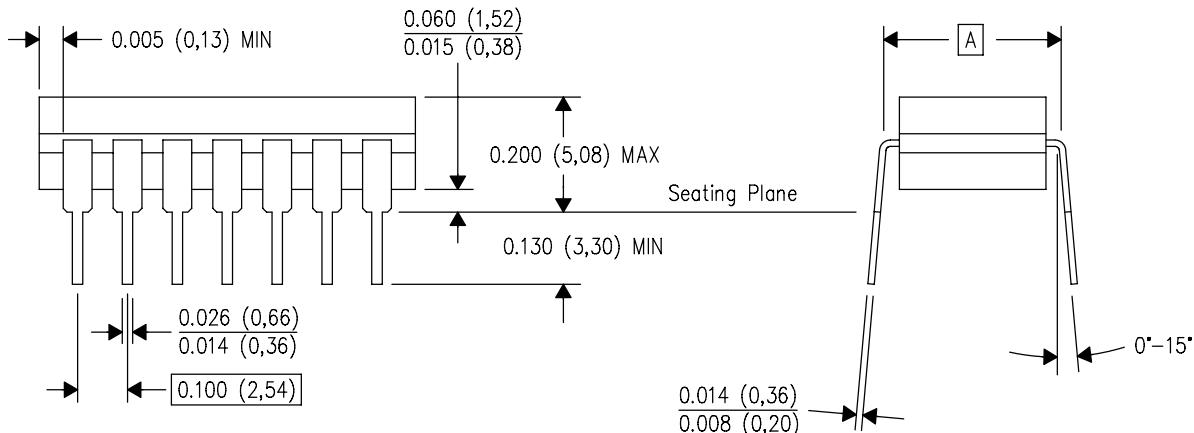
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

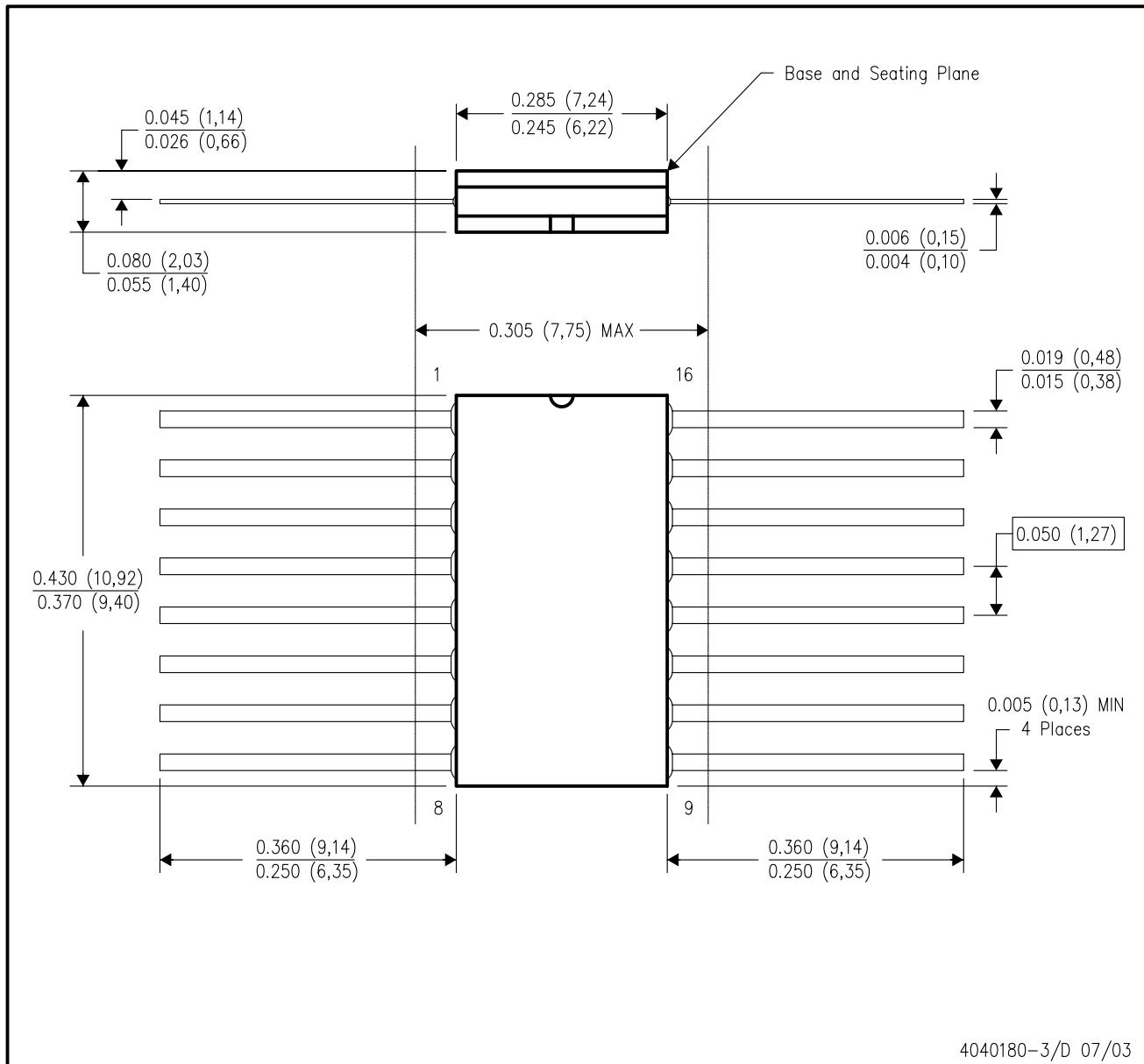


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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

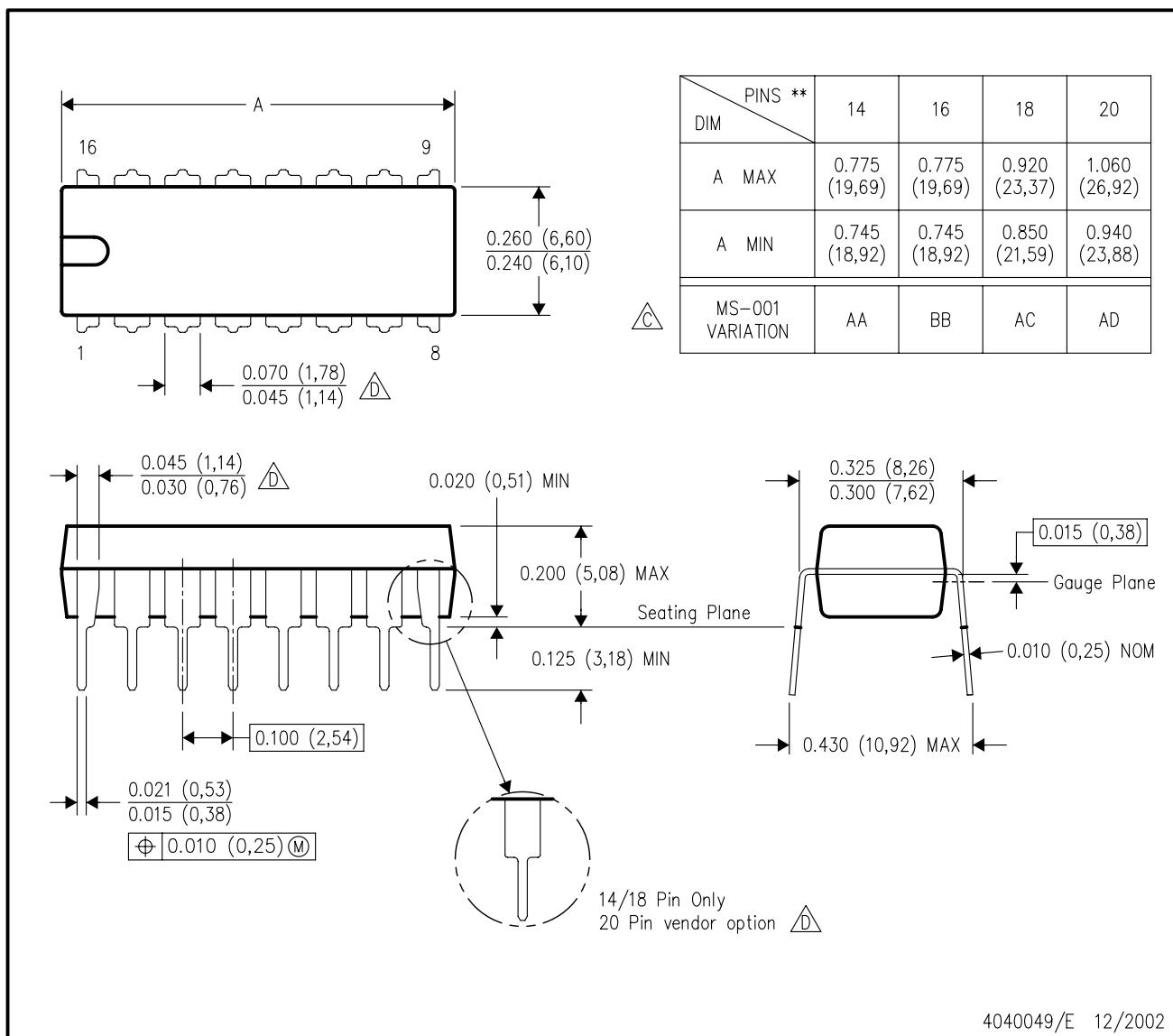
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

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N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



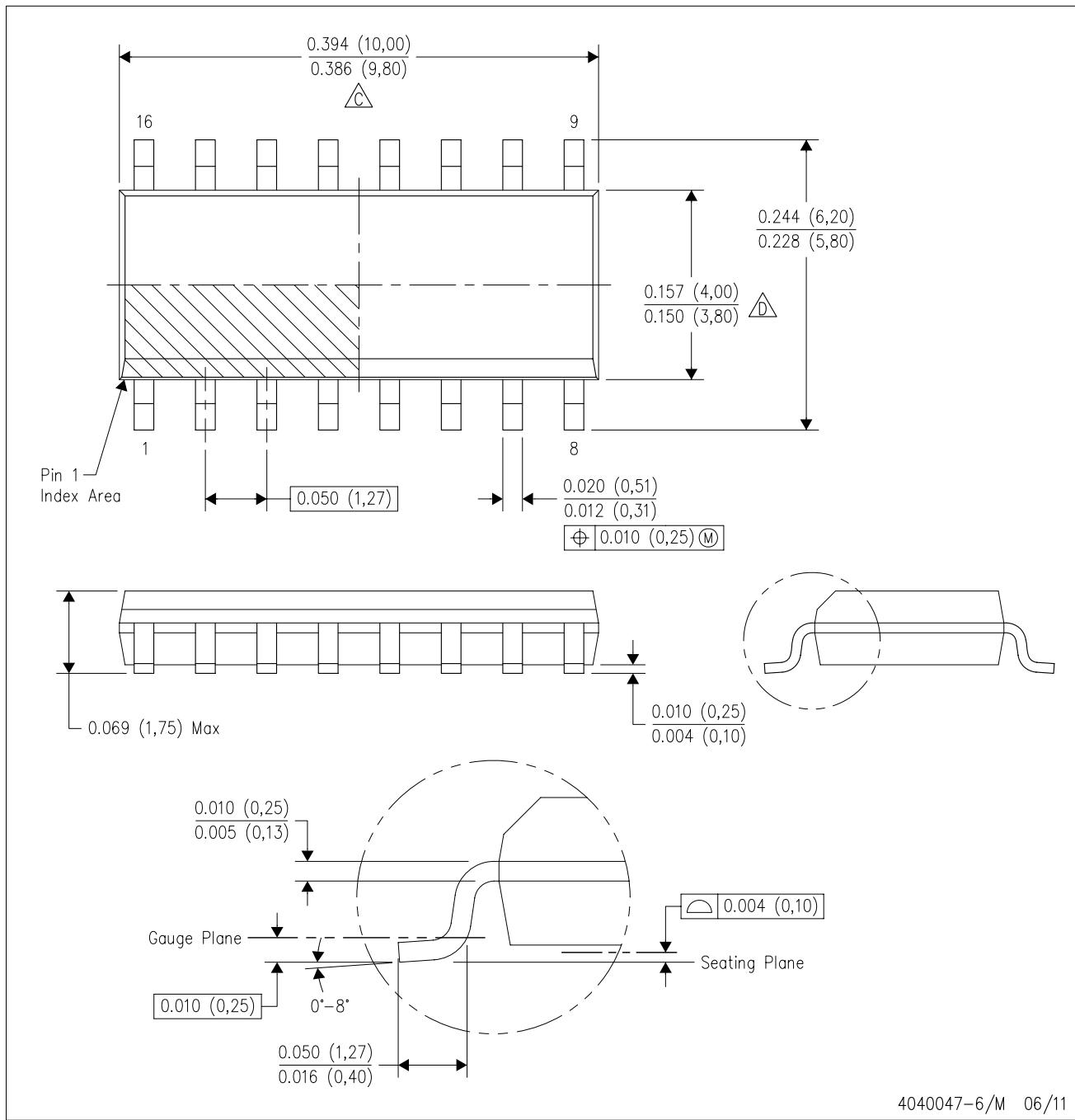
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

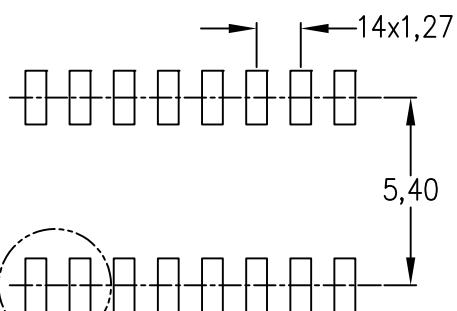
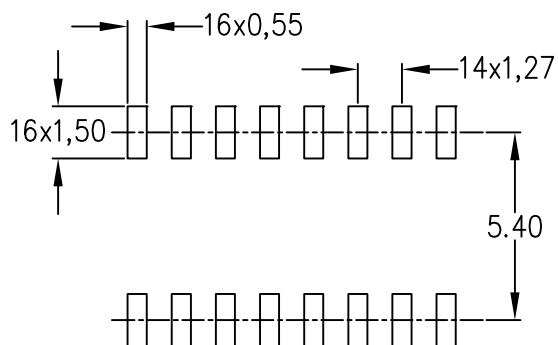
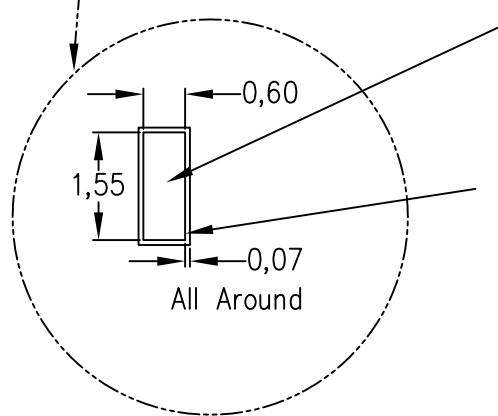
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

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NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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