

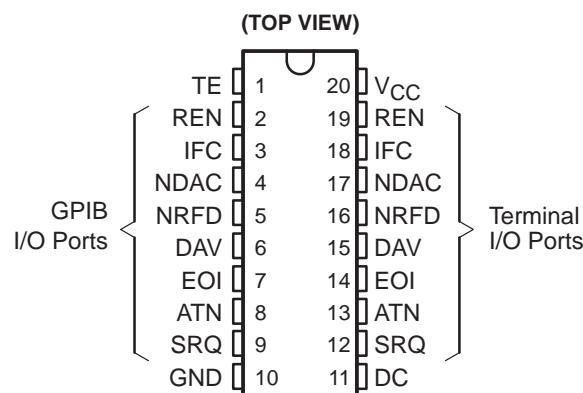
- Meets IEEE Standard 488-1978 (GPIB)
- 8-Channel Bidirectional Transceivers
- Power-Up/Power-Down Protection (Glitch Free)
- Designed to Implement Control Bus Interface
- SN75161B Designed for Single Controller
- SN75162B Designed for Multiple Controllers
- High-Speed, Low-Power Schottky Circuitry
- Low Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down ( $V_{CC} = 0$ )

### description

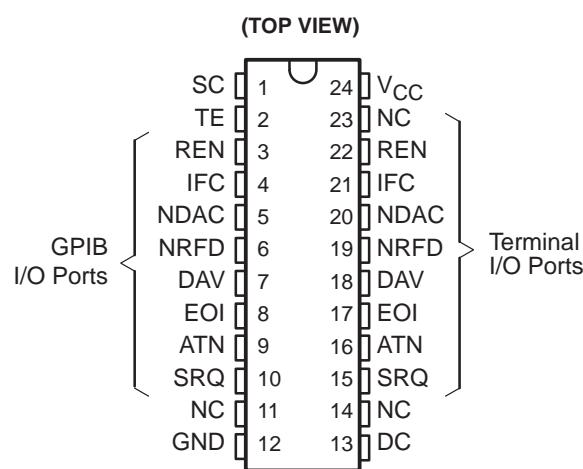
The SN75161B and SN75162B eight-channel, general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE-488 bus.

The SN75161B and SN75162B feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power-up/down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during  $V_{CC}$  power up and power down.

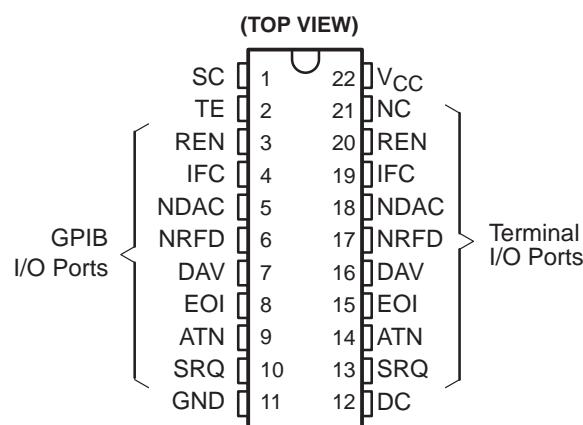
### SN75161B . . . DW OR N PACKAGE



### SN75162B . . . DW PACKAGE



### SN75162B . . . N PACKAGE



NC—No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN75161B, SN75162B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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## description (continued)

The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage  $V_{CC}$  is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

## Function Tables

SN75161B RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS			
DC	TE	ATN <sup>†</sup>	ATN <sup>†</sup>	SRQ	REN	IFC	EOI	DAV	NDAC	NRF
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

<sup>†</sup> ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

SN75162B RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS							
SC	DC	TE	ATN <sup>†</sup>	ATN <sup>†</sup>	SRQ	REN	IFC	EOI	DAV	NDAC	NRF			
H	H	H	R	T				T	T	R	R			
	H	H						R						
	L	L	T	R				R	R	T	T			
	L	L						T						
	H	L	X	R	T			R	R	T	T			
	L	H	X	T	R			T	T	R	R			
H						T	T							
L						R	R							

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

<sup>†</sup> ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

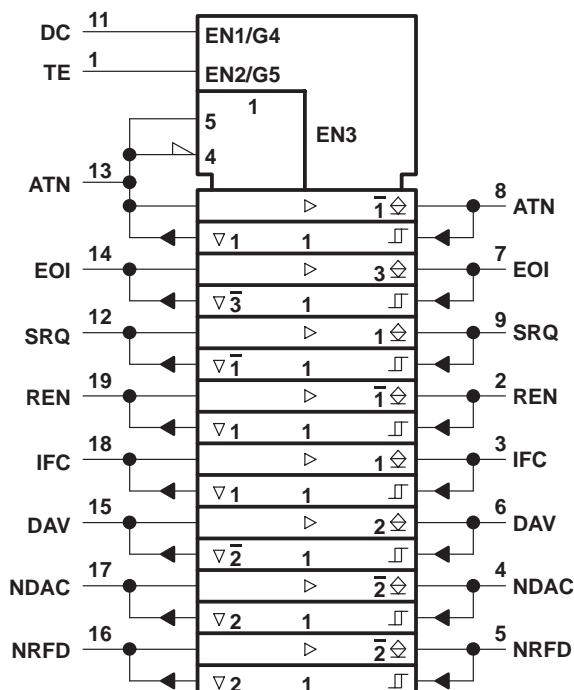
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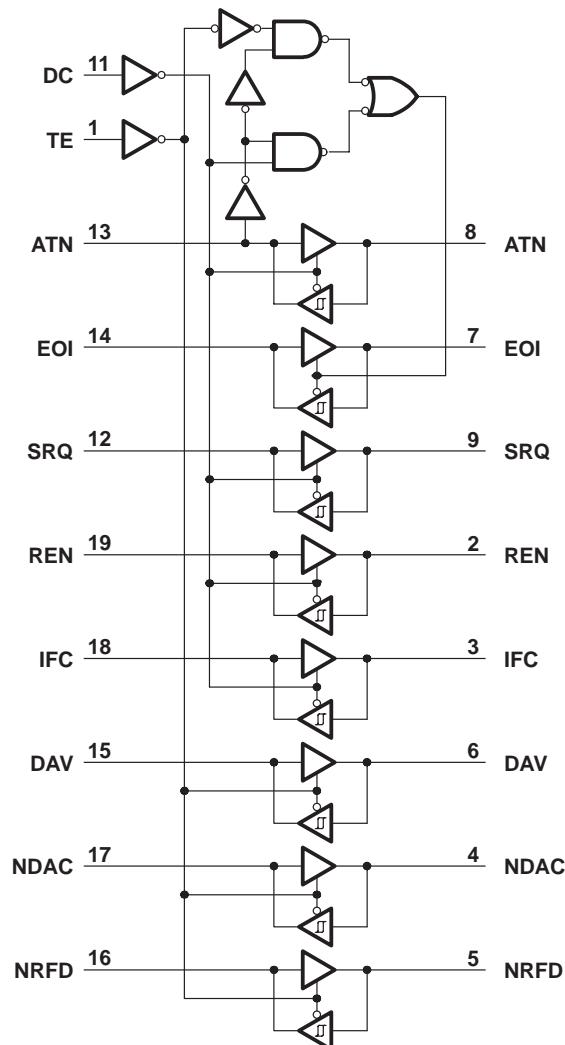
CHANNEL-IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	
TE	Talk Enable	Control
SC	System Control (SN75162B only)	
ATN	Attention	
SRQ	Service Request	
REN	Remote Enable	Bus
IFC	Interface Clear	Management
EOI	End of Identity	
DAV	Data Valid	
NDAC	Not Data Accepted	Data
NRFD	Not Ready for Data	Transfer

**SN75161B logic symbol†**



**SN75161B logic diagram (positive logic)**



†This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.

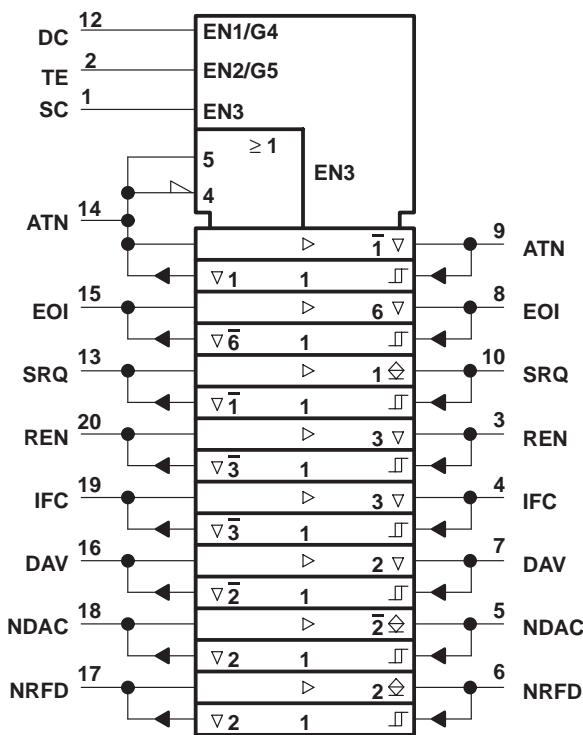
▽ Designates 3-state outputs

◇ Designates passive-pullup outputs

# SN75161B, SN75162B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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## SN75162B logic symbol†

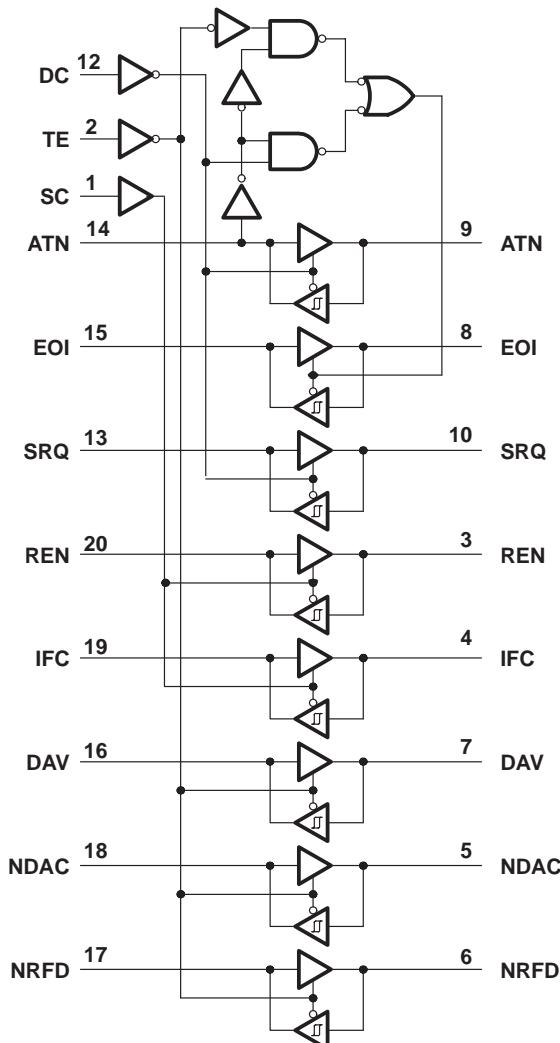


†This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.

▽ Designates 3-state outputs

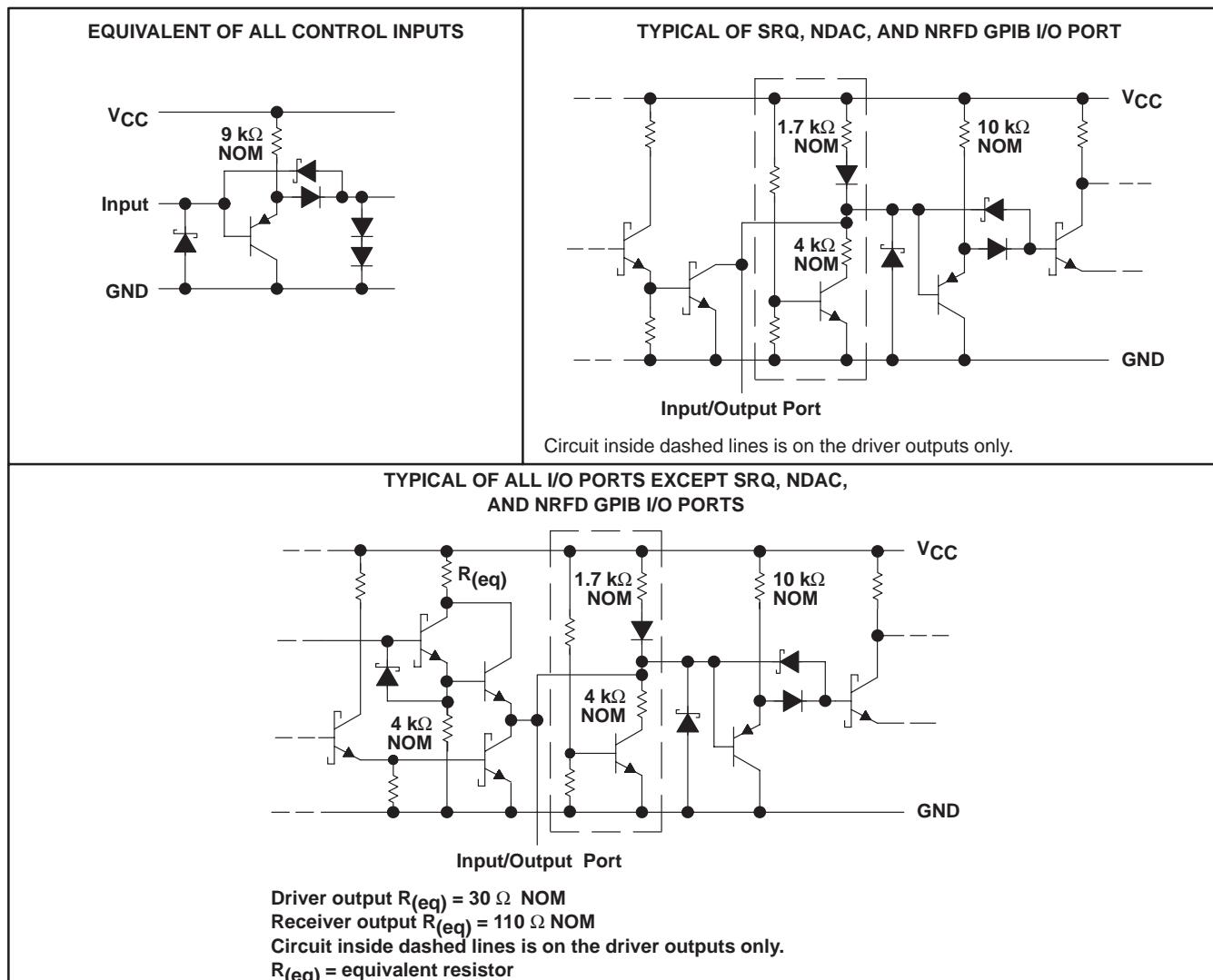
▷ Designates passive-pullup outputs

## SN75162B logic diagram (positive logic)



Pin numbers shown are for the N package.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$	5.5 V
Low-level driver output current, $I_{OL}$	100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1.6 mm (1/16) inch from the case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

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DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW (20 pin)	1125 mW	9.0 mW/ $^\circ\text{C}$	720 mW
DW (24 pin)	1350 mW	10.8 mW/ $^\circ\text{C}$	864 mW
N (20 pin)	1150 mW	9.2 mW/ $^\circ\text{C}$	736 mW
N (22 pin)	1700 mW	13.6 mW/ $^\circ\text{C}$	1088 mW

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
High-level input voltage, $V_{IH}$		2			V
Low-level input voltage, $V_{IL}$				0.8	V
High-level output current, $I_{OH}$	Bus ports with 3-state outputs			-5.2	mA
	Terminal ports			-800	$\mu\text{A}$
Low-level output current, $I_{OL}$	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, $T_A$		0	70		$^\circ\text{C}$

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage		$I_I = -18 \text{ mA}$		-0.8	-1.5	V
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )	Bus	See Figure 7	0.4	0.65		V
$V_{OH}^{\ddagger}$	High-level output voltage	Terminal	$I_{OH} = -800 \mu\text{A}$	2.7	3.5		V
		Bus	$I_{OH} = -5.2 \text{ mA}$	2.5	3.3		
$V_{OL}$	Low-level output voltage	Terminal	$I_{OL} = 16 \text{ mA}$		0.3	0.5	V
		Bus	$I_{OL} = 48 \text{ mA}$		0.35	0.5	
$I_I$	Input current at maximum input voltage	Terminal	$V_I = 5.5 \text{ V}$		0.2	100	$\mu\text{A}$
$I_{IH}$	High-level input current	Terminal and control inputs	$V_I = 2.7 \text{ V}$	0.1	20		$\mu\text{A}$
$I_{IL}$	Low-level input current		$V_I = 0.5 \text{ V}$	-10	-100		$\mu\text{A}$
$V_{I/O(\text{bus})}$	Voltage at bus port	Driver disabled	$I_I(\text{bus}) = 0$	2.5	3.0	3.7	V
			$I_I(\text{bus}) = -12 \text{ mA}$			-1.5	
$I_{I/O(\text{bus})}$	Current into bus port	Power on	$V_I(\text{bus}) = -1.5 \text{ V to } 0.4 \text{ V}$	-1.3			mA
			$V_I(\text{bus}) = 0.4 \text{ V to } 2.5 \text{ V}$	0		-3.2	
			$V_I(\text{bus}) = 2.5 \text{ V to } 3.7 \text{ V}$		2.5		
			$V_I(\text{bus}) = 3.7 \text{ V to } 5 \text{ V}$	0		2.5	
			$V_I(\text{bus}) = 5 \text{ V to } 5.5 \text{ V}$	0.7		2.5	
		Power off	$V_{CC} = 0, V_I(\text{bus}) = 0 \text{ V to } 2.5 \text{ V}$		-40		$\mu\text{A}$
$I_{OS}$	Short-circuit output current	Terminal		-15	-35	-75	mA
		Bus		-25	-50	-125	
$I_{CC}$	Supply current	No load, TE, DE, and SC low				110	mA
$C_{I/O(\text{bus})}$	Bus-port capacitance	$V_{CC} = 5 \text{ V to } 0, V_{I/O} = 0 \text{ to } 2 \text{ V}, f = 1 \text{ MHz}$			16		pF

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡  $V_{OH}$  applies for 3-state outputs only.

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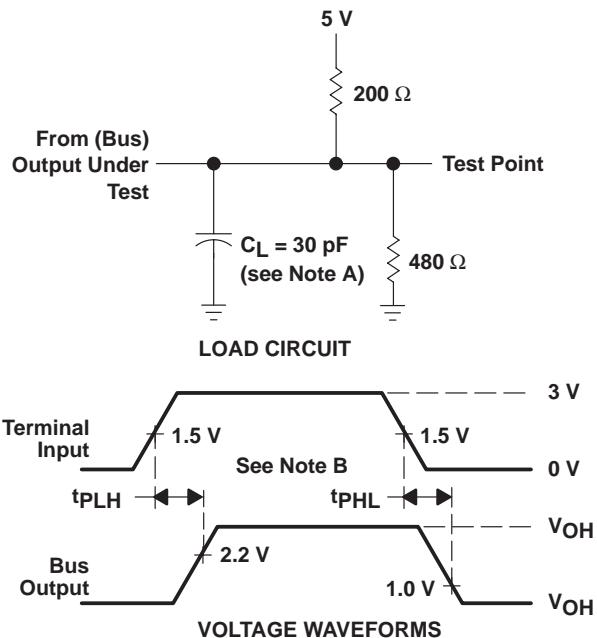
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**switching characteristics,  $V_{CC} = 5$  V,  $C_L = 15$  pF,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

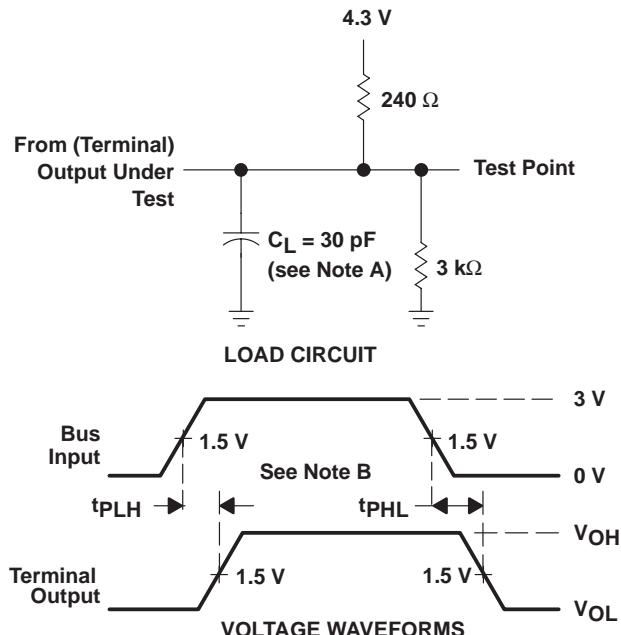
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	Terminal	Bus	$C_L = 30$ pF, See Figure 1	14	20	ns	
$t_{PHL}$ Propagation delay time, high- to low-level output							
$t_{PLH}$ Propagation delay time, low- to high-level output	Terminal	Bus (SRQ, NDAC, NRFD)	$C_L = 30$ pF, See Figure 1	29	35	ns	
$t_{PLH}$ Propagation delay time, low- to high-level output	Bus	Terminal	$C_L = 30$ pF, See Figure 2	10	20	ns	
$t_{PHL}$ Propagation delay time, high- to low-level output							
$t_{PZH}$ Output enable time to high level	TE,DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	See Figure 3	60	ns		
$t_{PHZ}$ Output disable time from high level							
$t_{PZL}$ Output enable time to low level							
$t_{PLZ}$ Output disable time from low level							
$t_{PZH}$ Output enable time to high level	TE,DC, or SC	Terminal	See Figure 4	55	ns		
$t_{PHZ}$ Output disable time from high level							
$t_{PZL}$ Output enable time to low level							
$t_{PLZ}$ Output disable time from low level							

PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms



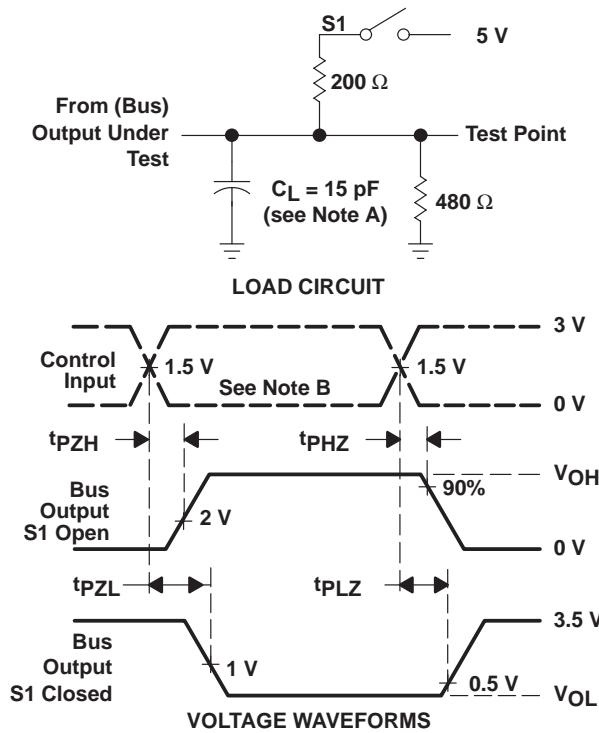
NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

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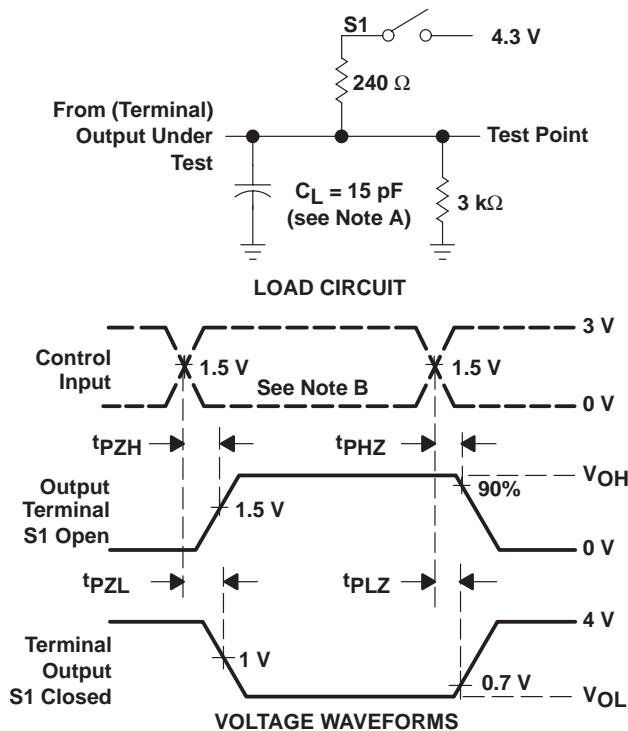
## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 1 \text{ MHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .

Figure 3. Bus Enable and Disable Times Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The Input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

Figure 4. Terminal Enable and Disable Times Load Circuit and Voltage Waveforms

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## TYPICAL CHARACTERISTICS

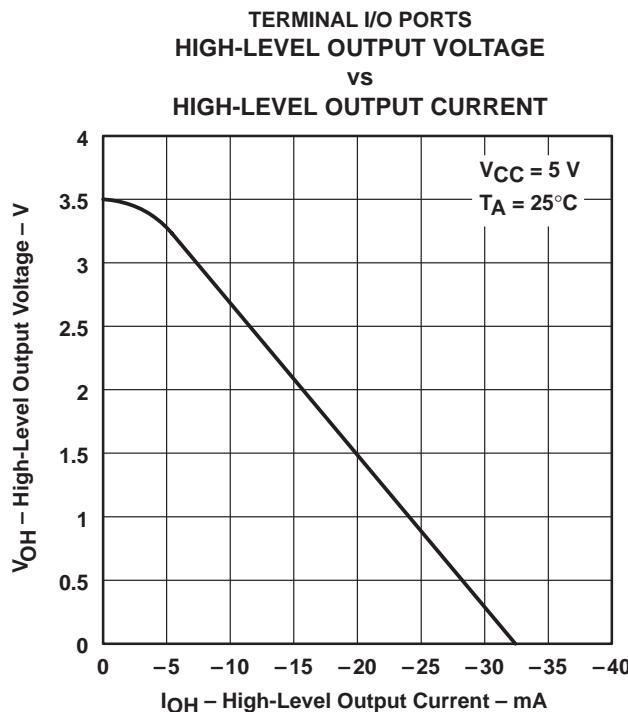


Figure 5

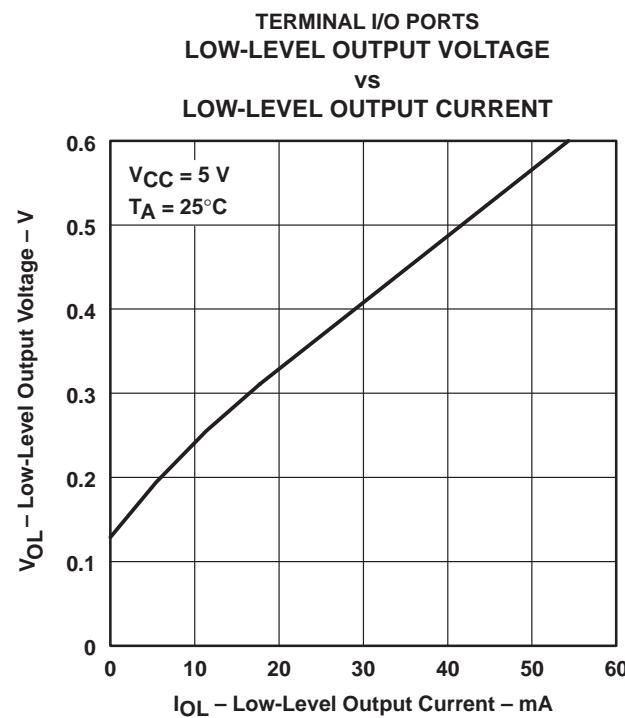


Figure 6

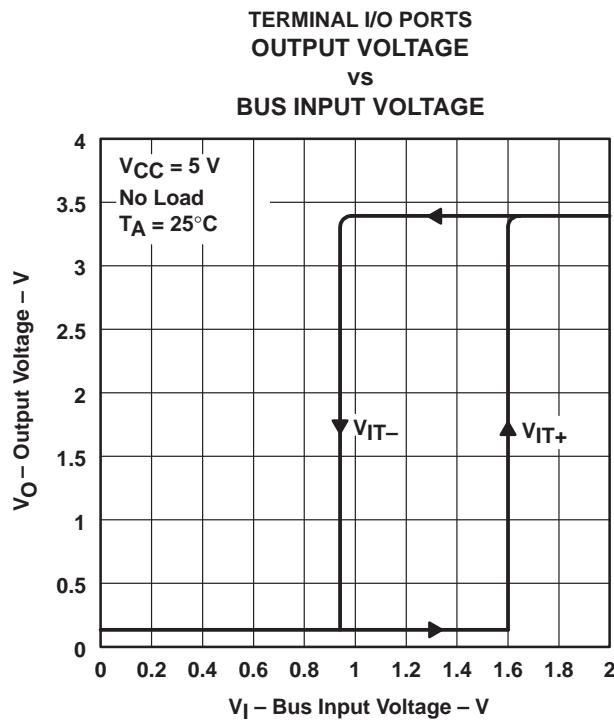


Figure 7

TYPICAL CHARACTERISTICS

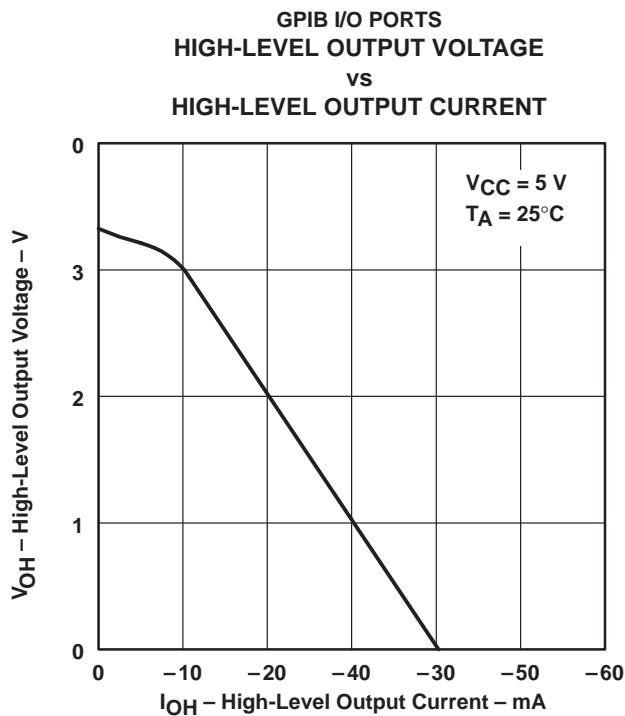


Figure 8

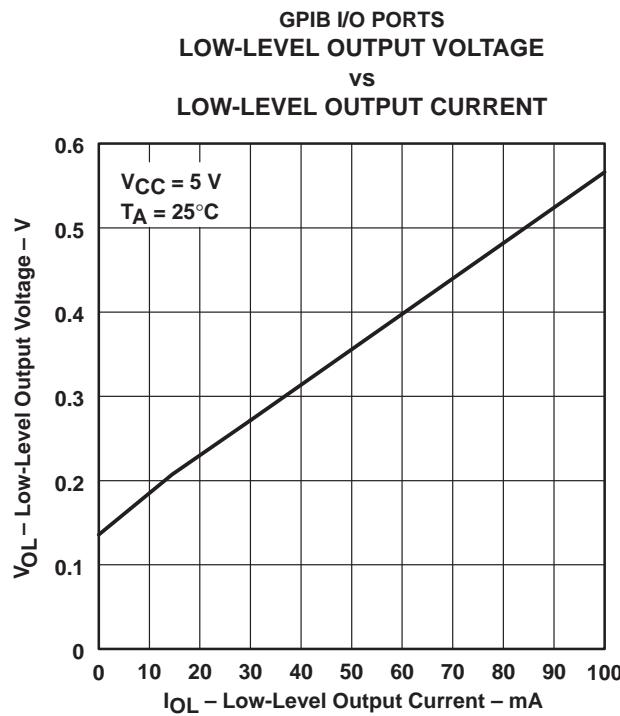


Figure 9

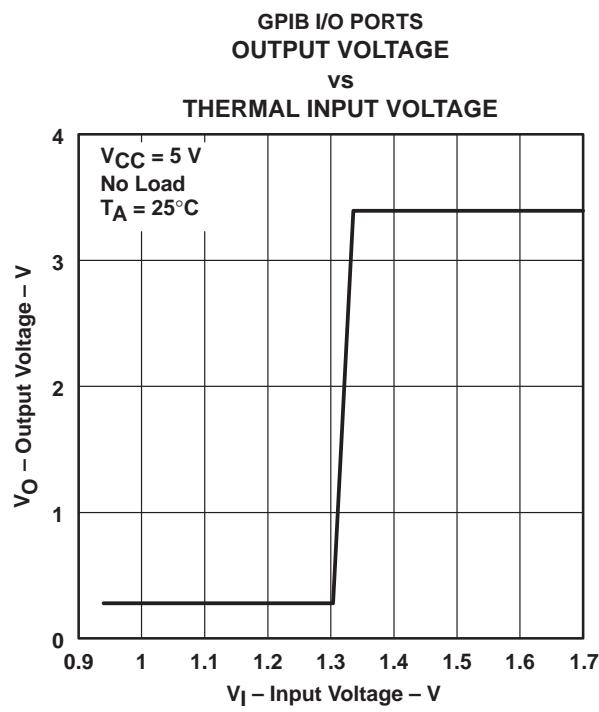


Figure 10

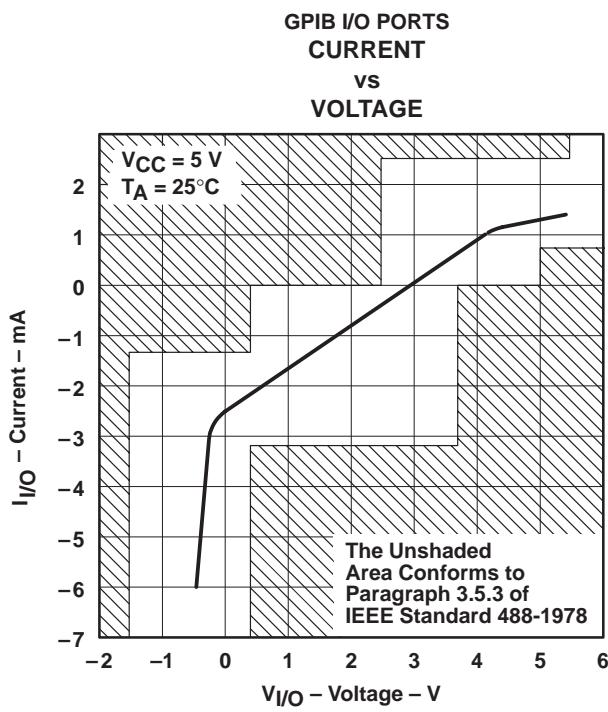


Figure 11

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75161BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75161BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75161BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75161BDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75161BDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75161BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75161BN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75161BNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75161BN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75162BDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75162BDWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75162BDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75162BDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN75162BN	OBsolete	PDIP	N	22		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

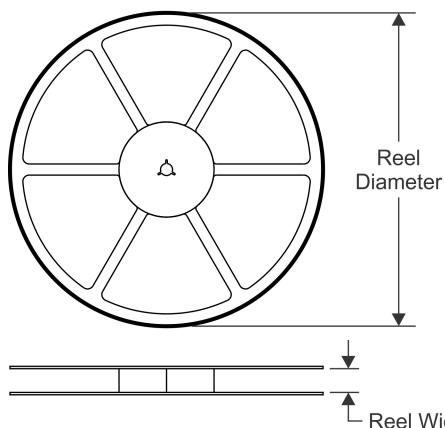
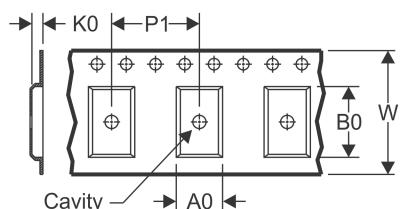
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

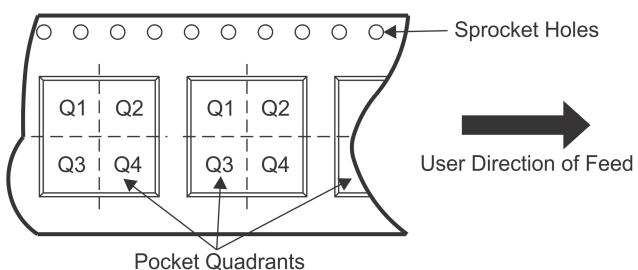
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75161BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75161BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75162BDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

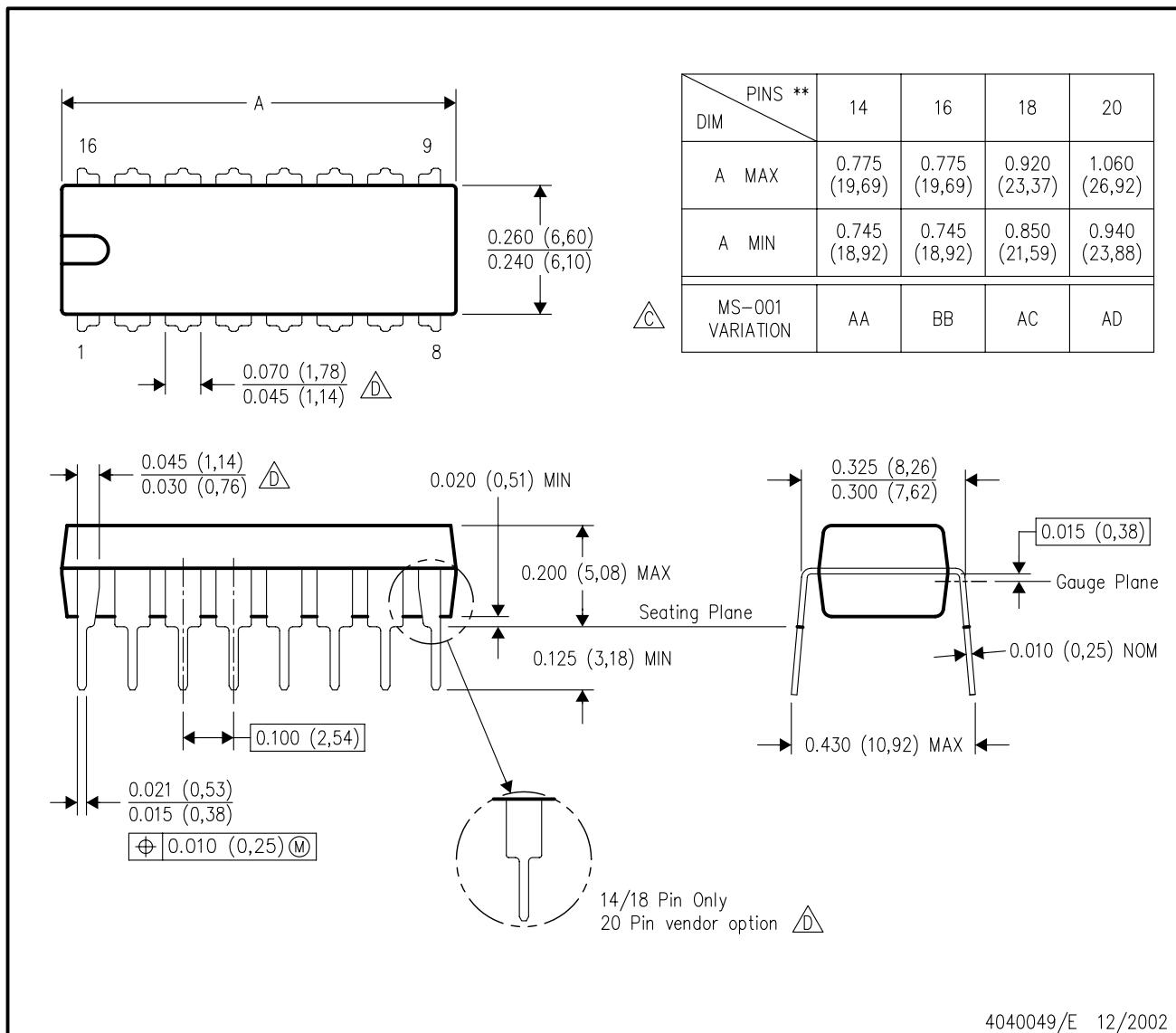

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75161BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75161BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75162BDWR	SOIC	DW	24	2000	367.0	367.0	45.0

## N (R-PDIP-T\*\*)

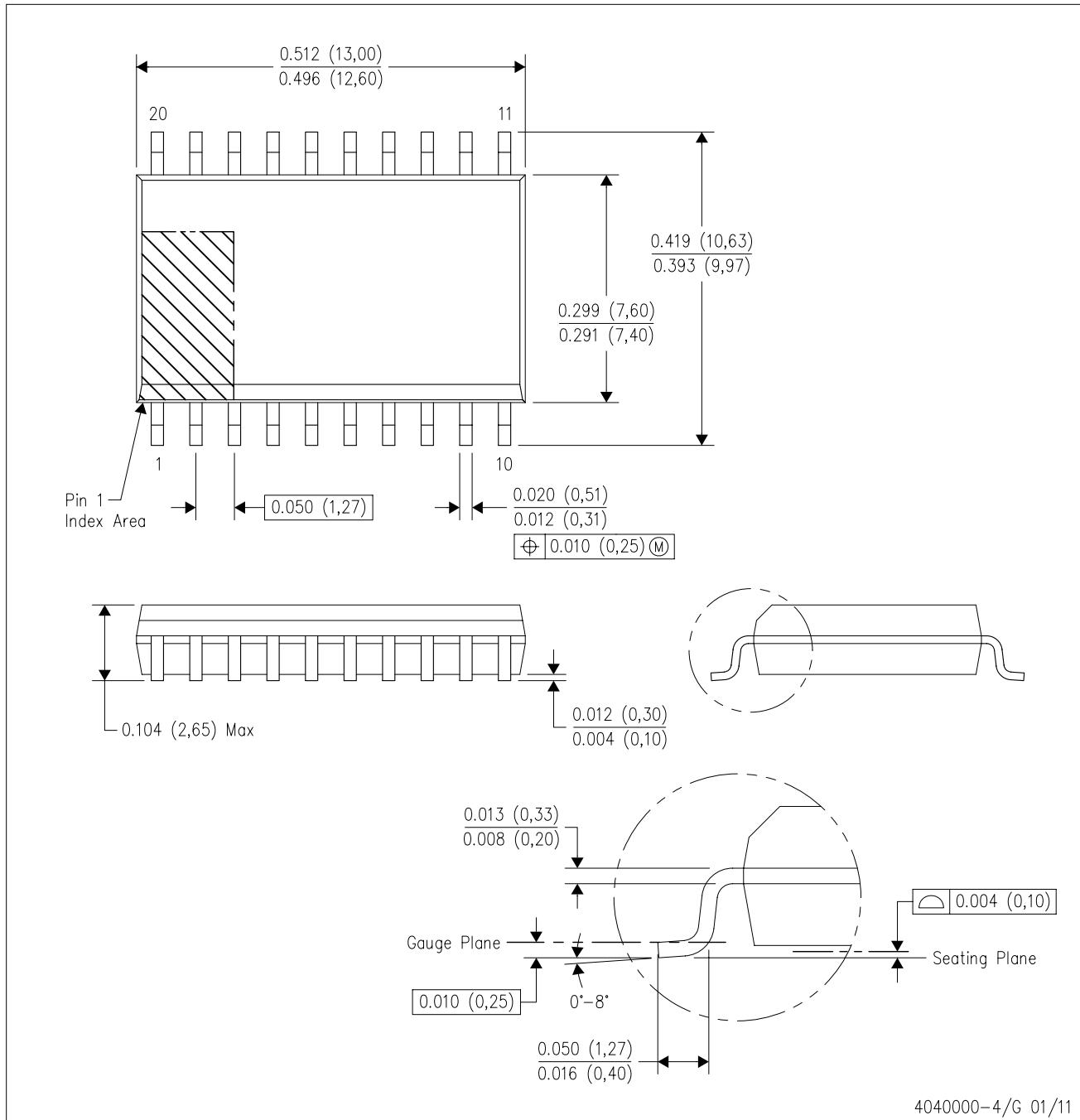
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

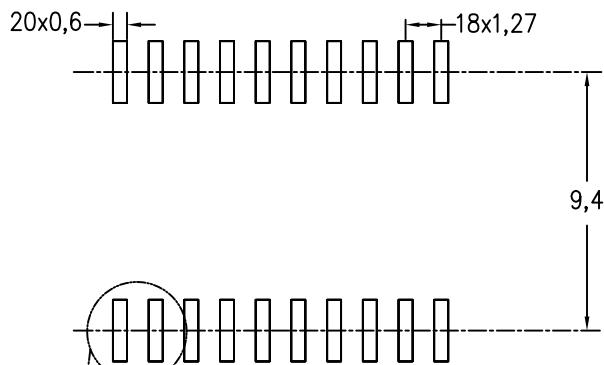
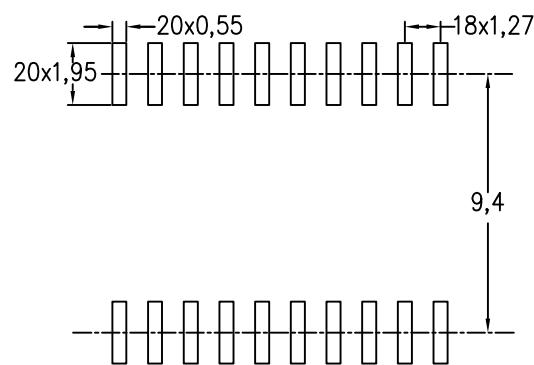


NOTES:

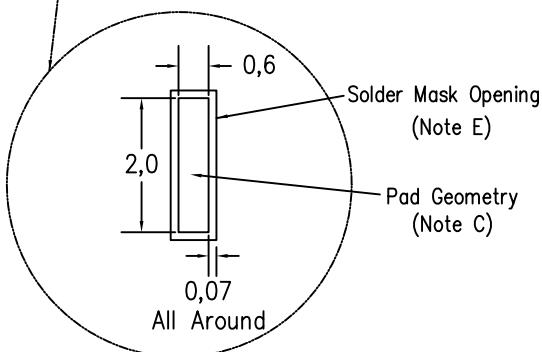
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



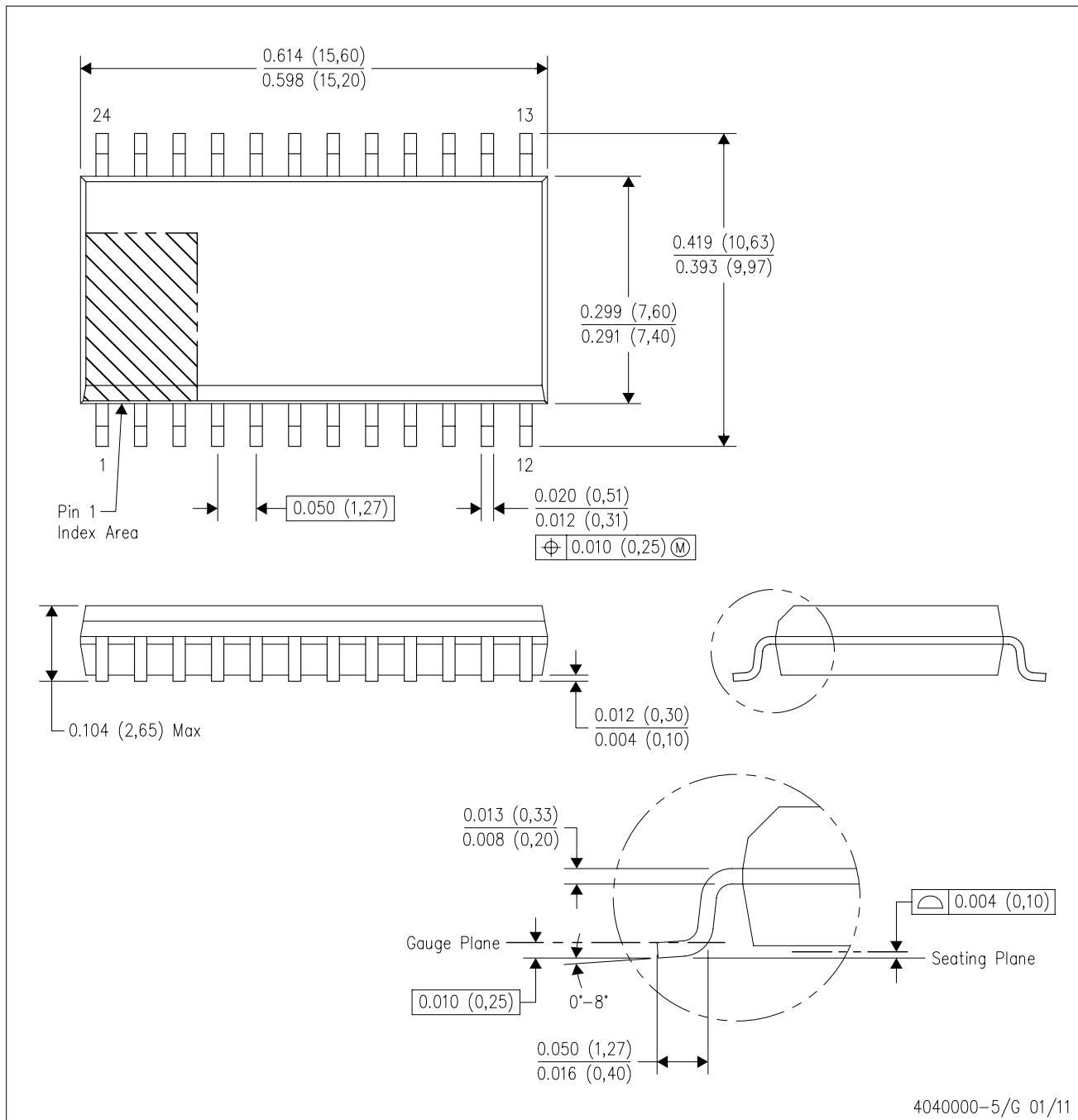
4209202-4/F 08/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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