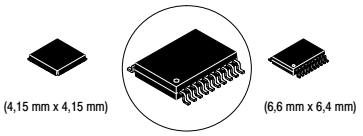


DUAL-OUTPUT, SINGLE-CELL BOOST CONVERTER

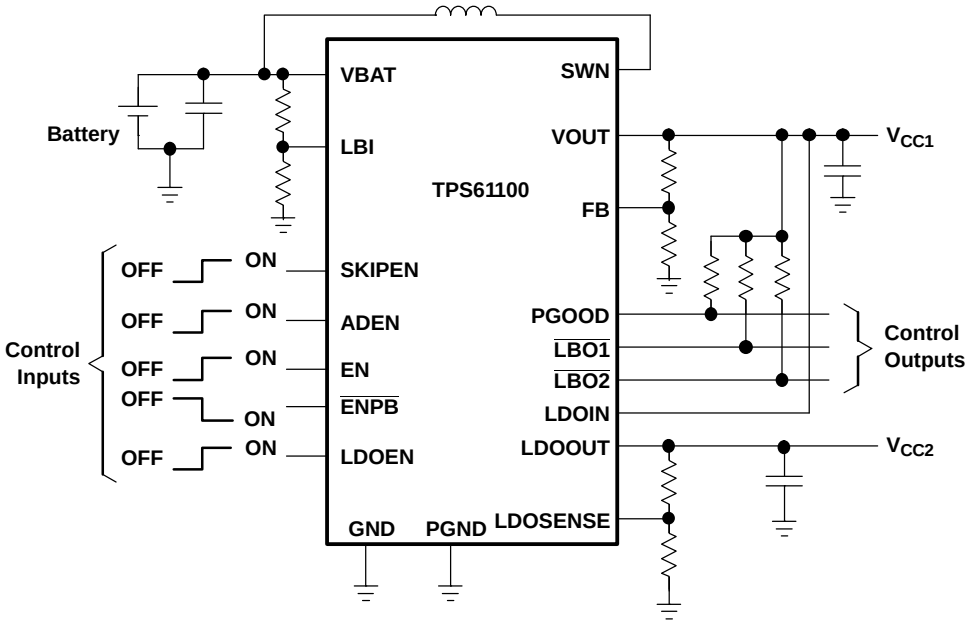
FEATURES

- Synchronous 95% Efficient Boost Converter
- Integrated 120 mA LDO for Second Output Voltage
- TSSOP-20 and QFN-24 Package
- 65 µA (Typ) Total Device Quiescent Current
- 0.8 V to 3.3 V Input Voltage Range
- Adjustable Output Voltage up to 5.5 V and Fixed Output Voltage Options
- Power-Save Mode for Improved Efficiency at Low Output Power
- Battery Supervision
- Power Good Output
- Pushbutton Function for Start-Up
- Low EMI-Converter (Integrated Antiringing Switch)
- Load Disconnect During Shutdown
- Auto Discharge Allows the Device to Discharge Output Capacitor During Shutdown
- Overtemperature Protection
- EVM Available (TPS6110XEVM-216)

APPLICATIONS

- All Single or Dual Cell Battery Operated Products Which Use Two System Voltages Like DSP C5X Applications
- Internet Audio Player, PDAs, Digital Still Cameras and Other Portable Equipment

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The TPS6110x devices provide a complete power supply solution for products powered by either one or two Alkaline, NiCd, or NiMH battery cells. The converter generates two stable output voltages that are either adjusted by an external resistor divider or fixed internally on the chip. It stays in operation with supply voltages down to 0.8 V. The implemented boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency.

The maximum peak current in the boost switch is limited to a value of 1800 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. An auto discharge function allows discharging the output capacitors during shutdown mode. This is especially useful in microcontroller applications where the microcontroller or microprocessor should not remain active due to the stored voltage on the output capacitors. Programming the ADEN-pin disables this feature. A low-EMI mode is implemented to reduce ringing and in effect lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode. A power good output at the boost stage provides additional control of cascaded power supply components.

The built-in LDO can be used for a second output voltage derived either from the boost output or directly from the battery. The output voltage of this LDO can be programmed by an external resistor divider or is fixed internally on the chip. The LDO can be enabled separately i.e., using the power good of the boost stage.

The device is packaged in a 20-pin TSSOP (20 PW) package or in a 24-pin QFN (24 RGE) package.

AVAILABLE PACKAGE OPTIONS

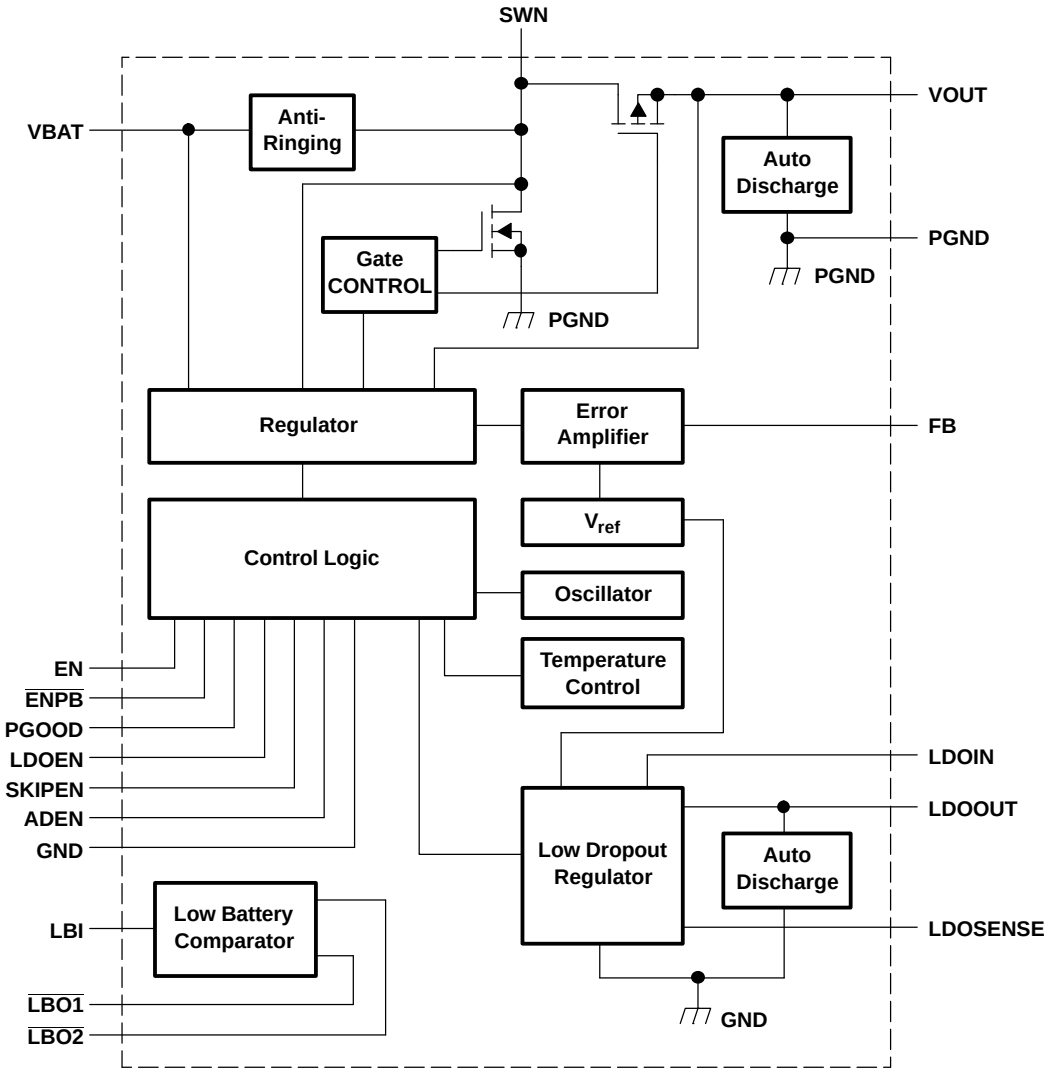
PACKAGE	CODE
20-Pin TSSOP	PW
24-Pin QFN	RGE

AVAILABLE OUTPUT VOLTAGE OPTIONS

T_A	OUTPUT VOLTAGE DC/DC	OUTPUT VOLTAGE LDO	PART NUMBER(1)	PART NUMBER(1)
40°C to 85°C	Adjustable	Adjustable	TPS61100PW	TPS61100RGE
	3.3 V	Adjustable	TPS61103PW	TPS61103RGE
	3.3 V	1.5 V	TPS61106PW	TPS61106RGE
	3.3 V	1.8 V	TPS61107PW	TPS61107RGE

(1) The PW package is available taped and reeled. Add R suffix to device type (e.g., TPS61100PWR) to order quantities of 2000 devices per reel. The RGE package is only available in reels. Add R suffix to device type (e.g. TPS61100RGER) to order quantities of 3000 devices per reel.

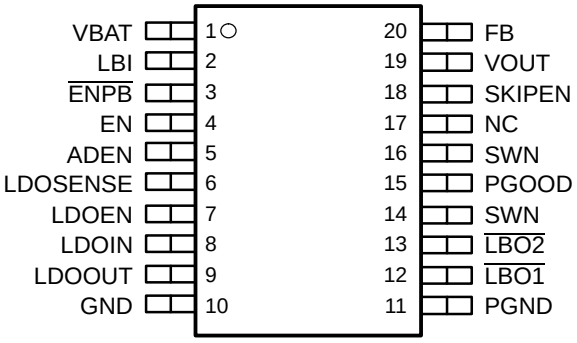
FUNCTIONAL BLOCK DIAGRAM



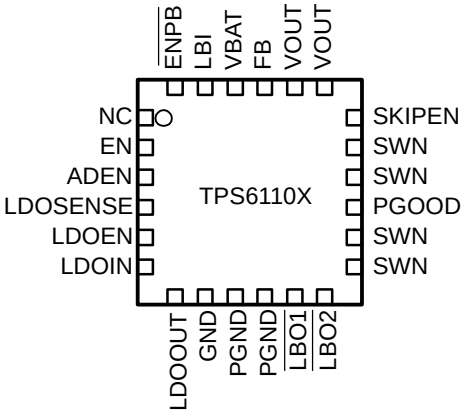
Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PW	RGE		
ADEN	5	3	I	Auto discharge enable (1/VBAT enabled, 0/GND disabled)
EN	4	2	I	Boost-enable input. (1/VBAT enabled, 0/GND disabled)
$\overline{\text{ENPB}}$	3	24	I	Boost-enable input (pushbutton). (0/GND enabled. 1/VBAT disabled)
FB	20	21	I	Boost-voltage feedback of adjustable versions
GND	10	8	I/O	Control/logic ground
LBI	2	23	I	Low battery comparator input (comparator enabled with EN)
$\overline{\text{LBO1}}$	12	11	O	Low battery comparator output 1 (open drain)
$\overline{\text{LBO2}}$	13	12	O	Low battery comparator output 2 (open drain)
LDOEN	7	5	I	LDO-enable input (1/VBAT enabled, 0/GND disabled)
LDOOUT	9	7	O	LDO output
LDOIN	8	6	I	LDO input
LDOSENSE	6	4	I	LDO feedback for voltage adjustment, must be connected to LDOOUT at fixed output voltage versions
NC	17	1		No connection
PGND	11	9, 10	I/O	Power ground
PGOOD	15	15	O	Boost output power good (1 : good, 0 : failure) (open drain)
SKIPEN	18	18	I	Enable/disable Power save mode (1: VBAT enabled, 0: GND disabled)
SWN	14, 16	13, 14, 16, 17	I	Boost switch input
VBAT	1	22	I	Supply pin
VOUT	19	19, 20	O	Boost output

PW PACKAGE
(TOP VIEW)



RGE PACKAGE
(TOP VIEW)



NC – No internal connection

DETAILED DESCRIPTION

SYNCHRONOUS RECTIFIER

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 95%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

CONTROLLER CIRCUIT

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The nominal peak current limit is set to 1500 mA.

An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

DEVICE ENABLE

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. It also can be enabled with a low signal on $\overline{\text{ENPB}}$. This forces the converter to start up as long as the low signal is applied. During this time EN must be set high to prevent the converter from going down into shutdown mode again. If EN is high, a negative signal on $\overline{\text{ENPB}}$ is ignored.

In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the synchronous rectifier section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 0.7 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 0.7 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

LDO ENABLE

When the voltage is applied at VBAT, the LDO can be separately enabled and disabled by using the LDOEN pin in the same way as the EN pin at the dc/dc converter stage described above.

POWER GOOD

The PGOOD pin stays high impedance when the dc/dc converter delivers an output voltage within a defined voltage window. So it can be used to enable the converter after pushbutton start-up, or to enable any connected circuitry such as cascaded converters (LDO) or processor circuits.

DETAILED DESCRIPTION (continued)

POWER SAVE MODE

The SKIPEN pin can be used to select different operation modes. To enable power save, SKIPEN must be set high. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the SKIPEN to GND.

AUTO DISCHARGE

The auto discharge function is needed in applications where the supply voltage of a microcontroller, microprocessor or memory has to be removed during shutdown in order to make sure that the system quickly goes in a defined state. The auto discharge function is enabled when the ADEN is set high. It is disabled when the ADEN is set to GND. When the auto discharge function is enabled, the output capacitor is discharged after the device is programmed in the shutdown mode. The output capacitor is discharged by an integrated switch of 400 Ω, hence the discharge time depends on the size of the output capacitor.

LOW BATTERY DETECTOR CIRCUIT—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, both LBO-pin are high-impedance. There are three programmed thresholds, 400 mV, 450 mV, and 500 mV. The outputs on $\overline{\text{LBO1}}$ and $\overline{\text{LBO2}}$ are shown as follows:

LBI INPUT (mV)	$\overline{\text{LBO1}}$	$\overline{\text{LBO2}}$
0-400	0	0
400-450	1	0
450-500	0	1
500-VBAT	1	1

1 means that the output stays at high-impedance and 0 means that the output goes active low. If there is only one LBO output needed, both outputs can be tied together. Then the switching threshold is at 500 mV at LBI.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI-pin. The resistive divider scales down the battery voltage to a voltage level of 400 mV (450 mV, 500 mV), which is then compared to the LBI threshold voltage. The LBI-pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI-threshold. If the low-battery detection circuit is not used, the LBI-pin should be connected to GND (or to VBAT) and the LBO-pin can be left unconnected. Do not let the LBI-pin float.

LOW-EMI SWITCH

The device integrates a circuit that removes the ringing that typically appears on the SW-node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW-pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

LDO

The built-in LDO can be used to generate a second output voltage derived from the dc/dc converter output, from the battery, or from another power source like an ac adapter or a USB power rail. The LDOSENSE input must be connected to LDOOUT at fixed output voltage versions.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	UNIT
Input voltage range on VBAT, LBI, SKIPEN, EN, $\overline{\text{ENPB}}$, ADEN, FB, LDOEN	-0.3 V to 3.6 V
Input voltage range on SWN, VOUT, LDOIN, LDOOUT, LDOSENSE, PGOOD, $\overline{\text{LBO1}}$, $\overline{\text{LBO2}}$	-0.3 V to 7 V
Operating free air temperature range, T_A	-40°C to 85°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s	260°C

(1) Stresses beyond those listed under„ absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under„ recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Supply voltage at VBAT	0.8		3.3	V
L	Boost—inductor	4.7	10		µH
C_i	Boost—input capacitor		10		µF
C_o	Boost—output capacitor	22	100		µF
C_i	LDO—input capacitor		1		µF
C_o	LDO—output capacitor	1	2.2		µF
T_J	Operating virtual junction temperature	-40		125	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

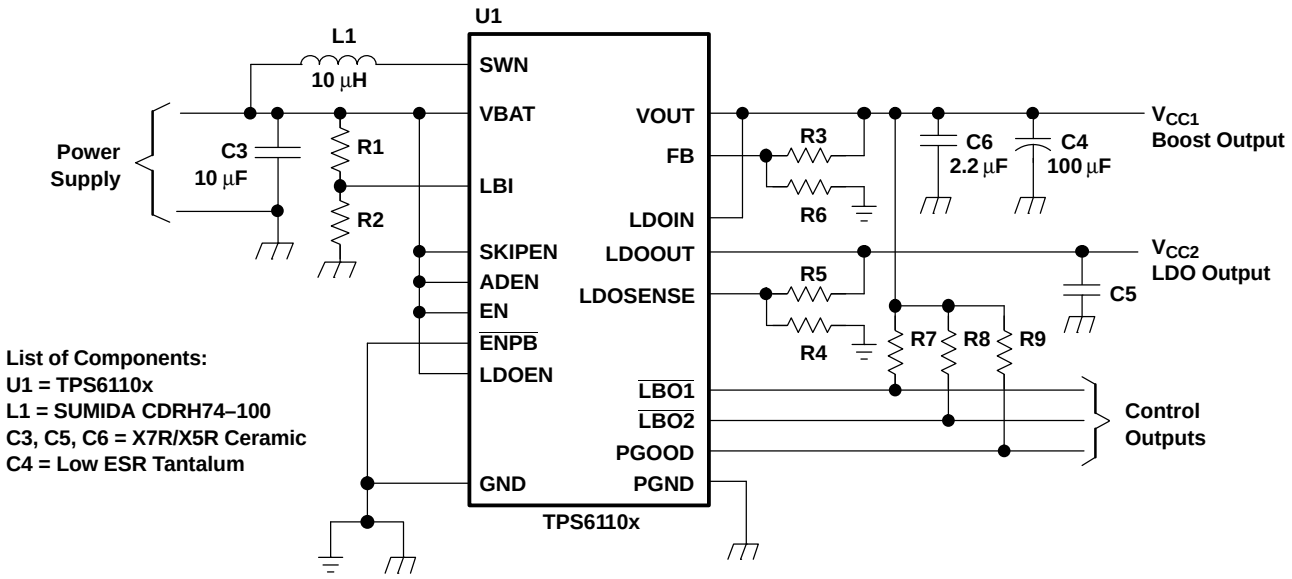
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST STAGE							
$V_{I(b)}$	Input voltage for start-up		R_L > = 66 Ω at V_o = 3.3 V		0.85	1.1	V
	Input voltage once started			0.8		3.3	V
$V_{o(b)}$	Output voltage			1.5		5.5	V
	Minimum possible output power		PW package, VBAT ≥ 1.5 V		600		mW
V_{ref}	Reference voltage			485	500	515	mV
f	Oscillator frequency			320	500	800	kHz
	Switch current limit		V_o = 3.3 V	1200	1500	1800	mA
	Startup current limit				610		mA
	Boost switch on resistance		V_o = 3.3 V		180	300	mΩ
	Sync switch on resistance		V_o = 3.3 V		180	300	mΩ
	Total accuracy			-3%		3%	
	Auto discharge switch resistance				400		Ω
	Boost quiescent current	VBAT	I_O = 0 mA, V_{EN} = VBAT = 3.3 V, V_o = 3.3 V, ENLDO = 0		25	40	µA
		VOUT	I_O = 0 mA, V_{EN} = VBAT = 3.3 V, V_o = 3.3 V, ENLDO = 0		12	20	µA
	Boost shutdown current		V_{EN} = 0 V		0.5	5	µA
LDO STAGE							
$V_{I(LDO)}$	Input voltage range			1.5		7	V
$V_{o(LDO)}$	Output voltage			0.9		3.6	V
$I_{o(LDO)}$	Output current		V_I ≥ 1.8 V	120	270		mA
			V_I < 1.8 V	80			
	LDO short circuit current limit					500	mA
	Minimum voltage drop		V_I ≥ 1.8 V, $I_{o(LDO)}$ = 120 mA			300	mV
	Total accuracy		I_o ≥ 1 mA			±3%	
	Line regulation		LDOIN change form 1.8 V to 2.6 V at 100 mA			0.6%	
	Load regulation		Load change from 10% to 90%			0.6%	
	Auto discharge switch resistance				400		Ω
	LDO quiescent current	LDOIN	LDOIN = 7 V, VBAT = 1.2 V, EN = 0		27	40	µA
		VBAT			27	40	
	LDO shutdown current				0.01	1	µA

ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL STAGE						
V_{IL}	LBI1 voltage threshold	V_{LBI} voltage decreasing	390	400	410	mV
	LBI2 voltage threshold	V_{LBI} voltage decreasing	440	450	460	mV
	LBI3 voltage threshold	V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis			10		mV
	LBI input current	EN = Vbat or GND		0.01	0.1	µA
	$\overline{LBO1}$ output low voltage	V_o = 3.3 V, I_{OL} = 10 µA		0.04	0.4	V
	$\overline{LBO1}$ output low current			10		µA
	$\overline{LBO1}$ output leakage current	V_{LBO} = 3.3 V		0.01	0.1	µA
	$\overline{LBO2}$ output low voltage	V_o = 3.3 V, I_{OL} = 10 µA		0.04	0.4	V
	$\overline{LBO2}$ output low current			10		µA
	$\overline{LBO2}$ output leakage current	V_{LBO} = 3.3 V		0.01	0.1	µA
V_{IL}	EN, $\overline{ENPB}$, LDOEN, SKIPEN and ADEN input low voltage				0.2 × VBAT	
V_{IH}	EN, $\overline{ENPB}$, LDOEN, SKIPEN and ADEN input high voltage		0.8 × VBAT			
	EN, $\overline{ENPB}$, LDOEN, SKIPEN and ADEN input current	Clamped on GND or VBAT		0.01	0.1	µA
	Powergood threshold	V_o = 3.3 V	0.9xV_o	0.92xV_o	0.95xV_o	
	Powergood delay			30		µs
	Powergood output low voltage	V_o = 3.3 V, I_{OL} = 10 µA		0.04	0.4	V
	Powergood output low current			10		µA
	Powergood output leakage current			0.01	0.1	µA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

Table of Graphs

BOOST CONVERTER		Figure
Maximum output current	vs Input voltage for VOUT = 3.3 V, 5.0 V	1
	vs Input voltage for VOUT = 1.8 V, 2.5 V	2
Efficiency	vs Output current for VIN = 1.2 V, VOUT = 1.5 V	3
	vs Output current for VIN = 1.2 V, VOUT = 2.5 V	4
	vs Output current for VIN = 1.2 V, VOUT = 3.3 V	5
	vs Output current for VIN = 1.8 V, VOUT = 2.5 V	6
	vs Output current for VIN = 2.4 V, VOUT = 3.3 V	7
	vs Output current for VIN = 2.4 V, VOUT = 5.0 V	8
	vs Input voltage for Iout = 10 mA/100 mA/200 mA, VOUT = 3.3 V	9
Output voltage	vs Output current TPS61103/6	10
Minimum start-up supply voltage	vs Load resistance	11
No-load supply current into VBAT	vs Input voltage	12
No-load supply current into VOUT	vs Input voltage	13
Waveforms	Output voltage (ripple) in continuous modeInductor current	14
	Output voltage (ripple) in power save modeInductor current	15
	Load transient response for output current step of 40 mA to 120 mA	16
	Line transient response for supply voltage step from 1 V to 1.5 V at Iout = 100 mA	17
	Boost converter start-up after enable	18
LDO		
Maximum output current	vs Input voltage for VOUT = 2.5 V, 3.3 V	19
	vs Input voltage for VOUT = 1.5 V, 1.8 V	20
Output voltage	vs Output current TPS61106	21
Dropout voltage	vs Output current TPS61100 at 3.3 V TPS61106	22
No-load supply current into LDOIN	vs Input voltage	23
PSRR	vs Frequency	24
Waveforms	Load transient response for output current step of 20 mA to 100 mA	25
	Line transient response for supply voltage step from 1.8 V to 2.4 V at Iout = 100 mA	26
	LDO start-up after enable	27

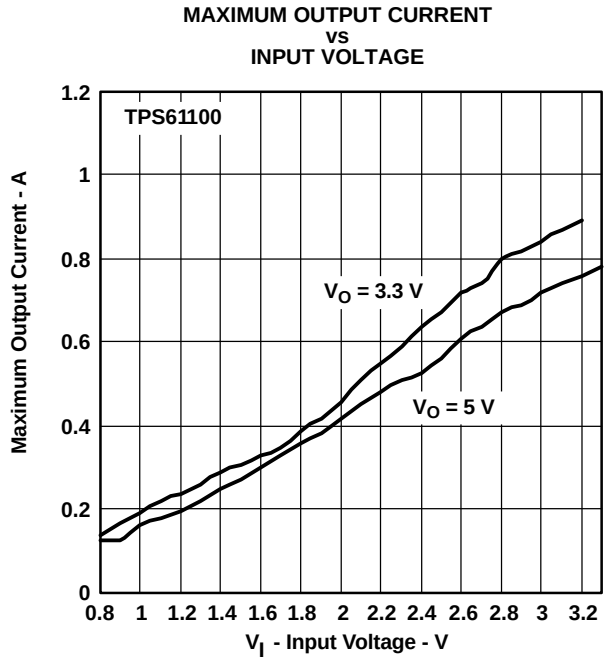


Figure 1.

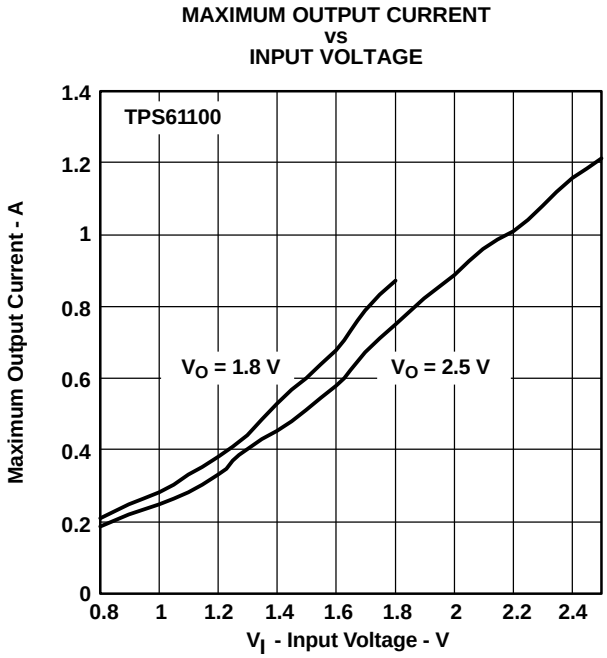


Figure 2.

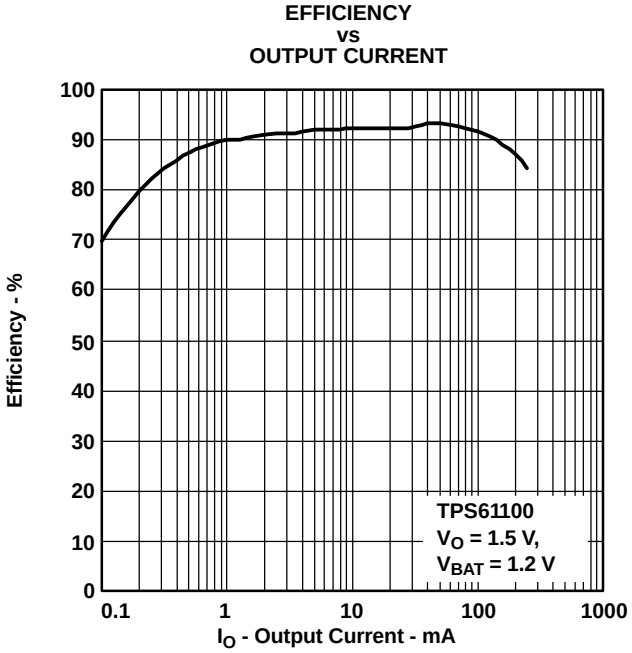


Figure 3.

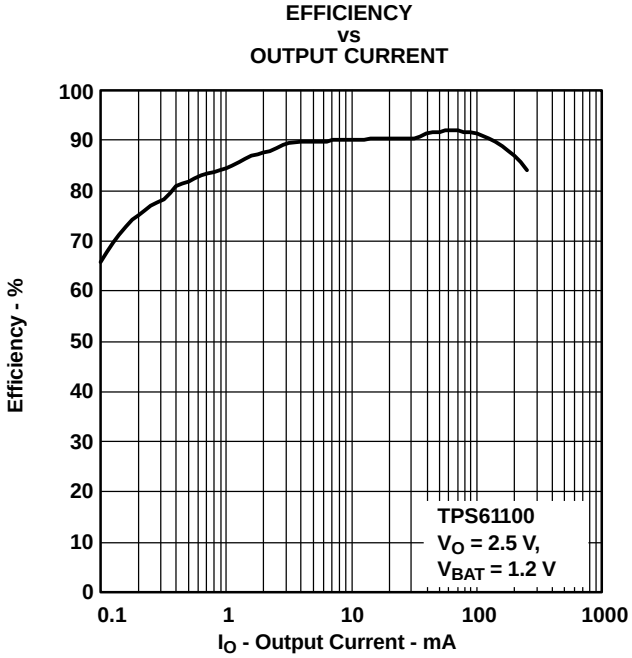


Figure 4.

TYPICAL CHARACTERISTICS (continued)

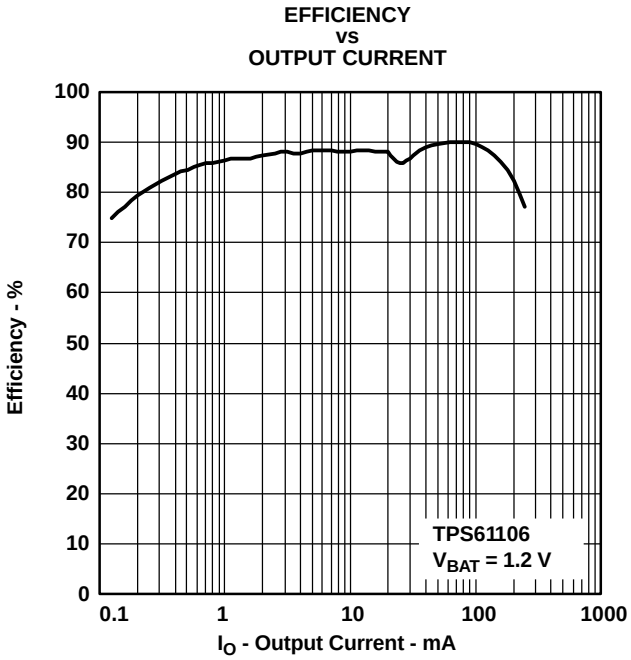


Figure 5.

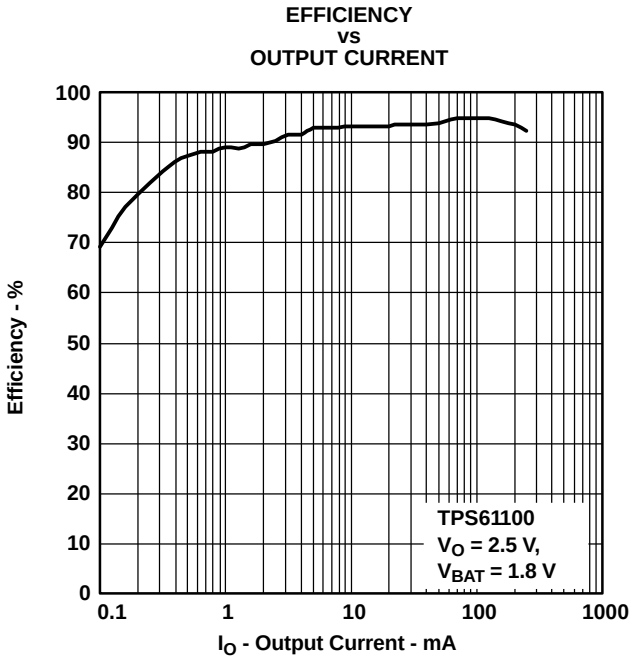


Figure 6.

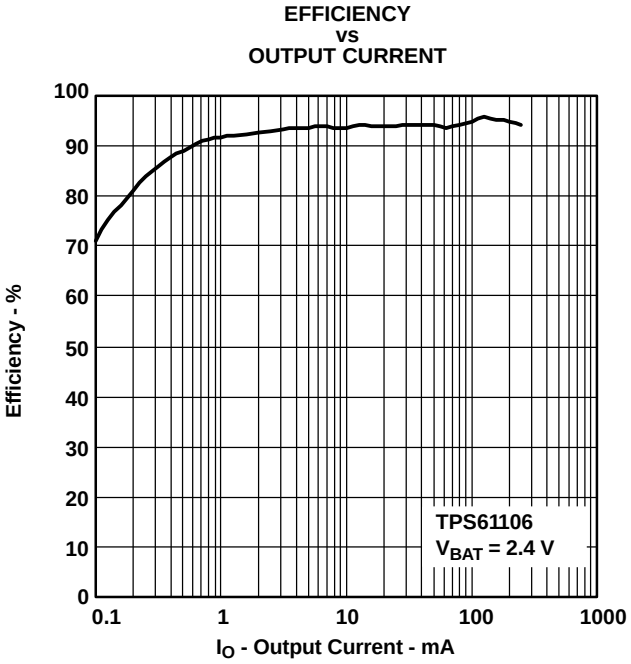


Figure 7.

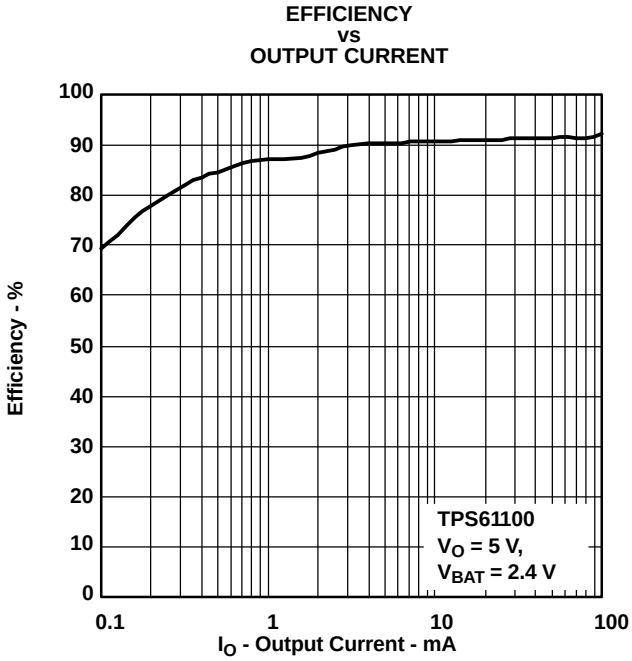


Figure 8.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
vs
INPUT VOLTAGE

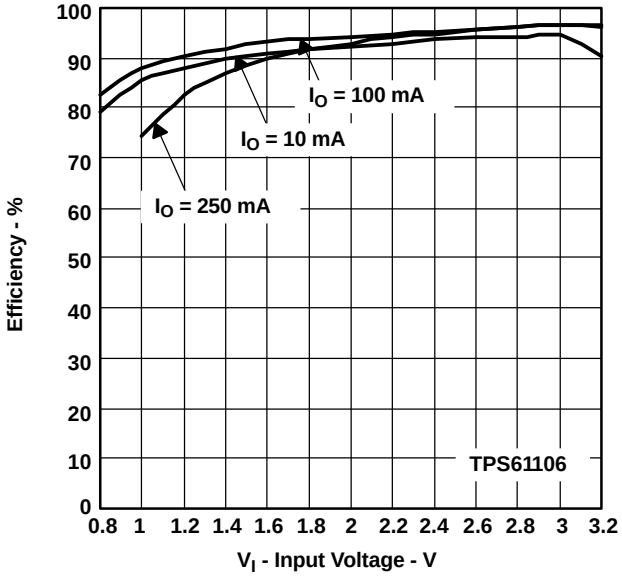


Figure 9.

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

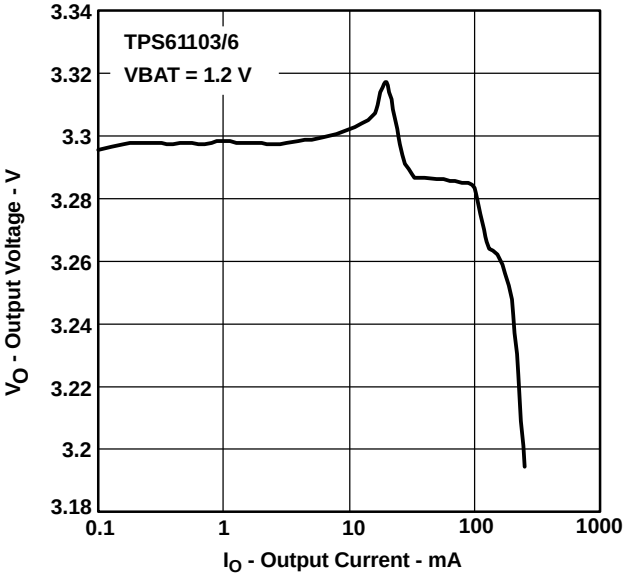


Figure 10.

MINIMUM START-UP SUPPLY VOLTAGE
vs
LOAD RESISTANCE

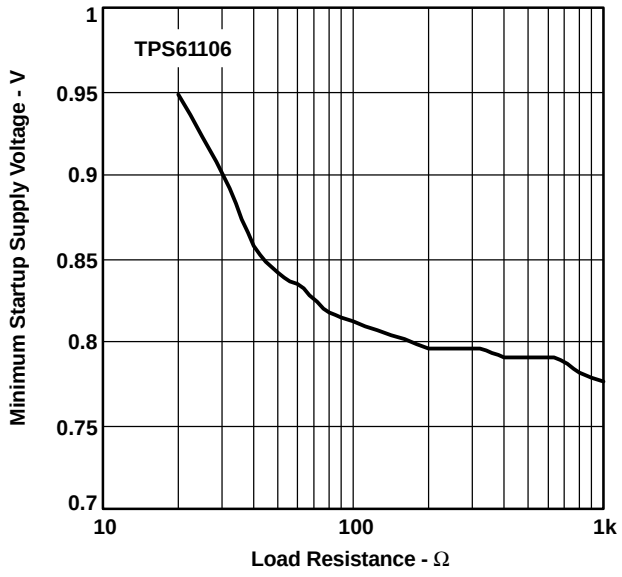


Figure 11.

NO-LOAD SUPPLY CURRENT INTO VBAT
vs
INPUT VOLTAGE

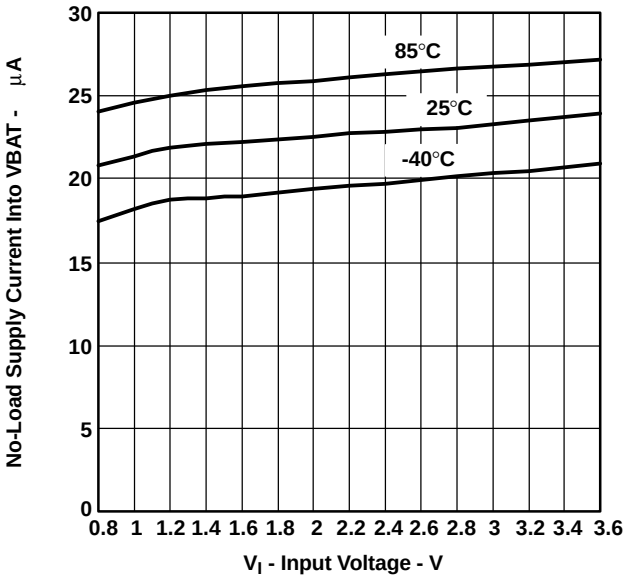


Figure 12.

TYPICAL CHARACTERISTICS (continued)

NO-LOAD SUPPLY CURRENT INTO VOUT
vs
INPUT VOLTAGE

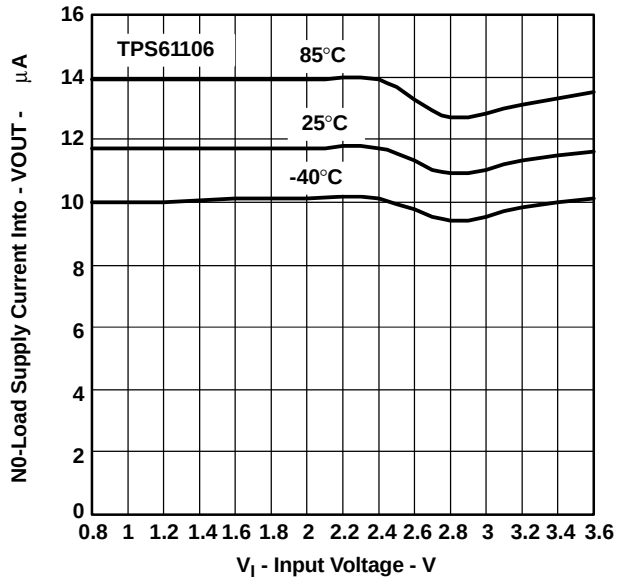


Figure 13.

OUTPUT VOLTAGE IN CONTINUOUS MODE

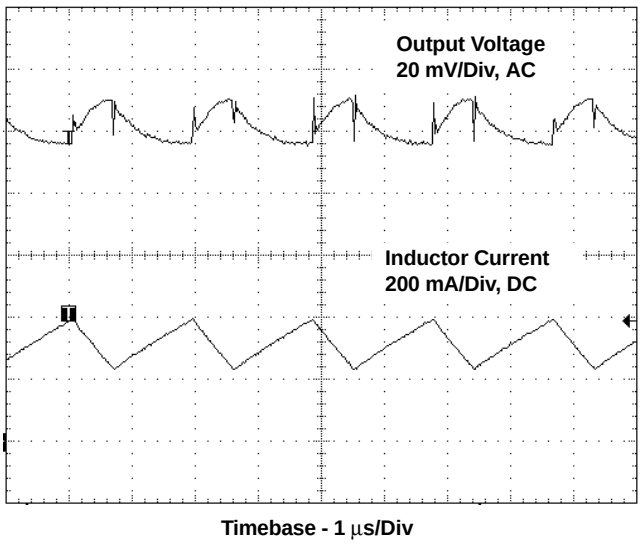


Figure 14.

OUTPUT VOLTAGE IN POWER SAVE MODE

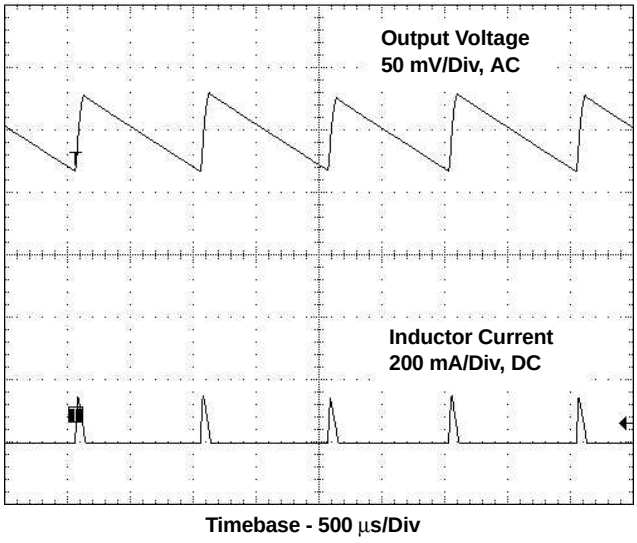


Figure 15.

LOAD TRANSIENT RESPONSE

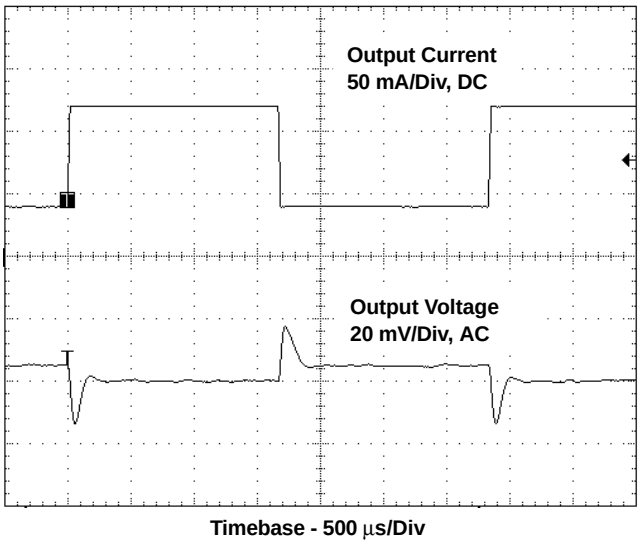


Figure 16.

TYPICAL CHARACTERISTICS (continued)

LINE TRANSIENT RESPONSE

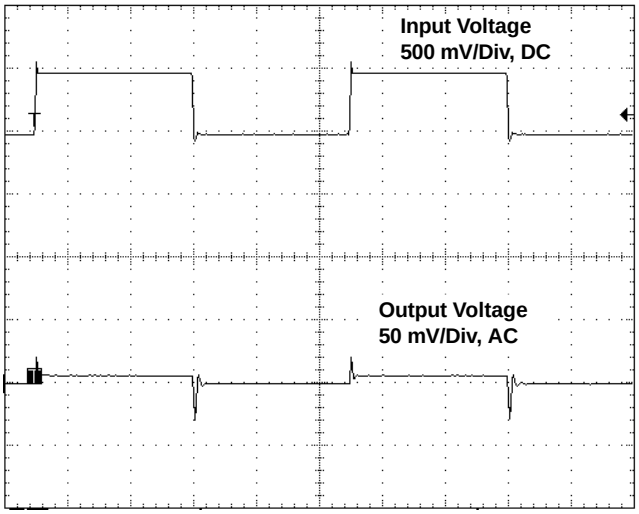


Figure 17.

BOOST-CONVERTER START-UP AFTER ENABLE

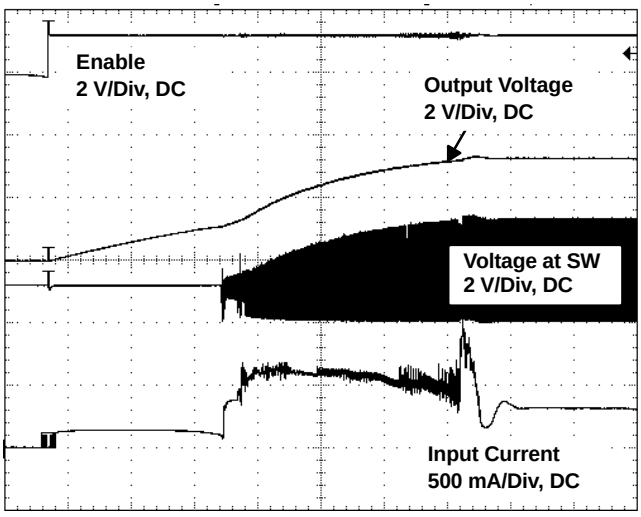


Figure 18.

MAXIMUM LDO OUTPUT CURRENT
vs
LDO INPUT VOLTAGE

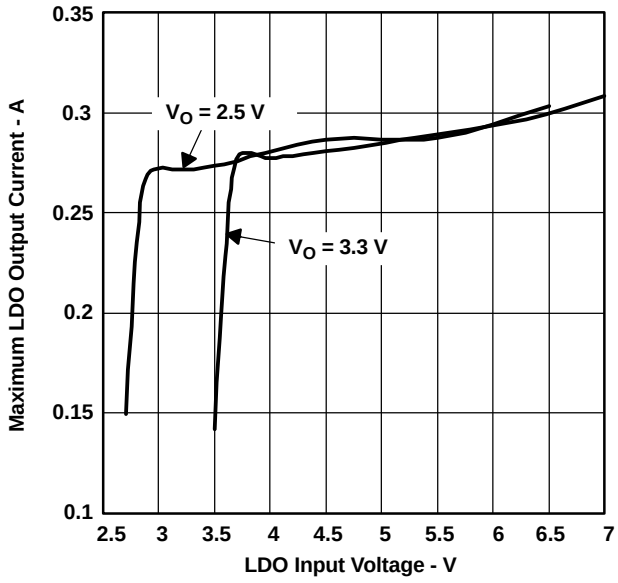


Figure 19.

MAXIMUM LDO OUTPUT CURRENT
vs
LDO INPUT VOLTAGE

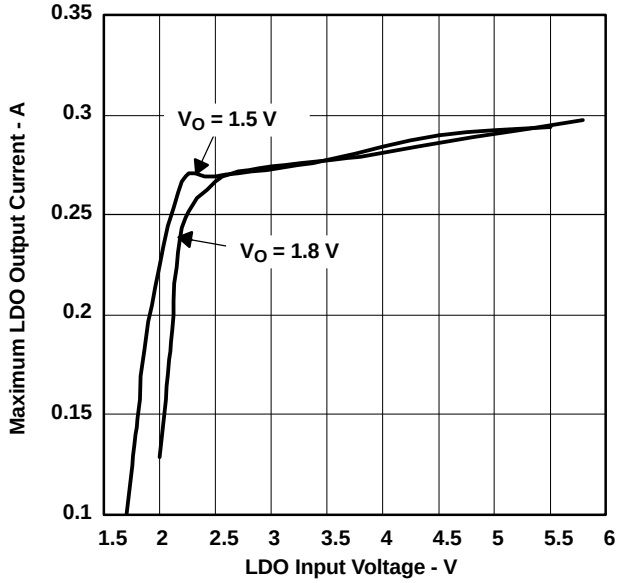


Figure 20.

TYPICAL CHARACTERISTICS (continued)

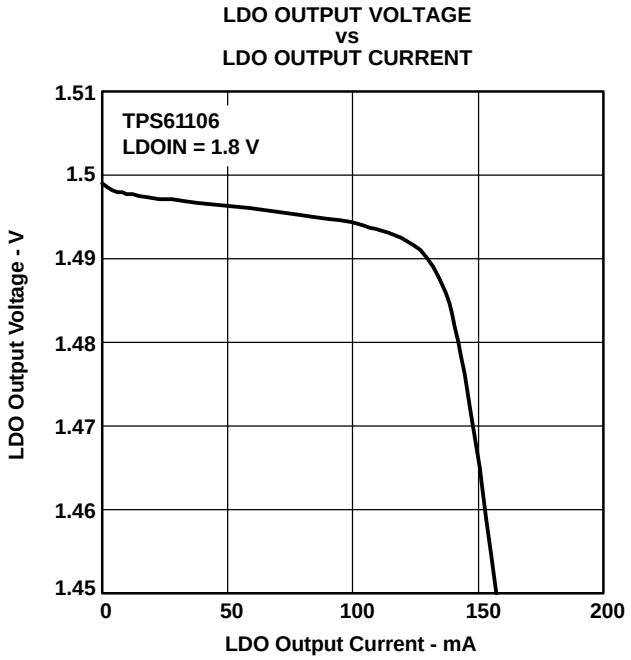


Figure 21.

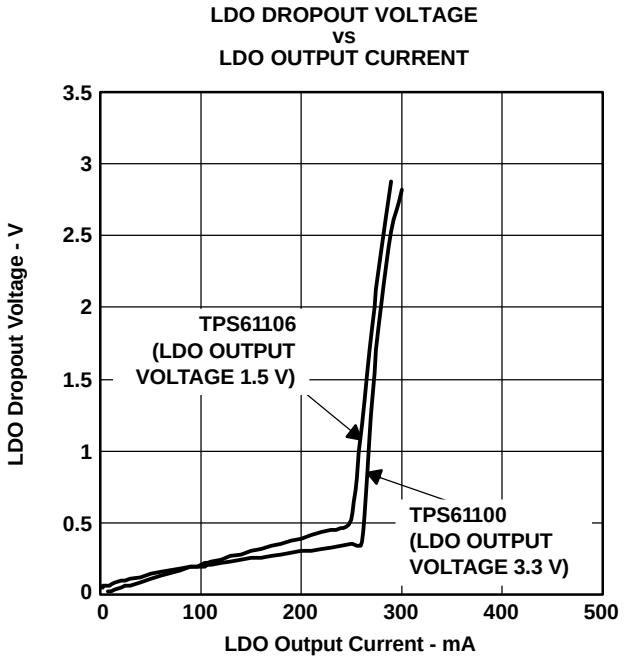


Figure 22.

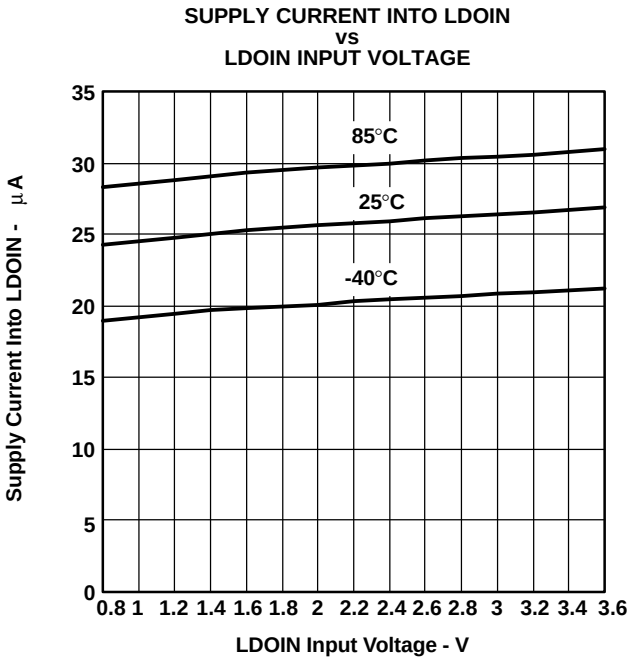


Figure 23.

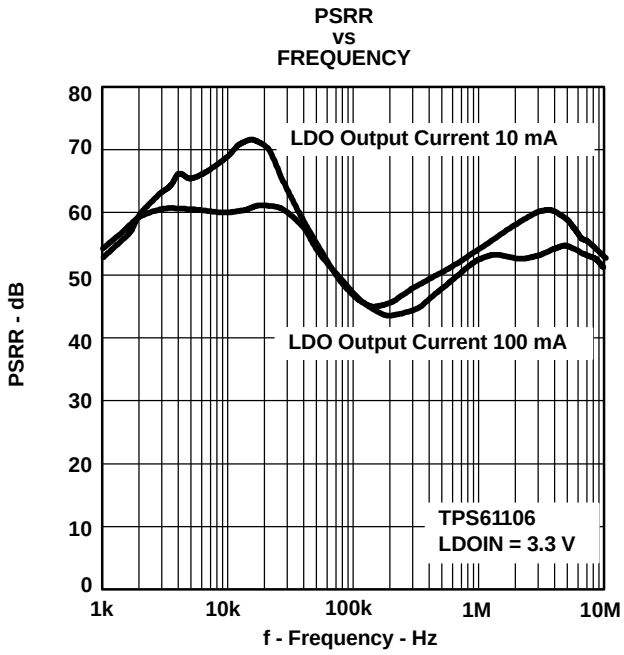
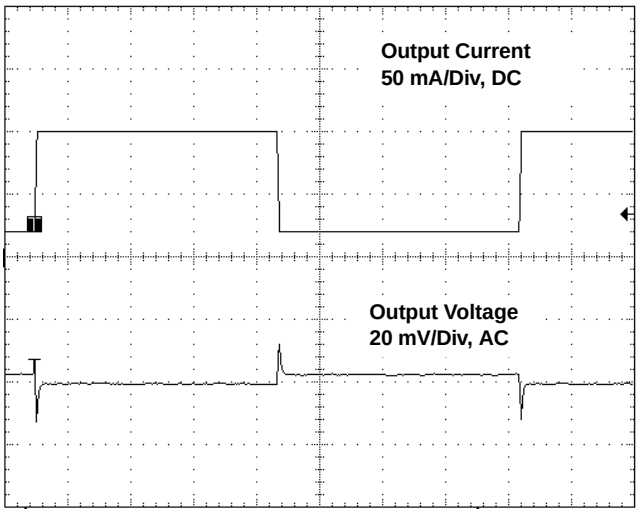


Figure 24.

TYPICAL CHARACTERISTICS (continued)

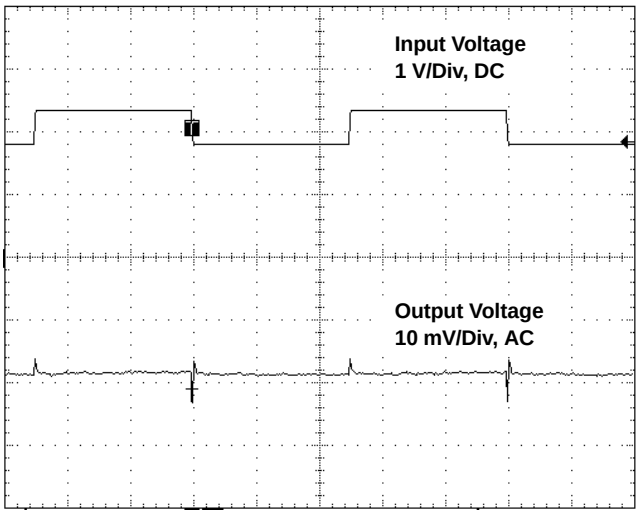
LDO LOAD TRANSIENT RESPONSE



Timebase - 1 ms/Div

Figure 25.

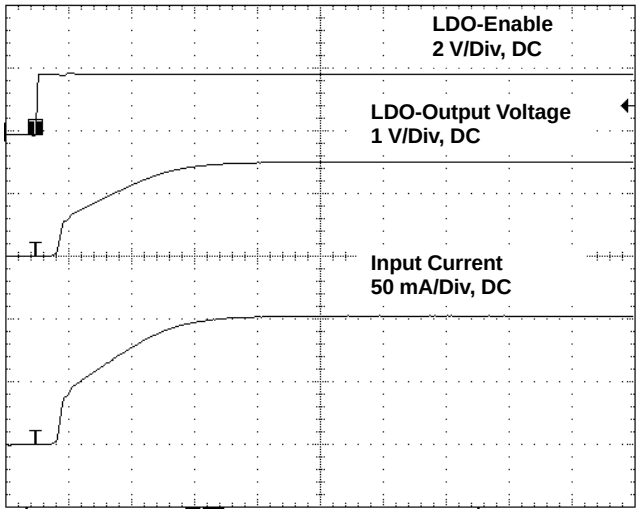
LDO LINE TRANSIENT RESPONSE



Timebase - 2 ms/Div

Figure 26.

LDO START-UP AFTER ENABLE



Timebase - 50 µs/Div

Figure 27.

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS6110x boost converters are intended for systems powered by a single-cell NiCd or NiMH battery with a typical terminal voltage between 0.9 V and 1.6 V. They can also be used in systems powered by two-cell NiCd or NiMH batteries with a typical stack voltage between 1.8 V and 3.2 V. Additionally, single- or dual-cell, primary and secondary alkaline battery cells can be the power source in systems where the TPS6110x is used.

Programming the Output Voltage

Boost Converter

The output voltage of the TPS61100 boost converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R6 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using Equation 1:

$$R3 = R6 \times \left(\frac{V_O}{V_{FB}} - 1\right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1\right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1-MΩ resistor should be chosen for R3.

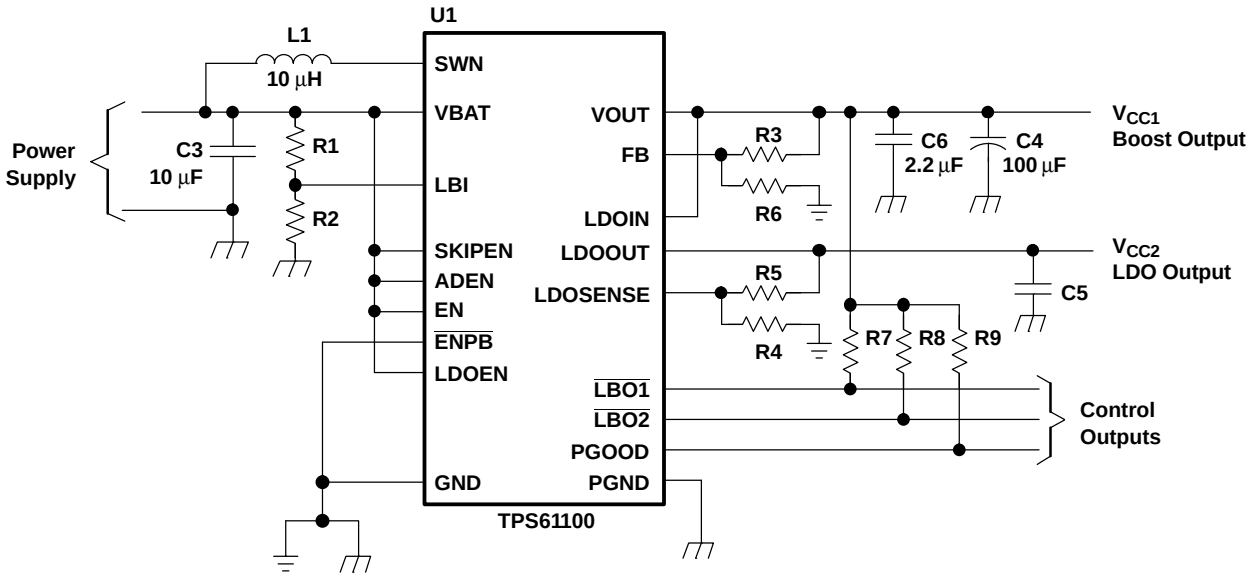


Figure 28. Typical Application Circuit for Adjustable Output Voltage Option

LDO

Programming the output voltage at the LDO follows almost the same rules as at the boost converter section. The maximum programmable output voltage at the LDO is 3.3 V. Since reference and internal feedback circuitry are similar, as they are at the boost converter section, R4 also should be in the 200-kΩ range. The calculation of the value of R5 can be done using the following Equation 2:

$$R5 = R4 \times \left(\frac{V_O}{V_{FB}} - 1\right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1\right) \quad (2)$$

If as an example, an output voltage of 1.5 V is needed, a 360 kΩ-resistor should be chosen for R5.

APPLICATION INFORMATION (continued)

Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 µA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 400 mV, 450 mV or 500 mV. The recommended value for R2is therefore in the range of 500 kΩ. From that, the value of resistor R_1, depending on the desired minimum battery voltage $V_{BAT,}$ can be calculated using Equation 3.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI\text{-}threshold}} - 1 \right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{450\ mV} - 1 \right) \quad (3)$$

For example, if the low-battery detection circuit should flag an error condition for the 450 mV threshold on the LBO outputs at a battery voltage of 1.23 V, a 680-kΩ resistor should be chosen for R1. The resulting battery voltages of the other thresholds can be calculated using Equation 4:

$$V_{BAT} = V_{LBI\text{-}threshold} \times \left(\frac{R1}{R2} + 1 \right) = 500\ mV \times \left(\frac{680\ k\Omega}{390\ k\Omega} + 1 \right) \quad (4)$$

The result for the 500-mV threshold in our example is 1.37 V and for the 400-mV threshold 1.1 V. This results in the following truth table for the battery supervisor outputs:

VBAT [V]	$\overline{LBO1}$	$\overline{LBO2}$
0-1.1	0	0
1.1-1.23	1	0
1.23-1.37	0	1
1.37-VBAT max	1	1

If the application requires only a simple LBI/LBO function both LBO outputs can be connected together. The LBI threshold then is 500 mV.

The outputs of the low battery supervisor are simple open-drain outputs that go active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the boost converter. If not used, the LBO pin can be left floating or tied to GND.

Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6110x's switch is 1200 mA at an output voltage of 3.3 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 5:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (5)$$

For example, for an output current of 100 mA at 3.3 V, at least 515 mA of current flows through the inductor at a minimum input voltage of 0.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using Equation 6:

$$L = \frac{V_{BAT} \times \left(V_{OUT} - V_{BAT}\right)}{\Delta I_L \times f \times V_{OUT}} \quad (6)$$

Parameter 0 is the switching frequency andΔ I_L is the ripple current in the inductor, i.e., 20% $\times$ I_L. In this example, the desired inductor has the value of 12 µH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in Equation 5. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

Table 1. Inductors

VENDOR	RECOMMENDED INDUCTOR SERIES
Sumida	CDRH73
	CDRH74
	CDRH5D18
	CDRH6D38
Coiltronics	DR73
	DR74
Murata	LQS66C
	LQN6C
TDK	SLF 7045
	SLF 7032
Wurth Electronic	WE-PD Type M
	WE-PD Type S

CAPACITOR SELECTION

Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

Output Capacitor Boost Converter

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 7:

$$C_{min} = \frac{I_{OUT} \times \left(V_{OUT} - V_{BAT}\right)}{f \times \Delta V \times V_{OUT}} \quad (7)$$

Parameter *f* is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 15 mV, a minimum capacitance of 10 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 8:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (8)$$

An additional ripple of 10 mV is the result of using a tantalum capacitor with a low ESR of 100 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 25 mV. It is possible to improve the design by enlarging the capacitor or using smaller capacitors in parallel to reduce the ESR or by using better capacitors with lower ESR, like ceramics. So, trade-offs have to be made between performance and costs of the converter circuit.

Output Capacitor LDO

To ensure stable output regulation, it is required to use an output capacitor at the LDO output. We recommend using ceramic capacitors in the range from 1 µF up to 4.7 µF. At 4.7 µF and above it is recommended to use standard ESR tantalum. There is no maximum capacitance value.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

APPLICATION EXAMPLES

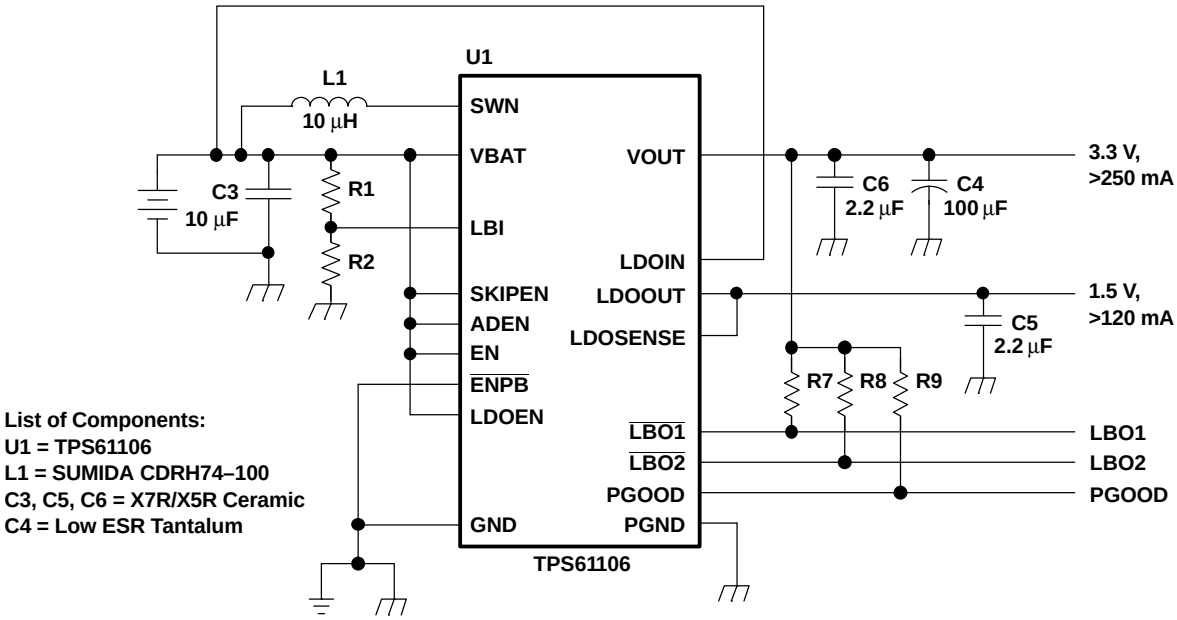


Figure 29. Solution for Maximum Output Power

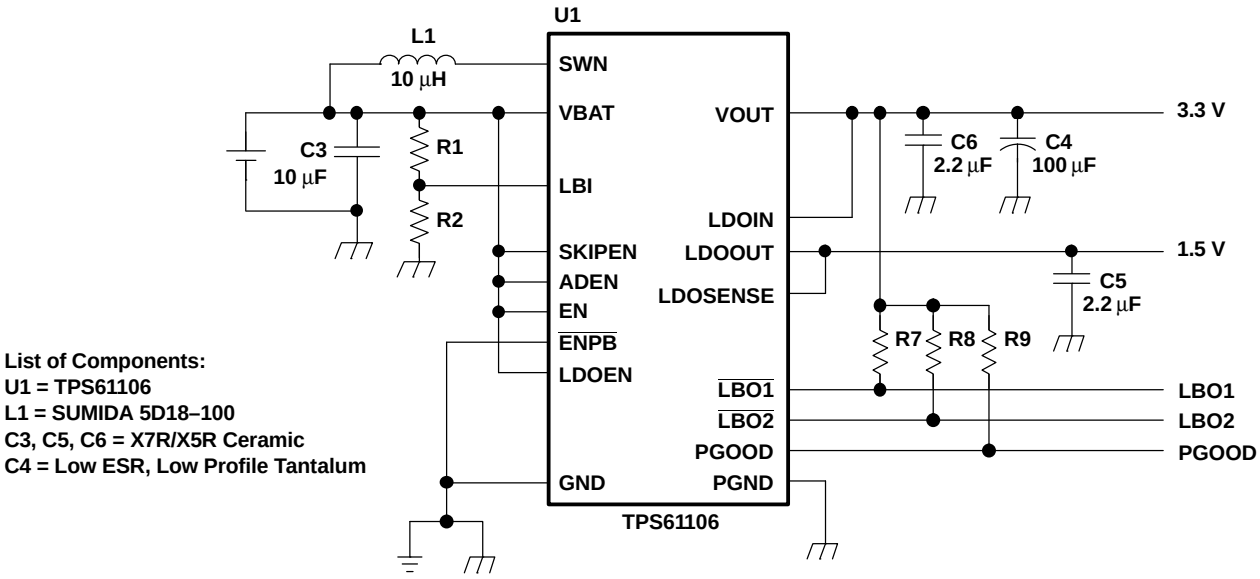


Figure 30. Low Profile Solution, Maximum Height 1,8 mm

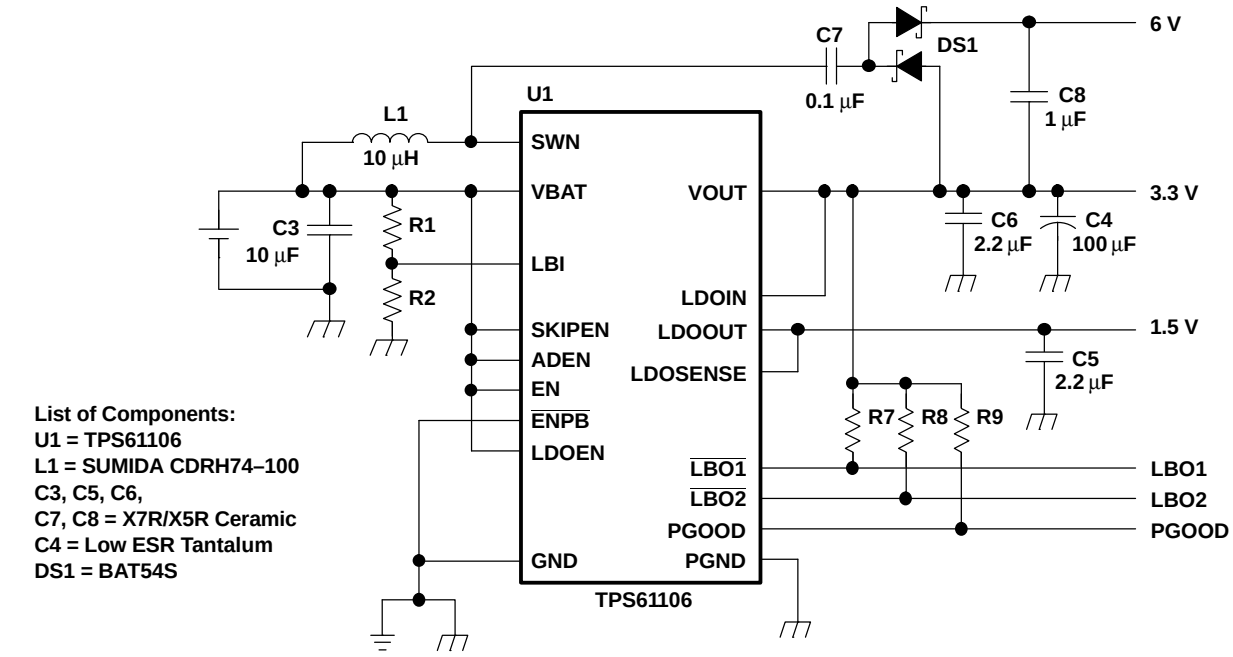


Figure 31. Dual Power Supply With Auxiliary Positive Output Voltage

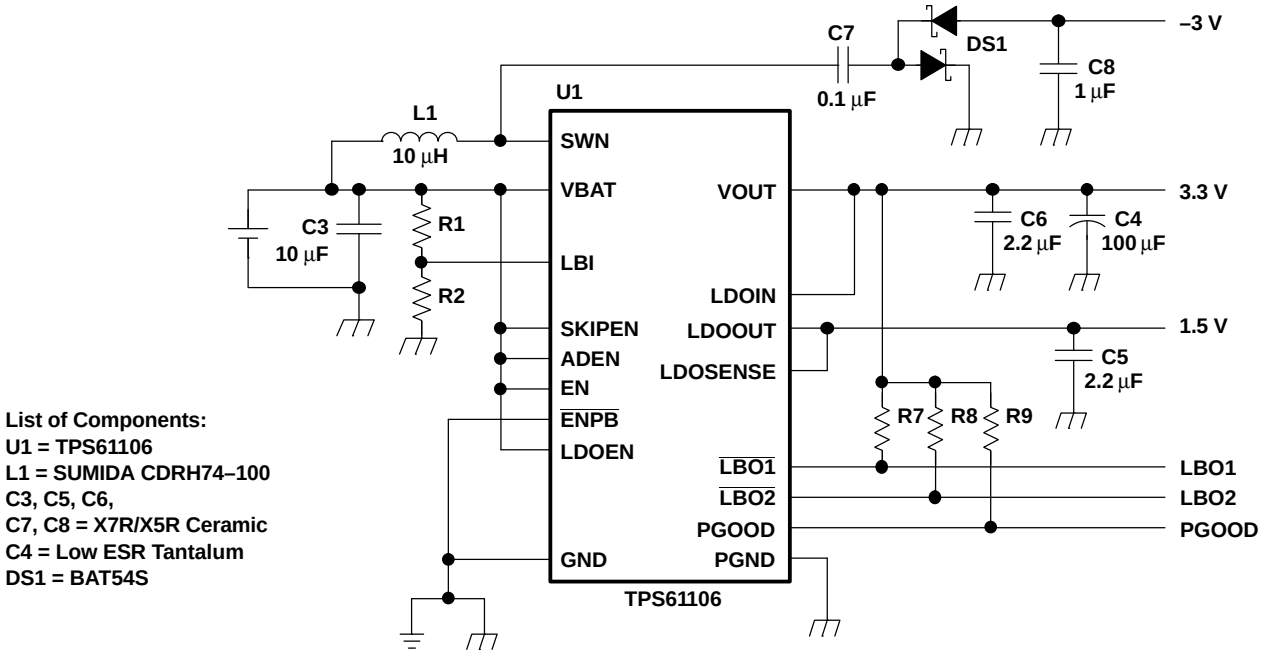


Figure 32. Dual Power Supply With Auxiliary Negative Output Voltage

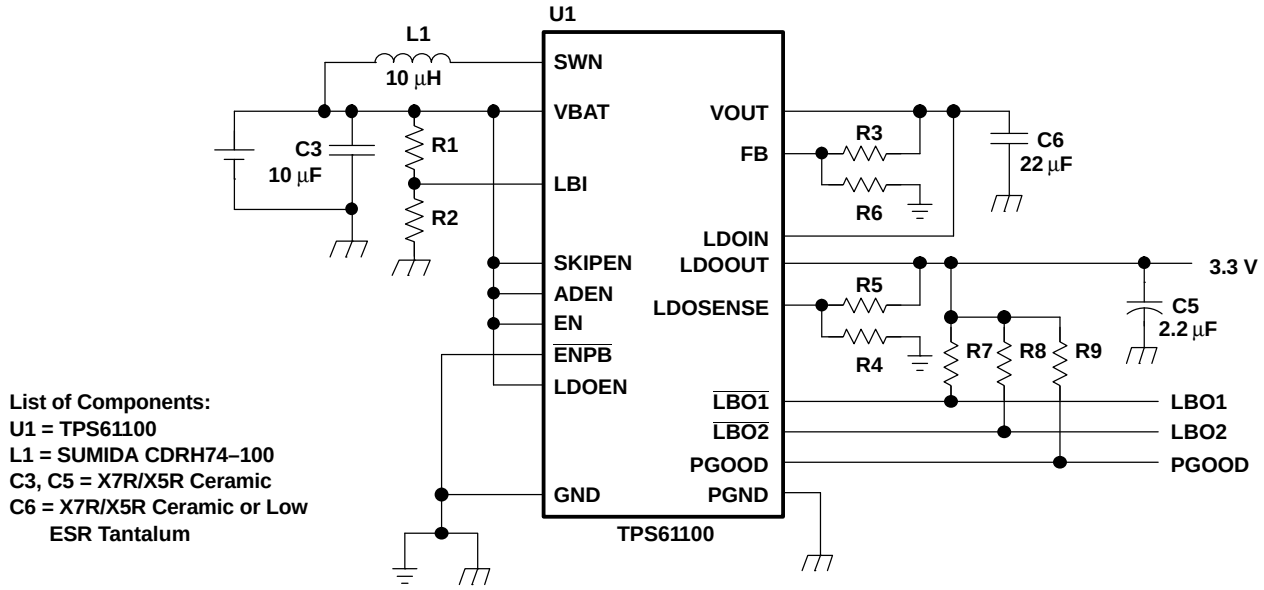


Figure 33. Single Output Using LDO as Filter

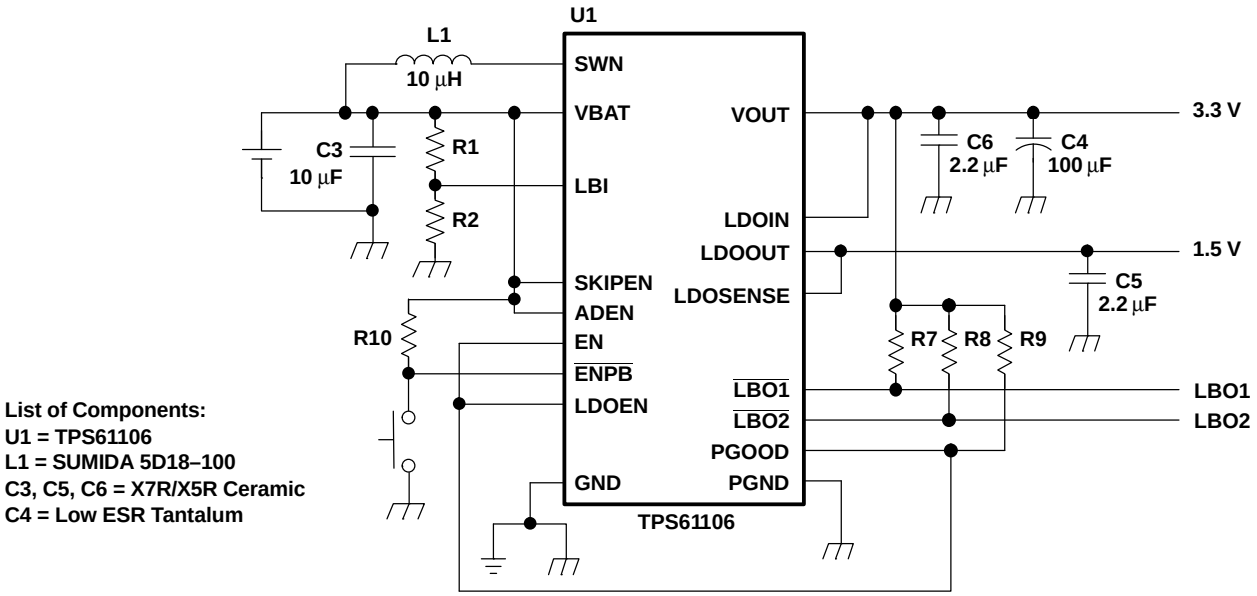


Figure 34. Simple Solution Using a Pushbutton for Start-Up

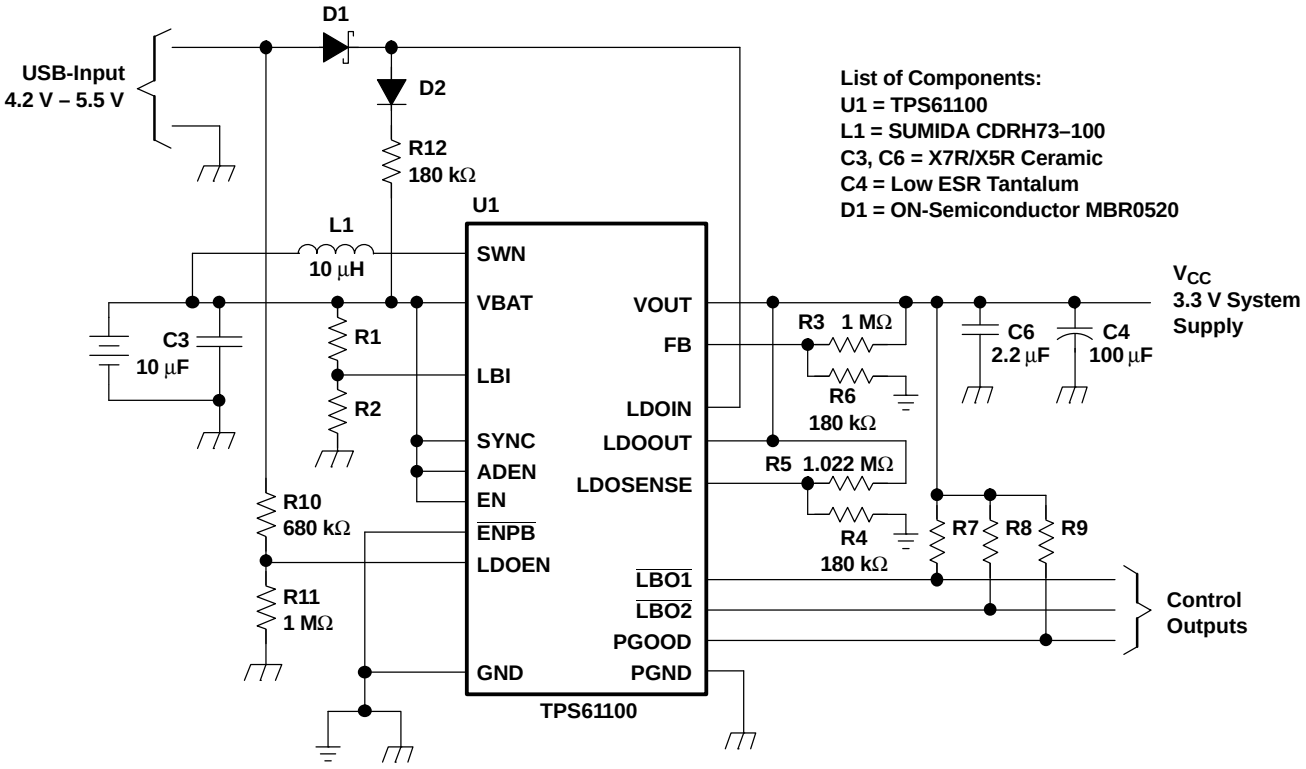


Figure 35. Dual Input Power Supply

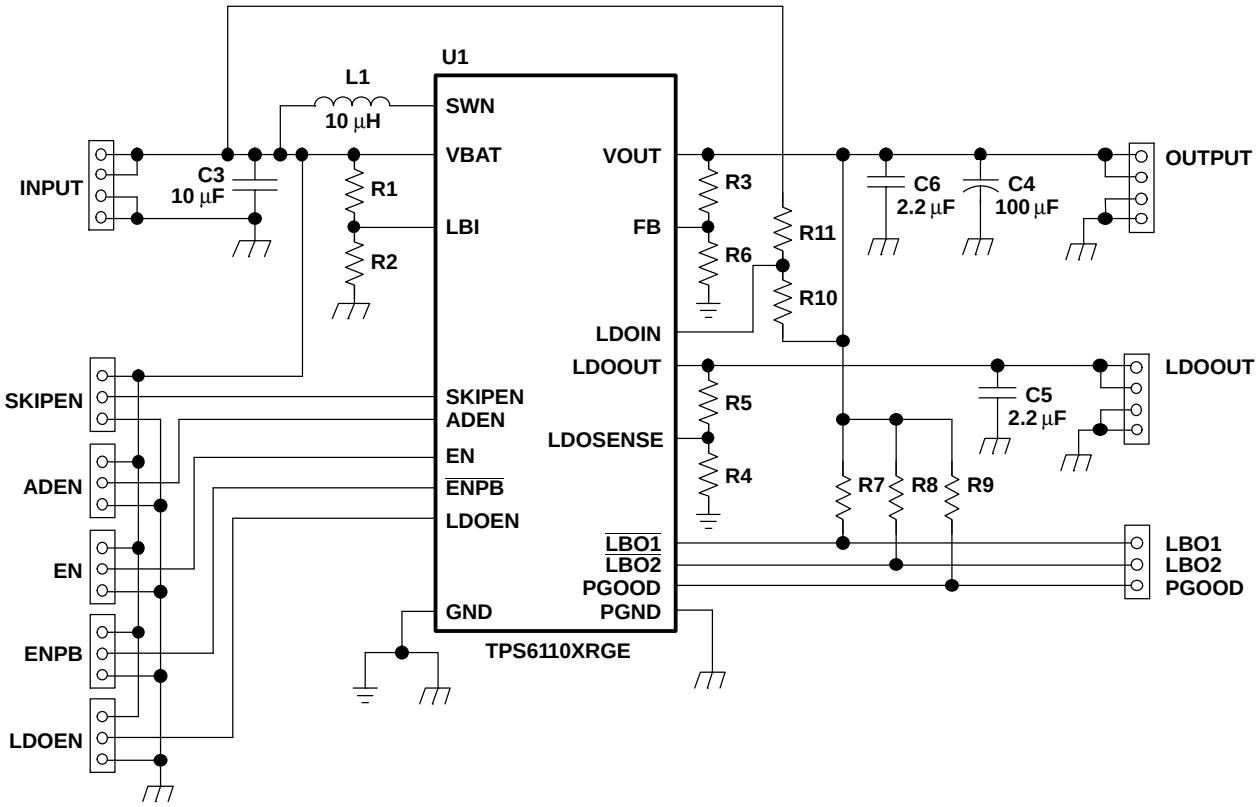


Figure 36. TPS6110x EVM Circuit Diagram

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow in the system.

The maximum junction temperature (T_J) of the TPS6110x devices is 150°C. The thermal resistance of the 20-pin TSSOP package (PW) is$R_{\Theta JA}$ = 155 K/W (QFN package, RGE, 161 K/W). Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 420 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{150°C - 85°C}{155\ k/W} = 420\ mW \quad (9)$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61100PW	NRND	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61100	
TPS61100PWG4	NRND	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61100	
TPS61100PWR	NRND	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61100	
TPS61100PWRG4	NRND	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61100	
TPS61100RGER	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 61100	
TPS61100RGERG4	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 61100	
TPS61103PW	NRND	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61103	
TPS61103PWG4	NRND	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61103	
TPS61103RGER	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 61103	
TPS61103RGERG4	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 61103	
TPS61106PW	NRND	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61106	
TPS61106PWG4	NRND	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
TPS61107PW	NRND	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61107	
TPS61107PWG4	NRND	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61107	
TPS61107PWR	NRND	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS61107	
TPS61107PWRG4	NRND	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
TPS61107RGER	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 61107	
TPS61107RGERG4	NRND	VQFN	RGE	24		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

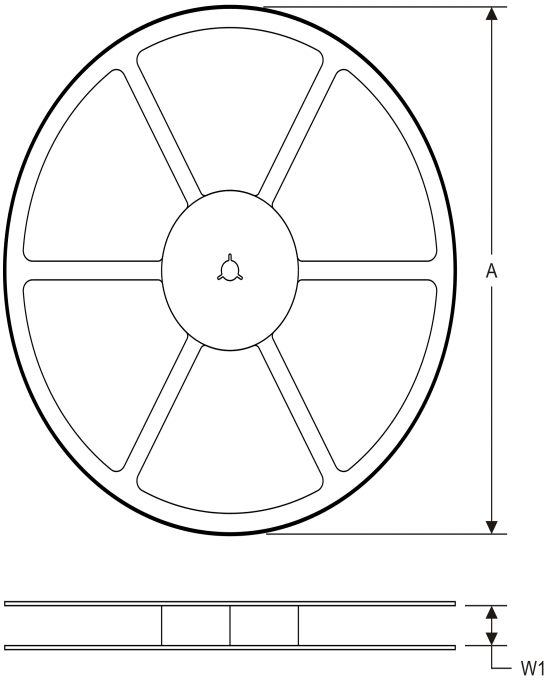
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

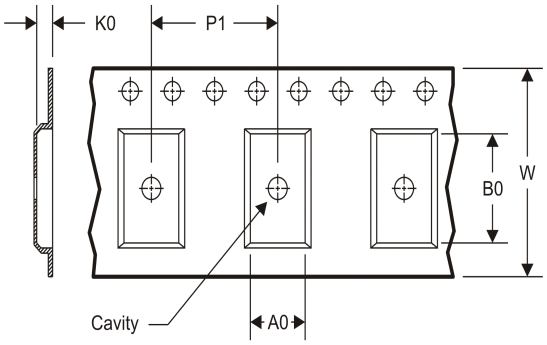
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



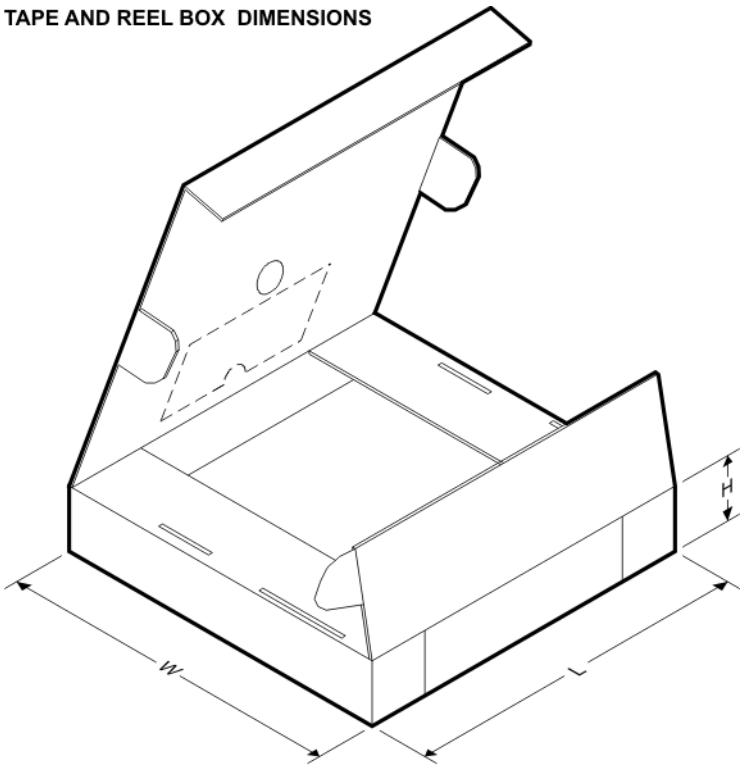
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61100PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS61100RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS61103RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS61107PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS61107RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

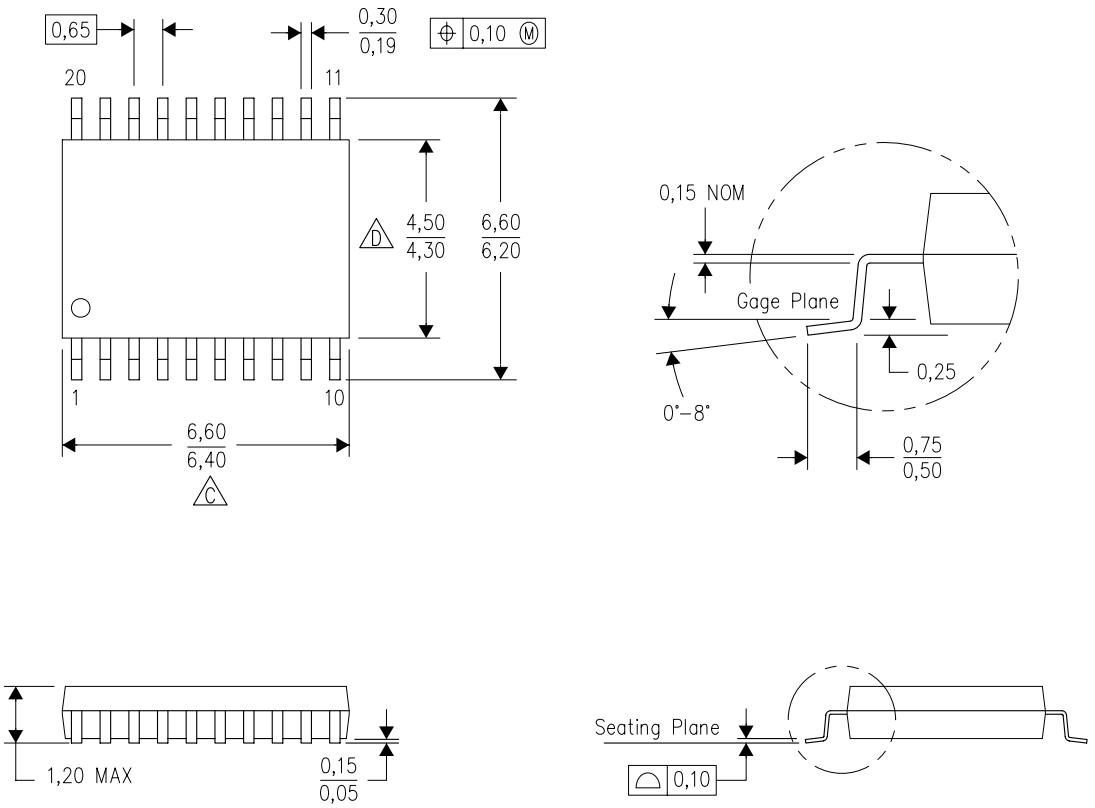
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61100PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TPS61100RGER	VQFN	RGE	24	3000	338.1	338.1	20.6
TPS61103RGER	VQFN	RGE	24	3000	338.1	338.1	20.6
TPS61107PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TPS61107RGER	VQFN	RGE	24	3000	338.1	338.1	20.6

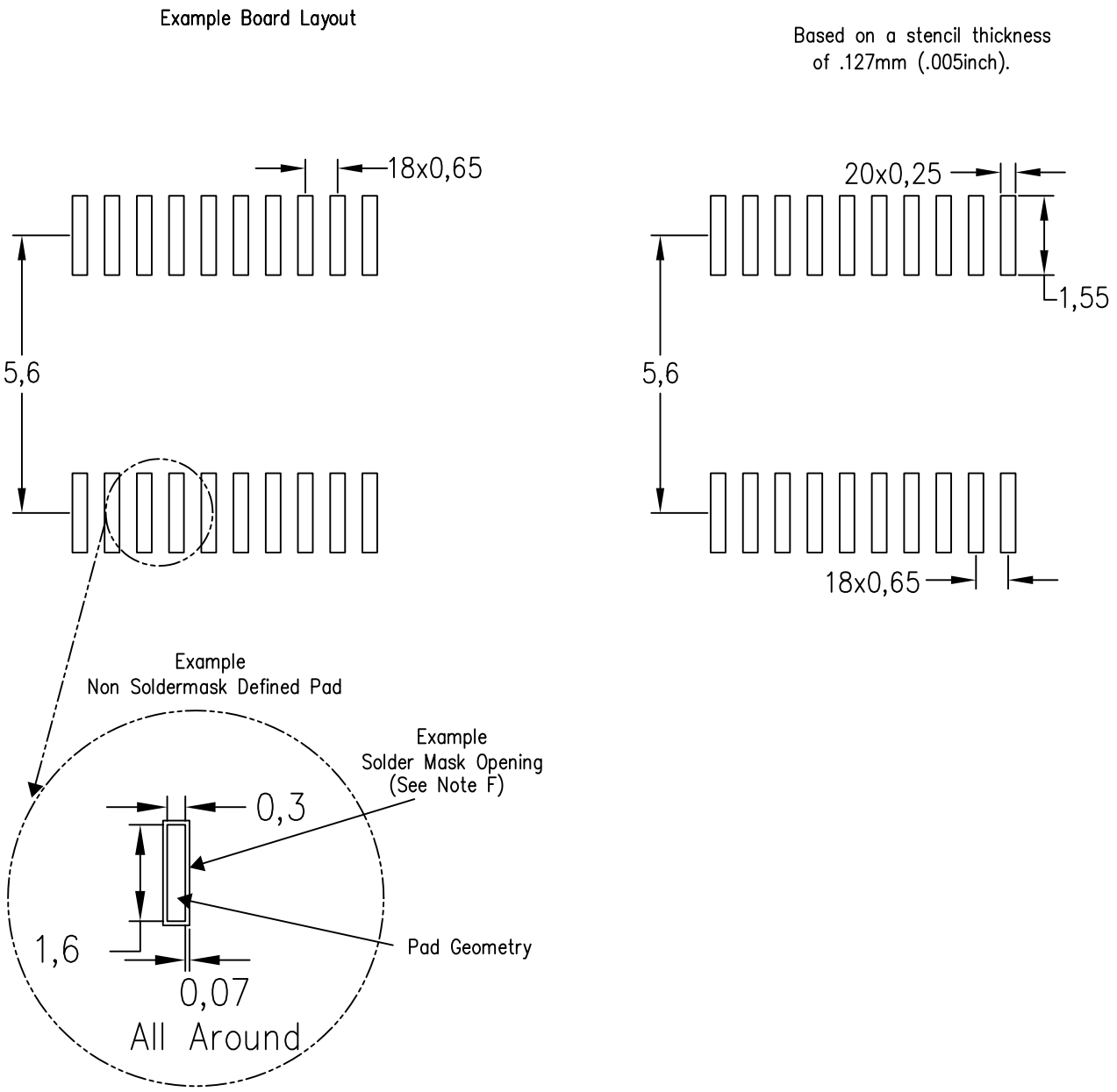
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

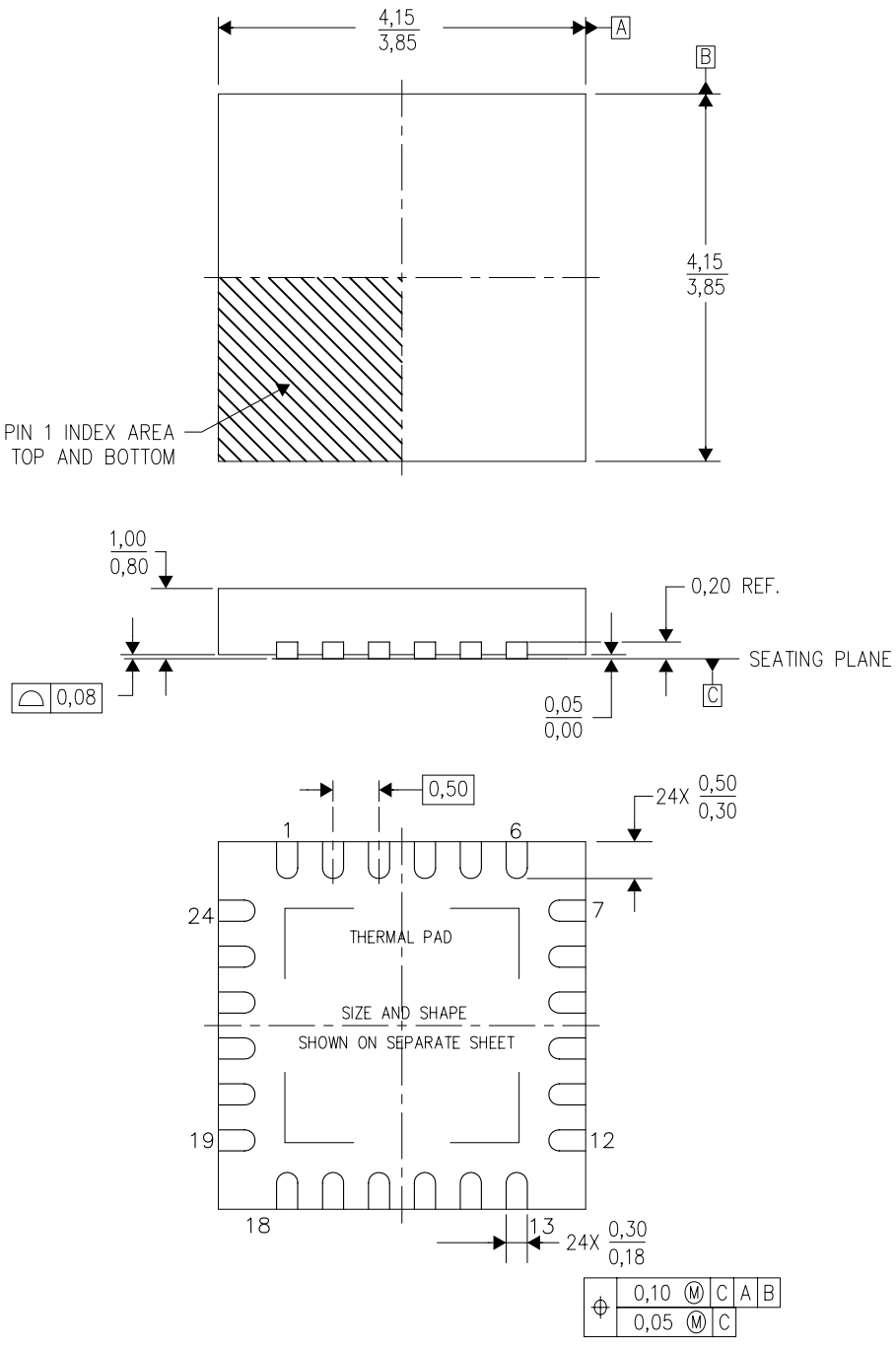
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

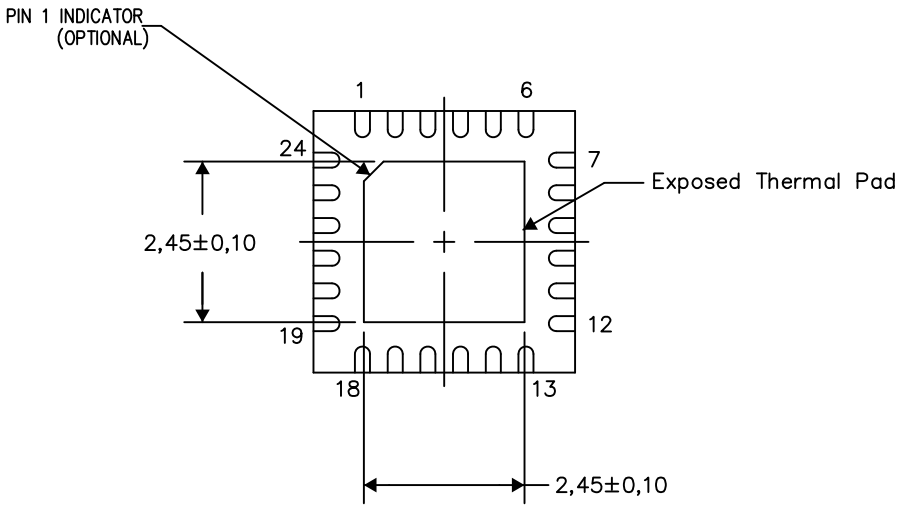
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



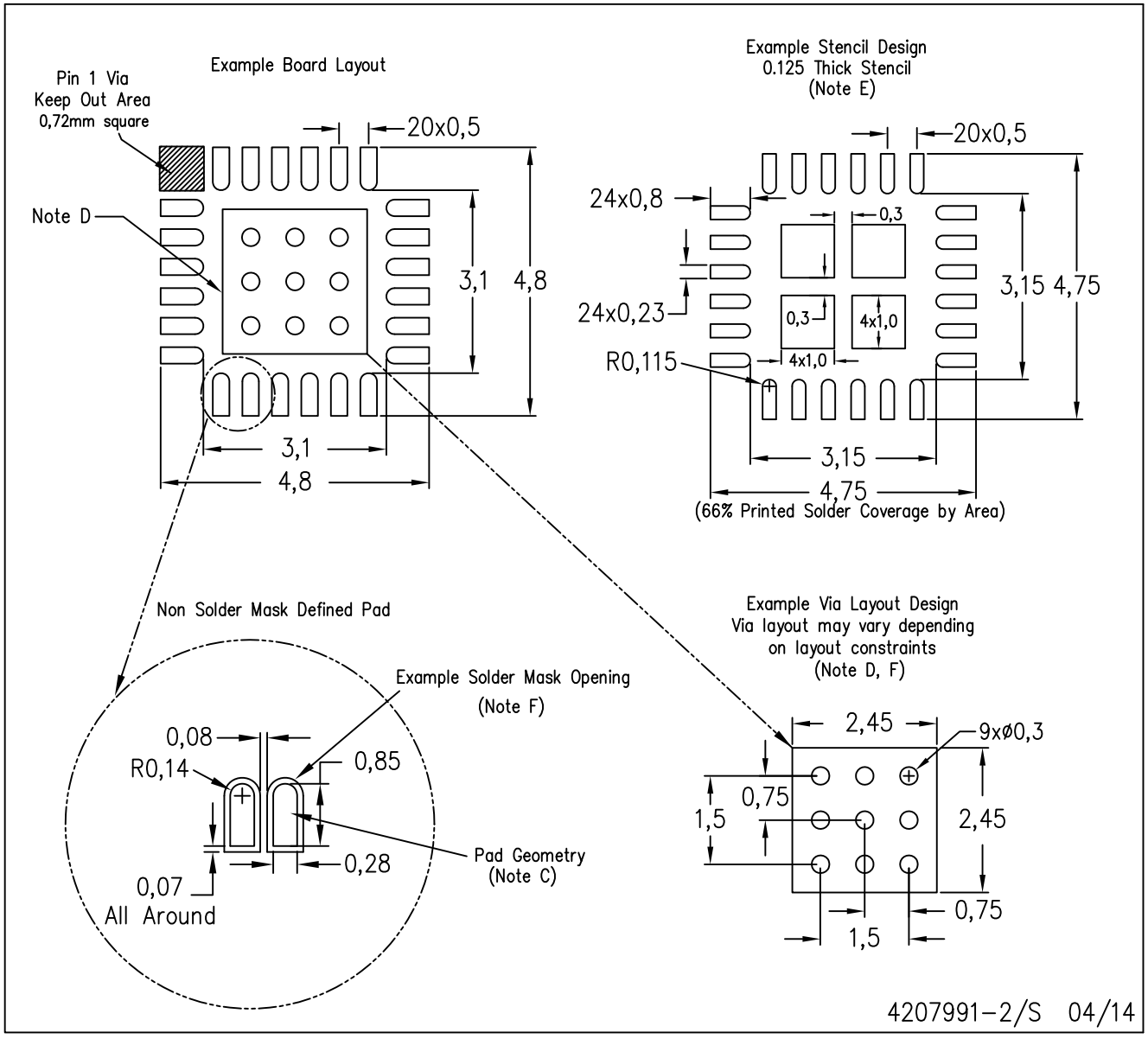
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AG 04/14

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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