

1-10 Clock Buffer for Networking Applications

Features

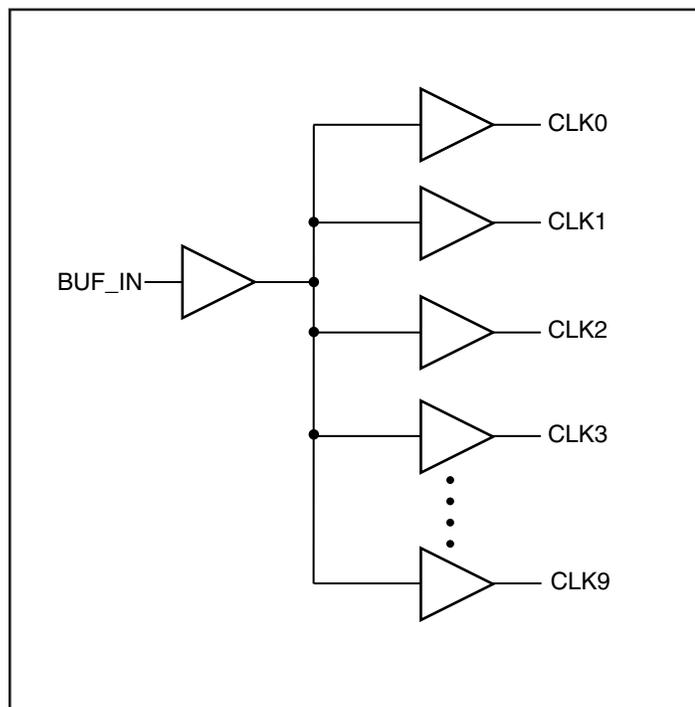
- Maximum Frequency up to 156 MHz
- High-speed, low-noise, non-inverting 1-10 buffer
- Low-skew (<250ps) between any two output clocks
- Low duty cycle distortion <250ps
- Low propagation delay <2.5ns
- Multiple V_{DD}, GND pins for noise reduction
- 3.3V supply voltage with 5V input tolerant
- Packages (Pb-free & Green Available):
 - 20-pin 300-mil wide SOIC (S)
 - 20-pin 209-mil wide SSOP (H)
 - 20-pin 150-mil wide QSOP (Q)

Description

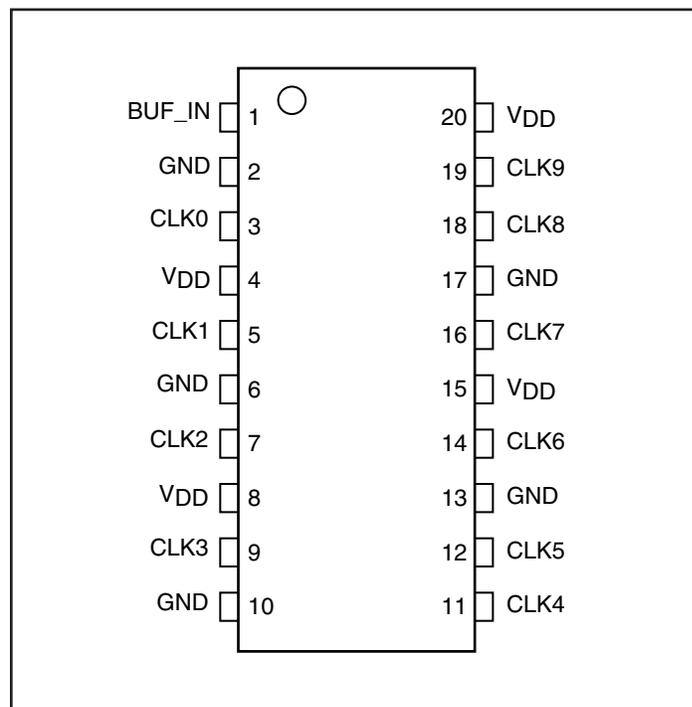
The PI49FCT3807D is a 3.3V high-speed, low-noise 1-10 non-inverting clock buffer. The key goal in designing the PI49FCT3807D is to target networking applications that require low-skew, low-jitter, and high-frequency clock distribution.

Providing output-to-output skew as low as 250ps, the PI49FCT3807D is an ideal clock distribution device for synchronous systems. Designing synchronous networking systems requires a tight level of skew from a large number of outputs.

Block Diagram



Pin Configuration



Pin Description

Pin Name	Description
BUF_IN	Input
CLK [0:9]	Outputs
GND	Ground
VDD	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
V _{DD} Voltage	-0.5V to +4.6V
Output Voltage.....	-0.5V to V _{DD} +0.5V
Input Voltage	-0.5V to +5.5V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

V _{DD} Voltage	3.3V ± 0.3V
Industrial Temperature	-40°C to +105°C
Input Frequency.....	DC to 156 MHz

DC Electrical Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH level (Input Pins)	2.0		5.5	V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW level (Input Pins)	-0.5		0.8	
I _{IH}	Input HIGH Current	V _{DD} = Max			1	μA
I _{IL}	Input LOW Current	V _{DD} = Max			1	
V _{IK}	Clamp Diode Voltage	V _{DD} = Min. I _{IN} = -18mA		-0.7	-1.2	V
V _{OH}	Output High Voltage	V _{DD} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = 0.1mA	V _{DD} -0.2		
			I _{OH} = -12mA	2.4 ⁽³⁾	3.0	
V _{OL}	Output LOW Voltage	V _{DD} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1mA		0.2	
			I _{OL} = 12mA		0.3	0.5
I _{ODH}	Output HIGH Current	V _{DD} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ^(4, 5)	-45	-75	-180	mA
I _{ODL}	Output LOW Current	V _{DD} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ^(4, 5)	50	80	200	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{DD} = 3.3V, +25°C ambient and maximum loading.
- V_{OH} = V_{DD} - 0.6V at rated current.
- This parameter is determined by device characterization but is not production tested.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
I_{DDQ}	Quiescent Power Supply Current	$V_{DD} = \text{Max.}$	$V_{IN} = \text{GND or } V_{DD}$		0.1	30	μA
ΔI_{DD}	Supply Current per Inputs @ TTL HIGH	$V_{DD} = \text{Max.}$	$V_{IN} = V_{DD} - 0.6\text{V}^{(3)}$		47	300	
I_D	Dynamic Supply Current	$V_{DD} = 3.6\text{V},$ No Load	50 MHz		43	55	mA
			67 MHz		56	70	
			80 MHz		66	85	
			100 MHz		81	105	
			125 MHz		97	125	
			156 MHz		121	155	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at $V_{DD} = 3.3\text{V}, +25^\circ\text{C}$ ambient.
3. Per TTL driven input ($V_{IN} = V_{DD} - 0.6\text{V}$); all other inputs at V_{DD} or GND.

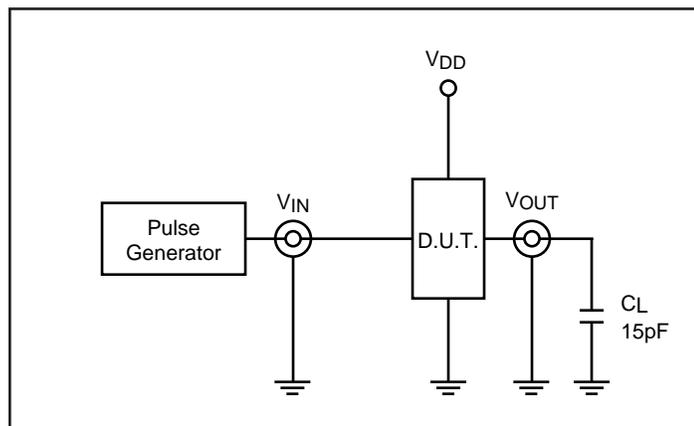
Capacitance ($T_A = 25^\circ\text{C}, f = 1\text{ MHz}$)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	3.0	4	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	—	6	

Note:

1. This parameter is determined by device characterization but is not production tested.

Test Circuits for All Outputs



Definitions:

- C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{out} of the Pulse Generator.

Switching Characteristics ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 85^\circ C$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
t_R/t_F	CLKn Rise/Fall Time 0.8V ~ 2.0V	$C_L = 15pF, 125 MHz$		0.8	1.0	ns
t_{PLH} t_{PHL}	Propagation Delay BUF_IN to CLKn		1.0	2.2	2.5	
$t_{SK(o)}^{(3)}$	Skew between two outputs of the same package (same transition)			110	250	ps
$t_{SK(p)}^{(3)}$	Skew bewteen opposite transitions ($t_{PHL}-t_{PLH}$) of the same output			200	250	
$t_{SK(o)}^{(3)}$	Skew between two outputs of different package ⁽⁴⁾				550	

Notes:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).
4. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.

Switching Characteristics ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 105^\circ C$)

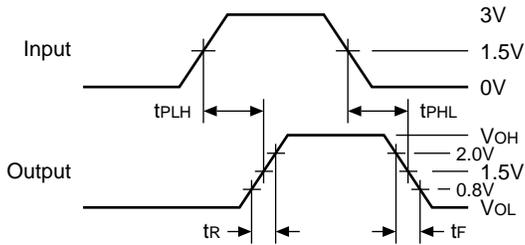
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t_R/t_F	CLKn Rise/Fall Time 0.8V ~ 2.0V	$C_L = 15pF, 125 MHz$		0.8	1.0	ns
t_{PLH} t_{PHL}	Propagation Delay BUF_IN to CLKn		1.0	2.8	3.0	
$t_{SK(o)}^{(3)}$	Skew between two outputs of the same package (same transition)			110	250	ps
$t_{SK(p)}^{(3)}$	Skew bewteen opposite transitions ($t_{PHL}-t_{PLH}$) of the same output			200	250	
$t_{SK(o)}^{(3)}$	Skew between two outputs of different package ⁽⁴⁾				550	

Notes:

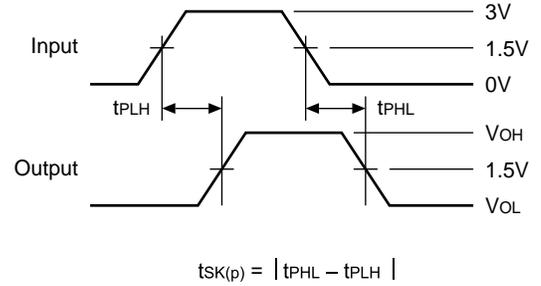
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).
4. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.

Switching Waveforms

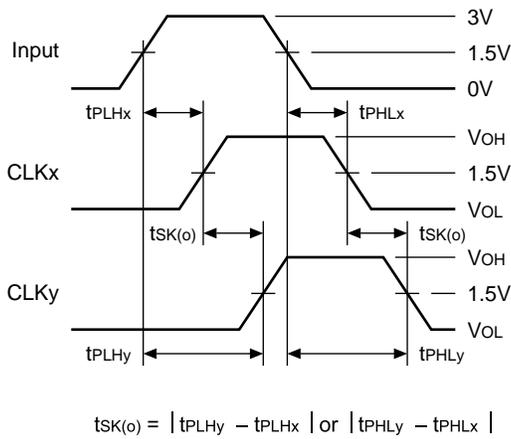
Propagation Delay



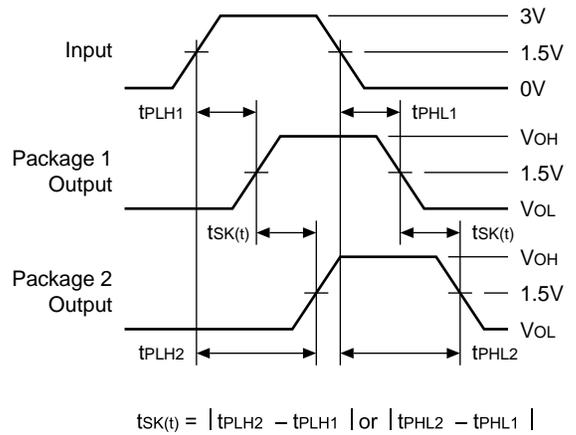
Pulse Skew – $t_{SK(P)}$



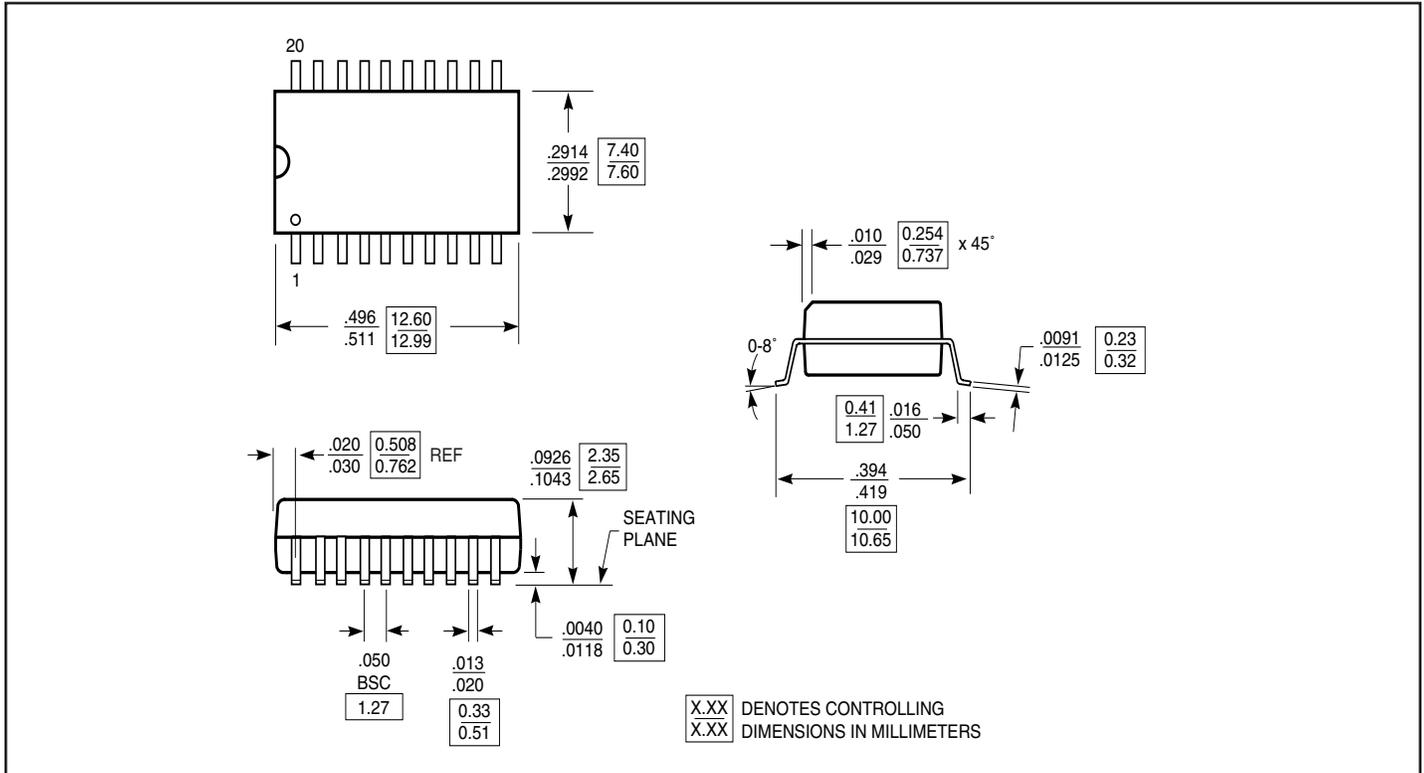
Output Skew – $t_{SK(O)}$



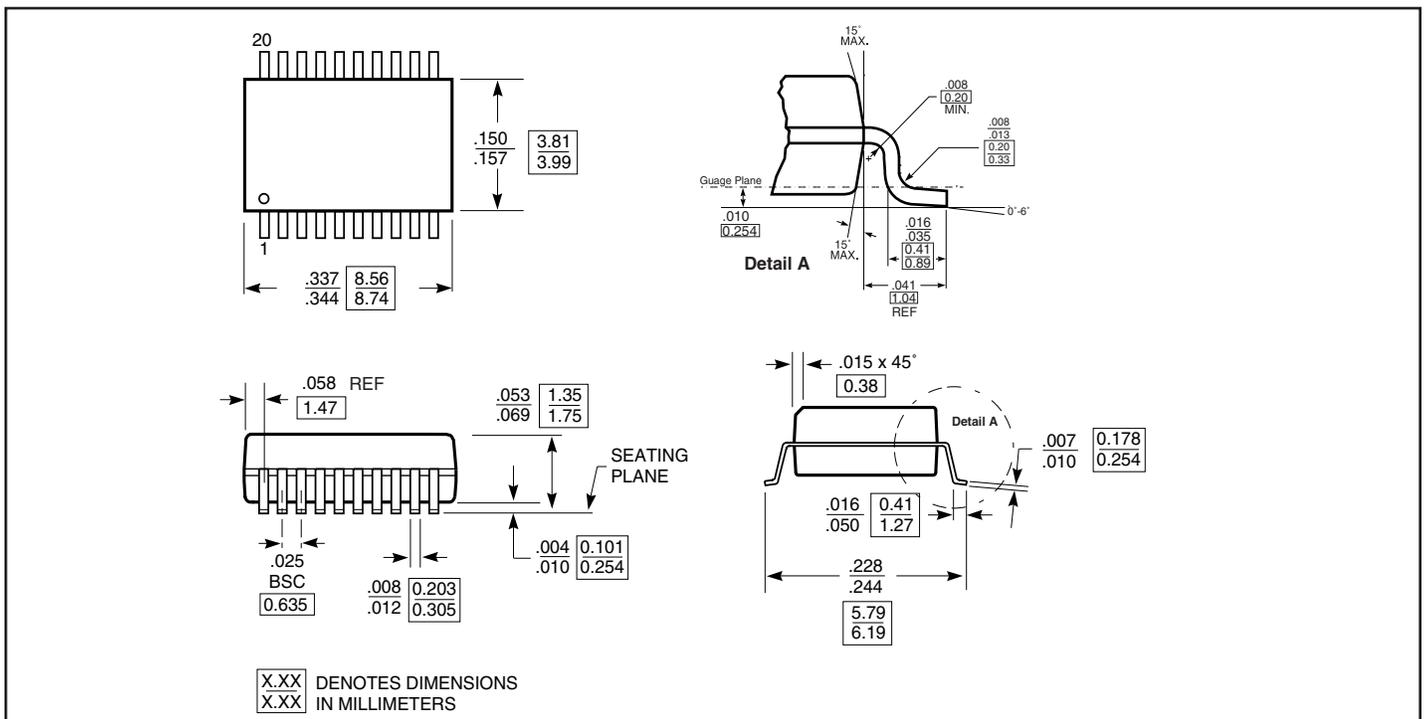
Package Skew – $t_{SK(T)}$



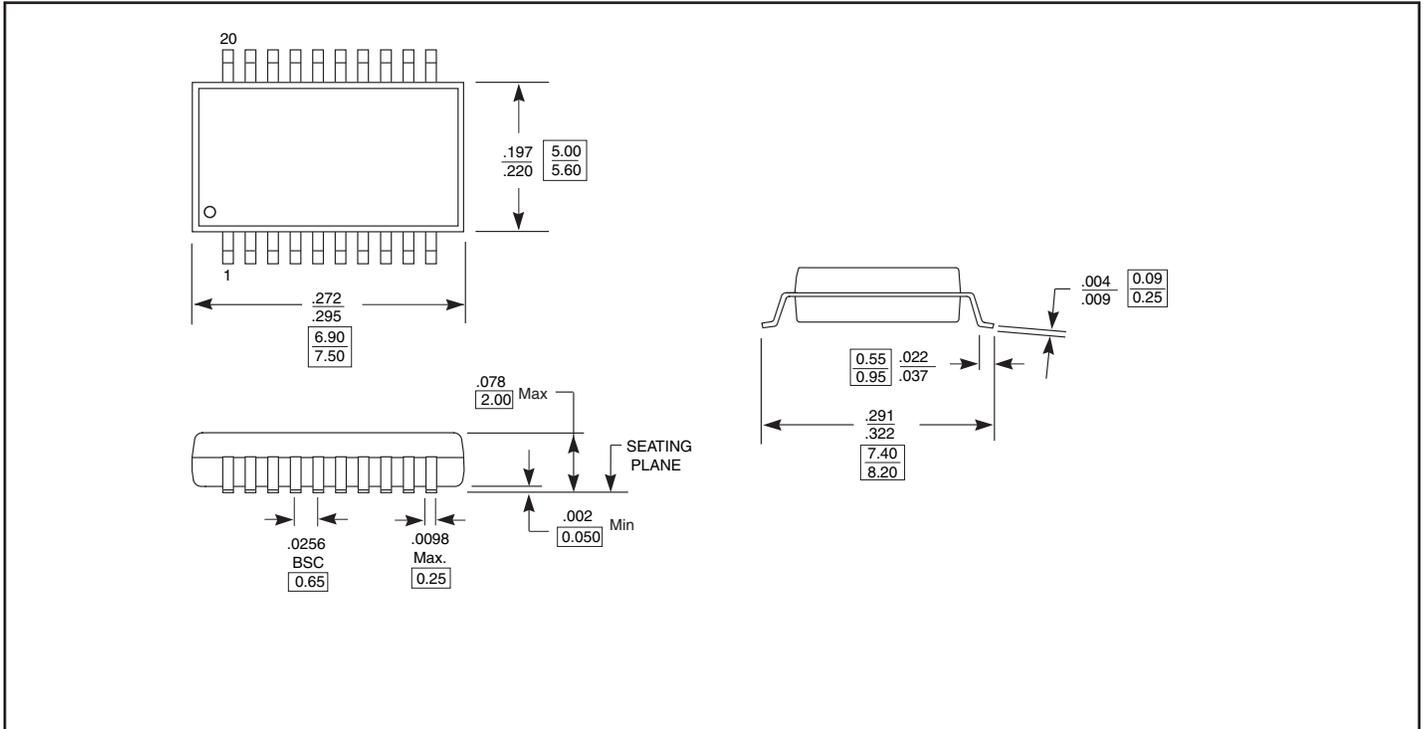
Packaging Mechanical: 20-Pin SOIC (S)



Packaging Mechanical: 20-Pin QSOP (Q)



Packaging Mechanical: 20-Pin SSOP (H)



Ordering Information

Ordering Code	Package Code	Package Type
PI49FCT3807DS	S	20-pin 300-mil wide SOIC
PI49FCT3807DSE	S	Pb-free & Green, 20-pin 300-mil wide SOIC
PI49FCT3807DQ	Q	20-pin 150-mil wide QSOP
PI49FCT3807DQE	Q	Pb-free & Green, 20-pin 150-mil wide QSOP
PI49FCT3807DH	H	20-pin 20-mil wide SSOP
PI49FCT3807DHE	H	Pb-free & Green, 20-pin 209-mil wide SSOP

Notes:

1. Thermal Characteristics can be found on the web at www.pericom.com/packaging/