19-3937; Rev 1; 10/94

MAXIM

High-Speed, Threshold-Programmable Voltage Comparators

General Description

The MAX910/MAX911 are the first high-speed comparators to include an 8-bit DAC with voltage reference to set the input threshold voltage. The MAX910 has a TTL compatible output while the MAX911 output is fully differential and ECL compatible. Comparator propagation delay is 8ns for the MAX910 and only 4ns for the MAX911. For high-speed comparator applications where the threshold must be updated rapidly, such as automatic test equipment (ATE) or process control applications, the MAX910/MAX911 provide a complete, single IC solution which significantly reduces stray capacitance, board space, design time and cost over multi-chip, discrete solutions.

The comparator threshold level, set by the DAC, has 10mV or 20mV pin-selectable resolution (a full-scale range of either 2.56V or 5.12V) when used with the internal reference. An external reference input is also provided.

The MAX910/MAX911 feature separate power and comparator ground pins to eliminate coupling between the comparator output and analog input. Both parts can be powered from either ±5V, or +5V and -5.2V supplies.

Applications

Analog-to-Digital Converters

Voltage-to-Frequency Converters

Threshold Detectors

Window Discriminators

Sampling

Automatic Test Equipment

Features

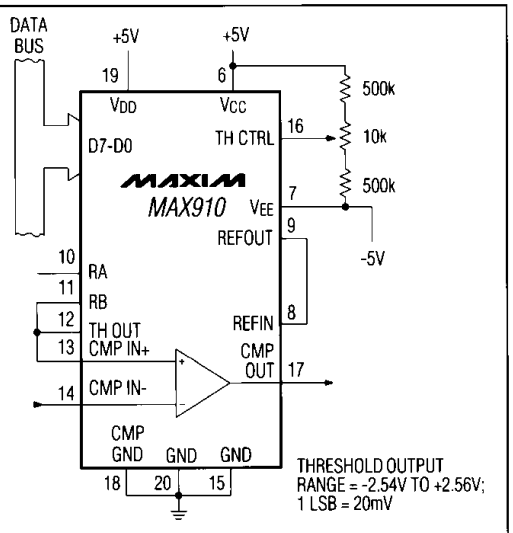
- **8ns Propagation Delay, TTL-Compatible Output (MAX910)**
- **4ns Propagation Delay, ECL-Compatible Output (MAX911)**
- **200mW Power Dissipation**
- **8-Bit Digitally Programmable Threshold Level**
- **Internal +2.56V Voltage Reference**
- **2.56V or 5.12V Full-Scale Range**
- **Separate Analog and Digital Supplies**
- **Comparator Output Latch Function**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX910CAG	0°C to +70°C	24 SSOP**
MAX910CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX910CWG	0°C to +70°C	24 Wide SO
MAX910C/D	0°C to +70°C	Dice*

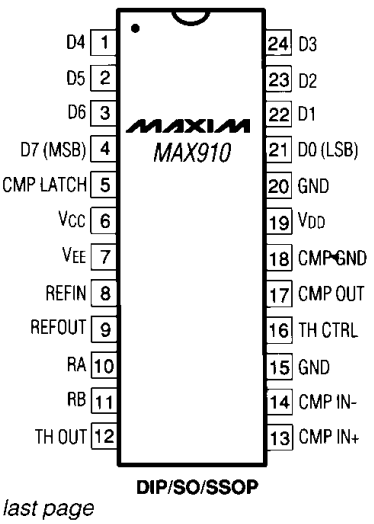
** Dice are specified at T_A = +25°C, DC parameters only.*
*** Contact factory for pricing and availability.*

Typical Operating Circuit



PROGRAMMABLE LEVEL DETECTOR

Pin Configurations



DIP/SO/SSOP

MAX911 on last page

Call toll free 1-800-998-8800 for free samples or literature.

High-Speed, Threshold-Programmable Voltage Comparators

ABSOLUTE MAXIMUM RATINGS (Note 1)

Analog Supply Voltage (V_{CC} to V_{EE}) ..... +12V
Digital Supply Voltage (V_{DD} to GND) ..... +6V
V_{EE} to GND ..... -6V
CMP GND to GND ..... ±1V
CMP IN+ to CMP IN- ..... [V_{EE} - 0.2V] to [V_{CC} + 0.2V]
TH CTRL ..... [V_{EE} - 0.2V] to [V_{CC} + 0.2V]
D0-D7 ..... -0.2V to [V_{DD} + 0.2V]
REFIN ..... [V_{EE} - 0.2V] to [V_{CC} + 0.2V]
CMP OUT Short-Circuit Duration (MAX910 only)
  to GND ..... Indefinite
  to V_{CC} ..... 1 minute
Q and $\overline{Q}$ Continuous Output Current (MAX911 only) 50mA
REFOUT Short-Circuit Duration
  to GND ..... 1 minute
  to V_{CC} ..... Indefinite
TH OUT Short-Circuit Duration
  to V_{EE} ..... 1 minute
  to V_{CC} or GND ..... Indefinite
REFIN Short-Circuit Duration
  to V_{EE} ..... 1 minute
  to V_{CC} or GND ..... Indefinite
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 8.70mW/°C above +70°C) 696mW
  SO (derate 11.76mW/°C above +70°C) 941mW
  SSOP (derate 8.00mW/°C above +70°C) 600mW
Operating Temperature Ranges:
  MAX91_C_ _ ..... 0°C to +70°C
Junction Temperature (Tj) ..... -65°C to +160°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR							
Input Offset Voltage	V_{OS}	V_{CM} = 0V (Note 2)			1.0	3.0	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}			3	6	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			100	400	nA
Wideband Input Voltage Noise	e_n				300		µV
Input Common-Mode Voltage Range	V_{CM}	(Note 3)		-3		3	V
Common-Mode Rejection Ratio	CMRR	-3V < V_{CM} < 3V			50	150	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 4)			100	250	µV/V
Output High Voltage	V_{OH}	MAX910	V_{IN} > 250mV, I_{SOURCE} = 1mA	2.4	3.5		V
		MAX911	V_{IN} > 250mV, R_L = 50Ω to -2V	-0.96		-0.81	
Output Low Voltage	V_{OL}	MAX910	V_{IN} > 250mV, I_{SINK} = 8mA		0.3	0.4	V
		MAX911	V_{IN} > 250mV, R_L = 50Ω to -2V	-1.85		-1.65	
CMP LATCH Input Voltage High	V_{LH}				1.4	2.0	V
CMP LATCH Input Voltage Low	V_{LL}			0.8	1.4		V
CMP LATCH Input Current High	I_{LH}	V_{LH} = 3.0V			1	20	µA
CMP LATCH Input Current Low	I_{LL}	V_{LL} = 0.3V			1	20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input to Output High Response Time	t_{pd+}	MAX910 (Notes 5, 6)		8	10	ns
		MAX911 (Notes 6, 7)		4	6	
Input to Output Low Response Time	t_{pd-}	MAX910 (Notes 5, 6)		8	10	ns
		MAX911 (Notes 6, 7)		4	6	
Latch Disable to Output High Delay	$t_{pd+(D)}$	MAX910		5		ns
		MAX911		1		
Latch Disable to Output Low Delay	$t_{pd-(D)}$	MAX910		5		ns
		MAX911		1		
Latch Setup Time	t_s	MAX910		2.0		ns
		MAX911		0.5		
Latch Hold Time	t_h	MAX910		1.0		ns
		MAX911		0.5		
Latch-Disable Pulse Width	$t_{pw(D)}$	MAX910		5		ns
		MAX911		1		
VOLTAGE REFERENCE						
Reference Voltage Output	VREF	(Note 8)	2.55	2.56	2.57	V
D0-D7						
TTL Input Voltage High	V_{IH}			1.4	2.0	V
TTL Input Voltage Low	V_{IL}		0.8	1.4		V
TTL Input Current High	I_{IH}	V_{IH} = 3.0V		1	20	µA
TTL Input Current Low	I_{IL}	V_{IL} = 0.3V		1	20	µA
THRESHOLD VOLTAGE OUTPUT						
Threshold Voltage Range	V_{TH}	REFIN = 2.56V, TH OUT connected to RB		+2.56 to -2.54		V
		REFIN = 2.56V, TH OUT connected to RA		+2.56 to +0.01		
Threshold Resolution	$V_{TH(R)}$	TH OUT connected to RB		20		mV
		TH OUT connected to RA		10		
Upper Threshold Limit Absolute Error	$V_{TH+(E)}$	(Note 9)		±1	±3	mV
Lower Threshold Limit Absolute Error	$V_{TH-(E)}$	(Notes 10, 11)		±10	±30	mV
Wideband Threshold Voltage Noise	$V_{TH(en)}$			800		µV

High-Speed, Threshold-Programmable Voltage Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Threshold Voltage Differential Nonlinearity	$V_{TH(DNL)}$	(Notes 10, 12)			±10	mV
Threshold Trim Range	$V_{TH(TR)}$	(Note 13)			±100	mV
Threshold Settling Time	t_S (V_{TH})	To 1/2LSB (Note 14)		50	75	ns
POWER REQUIREMENTS						
Positive Analog Supply Current	I_{CC}	(Note 4)		22	30	mA
Negative Analog Supply Current	I_{EE}	(Note 4)		16	25	mA
Digital Supply Current	I_{DD}	MAX910 only; V_{DD} = 5.5V		2	5	mA
Power Dissipation	PD			200	320	mW

ELECTRICAL CHARACTERISTICS

(V_{CC} = + 5V, V_{EE} = -5V, V_{DD} = +5V, T_A = 0°C to 70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR							
Input Offset Voltage	V_{OS}	V_{CM} = 0V (Note 2)			2.0	5.0	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}			4	8	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			150	600	nA
Input Common-Mode Voltage Range	V_{CM}	(Note 3)		-3		3	V
Common-Mode Rejection Ratio	CMRR	-3V < V_{CM} < +3V			75	250	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 4)			150	400	µV/V
Output High Voltage	V_{OH}	MAX910, V_{IN} > 250mV, I_{SOURCE} = 1mA		2.4	3.5		V
		MAX911, V_{IN} > 250mV, R_L = 50Ω to -2V	0°C	-1.010		-0.850	
			+70°C	-0.900		-0.720	
Output Low Voltage	V_{OL}	MAX910, V_{IN} > 250mV, I_{SINK} = 8mA			0.3	0.4	V
		MAX911, V_{IN} > 250mV, R_L = 50Ω to -2V	0°C	-1.870		-1.660	
			+70°C	-1.830		-1.620	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = + 5V, V_{EE} = -5V, V_{DD} = +5V, T_A = 0°C to 70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CMP Latch Input Voltage High	V_{LH}			1.4	2.0	V
CMP Latch Input Voltage Low	V_{LL}		0.8	1.4		V
CMP Latch Input Current High	I_{LH}	V_{LH} = 3.0V		1	20	µA
CMP Latch Input Current Low	I_{LL}	V_{LL} = 0.3V		1	20	µA
Input to Output High Response Time	tpd+	MAX910 (Notes 5, 6)		10	15	ns
		MAX911 (Notes 6, 7)		5	8	
Input to Output Low Response Time	tpd-	MAX910 (Notes 5, 6)		10	15	ns
		MAX911 (Notes 6, 7)		5	8	
VOLTAGE REFERENCE						
Reference Voltage Output	VREF (E)	(Note 8)	2.54	2.56	2.58	V
Reference Voltage Tempco	TC VREF			0.2		mV/°C
D0-D7						
TTL Input Voltage High	V_{IH}			1.4	2.0	V
TTL Input Voltage Low	V_{IL}		0.8	1.4		V
TTL Input Current High	I_{IH}	V_{IN} = 3.0V		1	20	µA
TTL Input Current Low	I_{IL}	V_{IL} = 0.3V		1	20	µA
THRESHOLD VOLTAGE OUTPUT						
Upper Threshold Limit Absolute Error	VTH+(E)	(Note 9)			±5	mV
Lower Threshold Limit Absolute Error	VTH-(E)	(Notes 10, 11)			±30	mV
Threshold Limit Tempco (Note 10)	TCV_{TH}	Positive threshold limit		0.2		mV/°C
		Negative threshold limit		0.2		
Threshold Voltage Differential Nonlinearity	$V_{TH(DNL)}$	(Notes 10, 12)			±15	mV
POWER REQUIREMENTS						
Positive Analog Supply Current	I_{CC}	(Note 4)		22	30	mA
Negative Analog Supply Current	I_{EE}	(Note 4)		16	25	mA
Digital Supply Current	I_{DD}	MAX910 only V_{DD} = 5.5V		2	5	mA
Power Dissipation	PD			200	320	mW

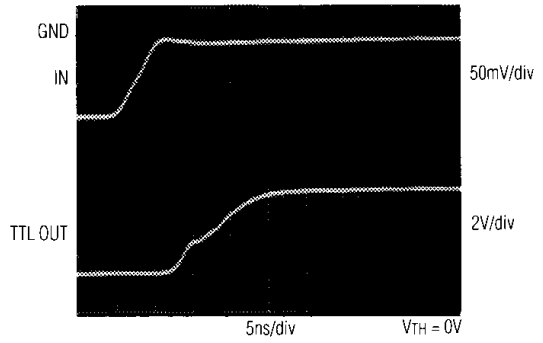
Note 2: Specifications are quoted with CMP OUT = +1.4V (TTL threshold) for the MAX910 and Q OUT, $\overline{Q}$ OUT = -1.3V (ECL threshold) for the MAX911.
Note 3: Inferred from the CMRR test.
Note 4: Tested for +4.75V ≤ V_{CC} ≤ +5.25V, and -5.5V ≤ V_{EE} ≤ +4.75V with V_{DD} = +5V.
Note 5: Conditions for MAX910 switching specifications are 100mV step input with 5mV of overdrive, 15pF of output load capacitance, and 2mA external pull-up load current.
Note 6: Parameter is guaranteed by design.
Note 7: Conditions for MAX911 switching specifications are 100mV step input with 5mV of overdrive, and with both outputs terminated to -2V through 50Ω load resistors
Note 8: VREF specified while supplying internal DAC current (i.e. REFOUT tied to REFIN).
Note 9: Specified with 2.56V applied to REFIN. Specification denotes maximum V_{TH+} deviation from 2.56V.
Note 10: Specified in a 5.10V FS system (i.e. with TH OUT terminated through internal 640Ω span resistor, 2.56V applied to REFIN, and with TH CTRL to GND).
Note 11: V_{TH-} limit quoted as a deviation from the nominal value of -2.54V with conditions specified in Note 10.
Note 12: Tested for each major carry transition of the input digital code.
Note 13: $V_{TH(TR)}$ specified for lower threshold voltage limit (i.e. with data-bits D0-D7 at logic low). A ±50mV change at TH CTRL causes a ±100mV change in V_{TH} -.
Note 14: Guaranteed by design. Specifications are taken from measurements made with a high-speed test fixture, C_{LOAD} = 2pF on TH OUT for both MAX to MIN and MIN to MAX threshold voltage transition and settling to within 10mV (1/2LSB) of the final voltage.

High-Speed, Threshold-Programmable Voltage Comparators

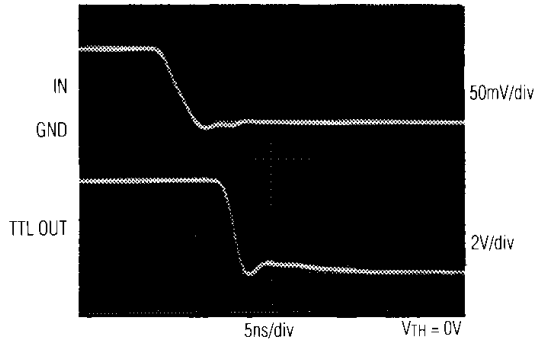
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

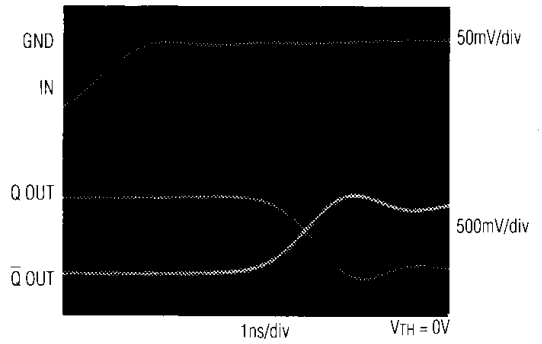
MAX910 t_{pd+} RESPONSE (5mV OVERDRIVE)



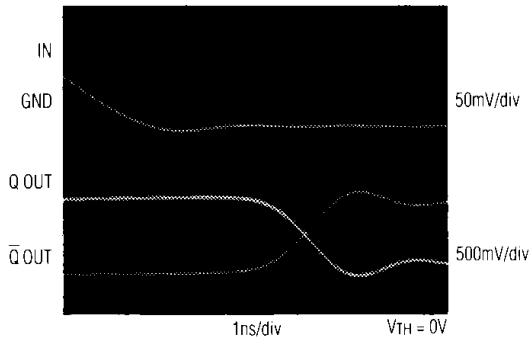
MAX910 t_{pd-} RESPONSE (5mV OVERDRIVE)



MAX911 t_{pd+} RESPONSE (5mV OVERDRIVE)



MAX911 t_{pd-} RESPONSE (5mV OVERDRIVE)

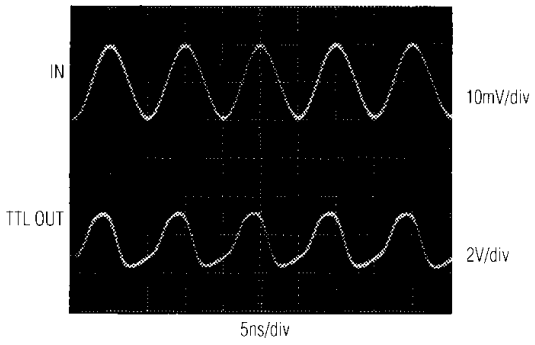


High-Speed, Threshold-Programmable Voltage Comparators

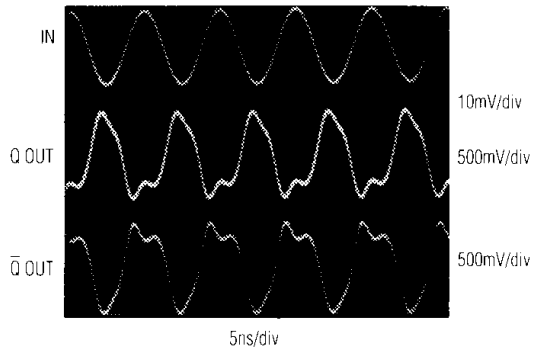
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

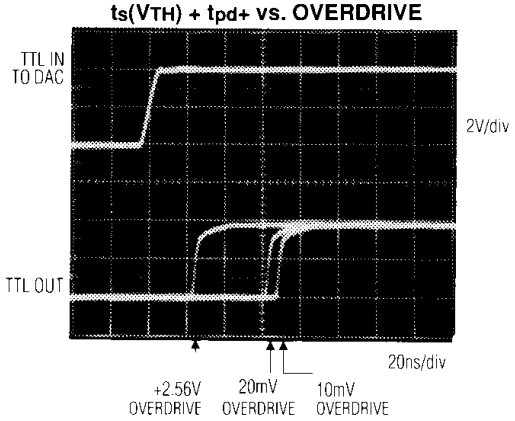
MAX910 100MHz COMPARATOR RESPONSE



MAX911 100MHz COMPARATOR RESPONSE

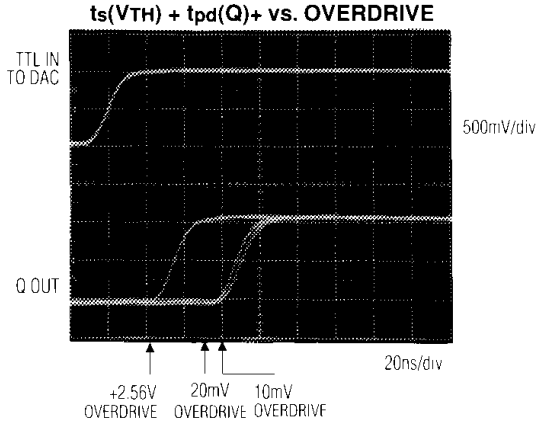


MAX910 ts(VTH) + tpd+ vs. OVERDRIVE



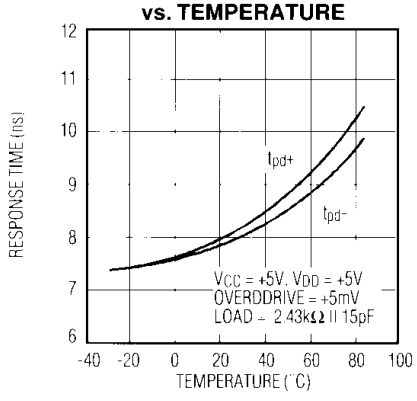
NOTE: CMP IN- CONNECTS TO GND AND TH OUT CONNECTS TO CMP IN+. THE DAC IS UPDATED, CAUSING TH OUT TO OVERDRIVE THE COMPARATOR INPUT.

MAX911 ts(VTH) + tpd(Q)+ vs. OVERDRIVE

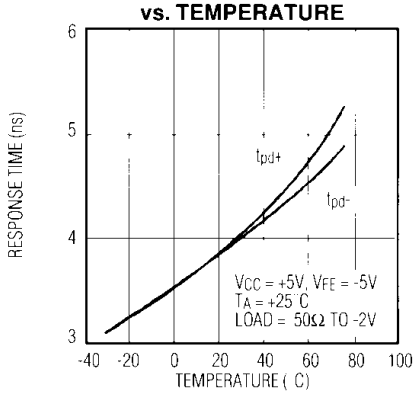


NOTE: CMP IN- CONNECTS TO GND AND TH OUT CONNECTS TO CMP IN+. THE DAC IS UPDATED, CAUSING TH OUT TO OVERDRIVE THE COMPARATOR INPUT.

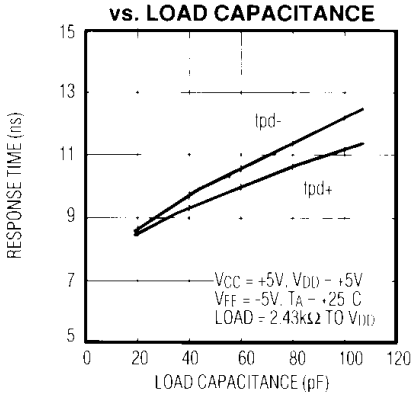
MAX910 RESPONSE TIME vs. TEMPERATURE



MAX911 RESPONSE TIME vs. TEMPERATURE



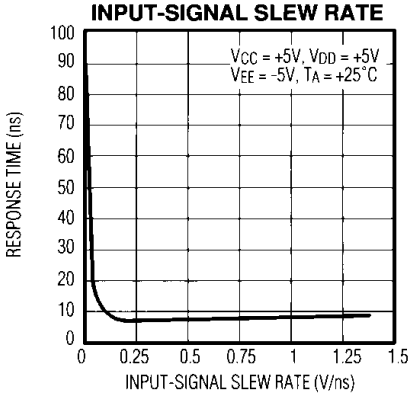
MAX910 RESPONSE TIME vs. LOAD CAPACITANCE



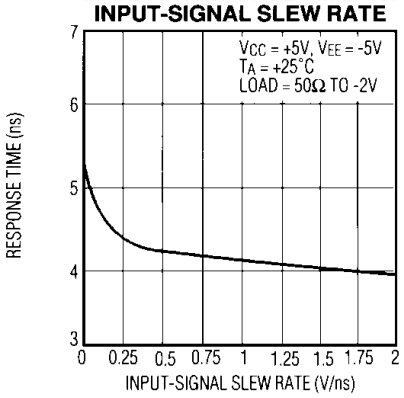
High-Speed, Threshold-Programmable Voltage Comparators

Typical Operating Characteristics (continued)

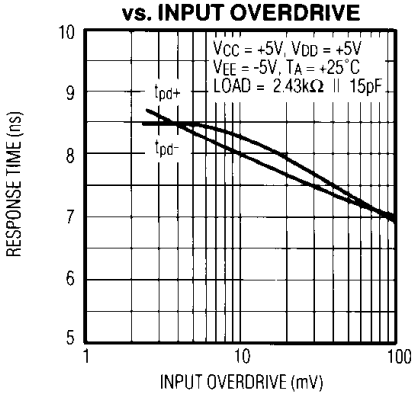
MAX910 RESPONSE TIME vs. INPUT-SIGNAL SLEW RATE



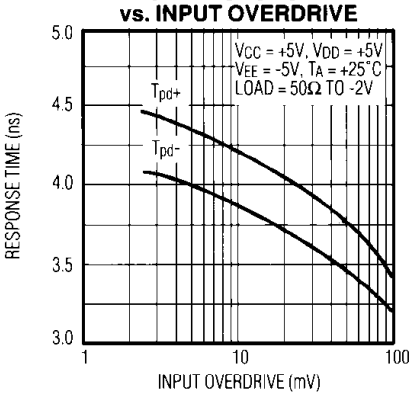
MAX911 RESPONSE TIME vs. INPUT-SIGNAL SLEW RATE



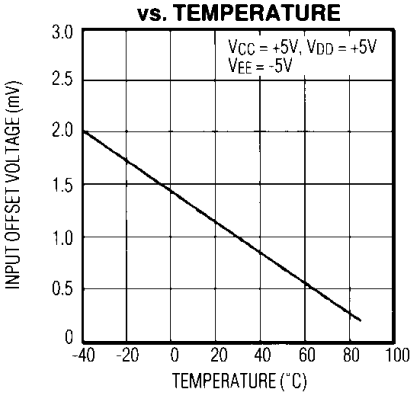
MAX910 RESPONSE TIME vs. INPUT OVERDRIVE



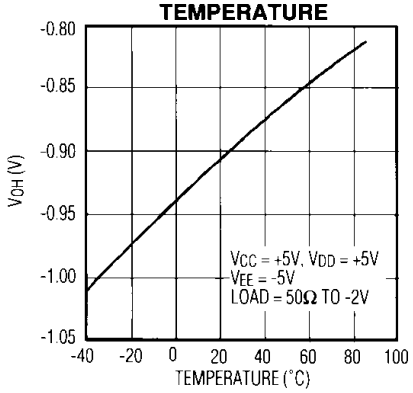
MAX911 RESPONSE TIME vs. INPUT OVERDRIVE



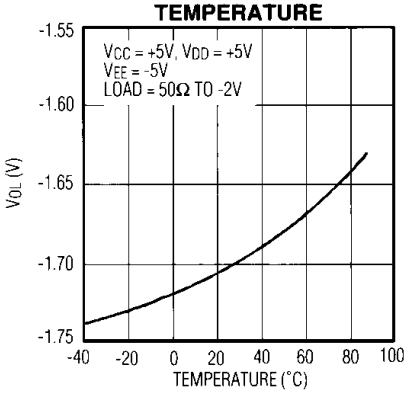
INPUT OFFSET VOLTAGE vs. TEMPERATURE



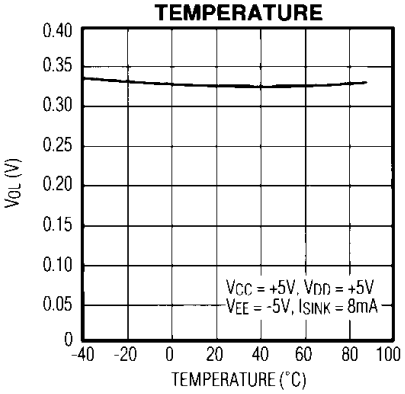
MAX911 OUTPUT HIGH VOLTAGE vs. TEMPERATURE



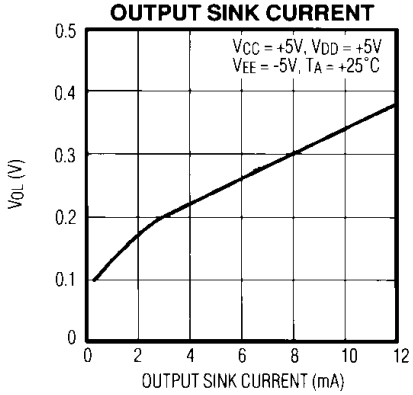
MAX911 OUTPUT LOW VOLTAGE vs. TEMPERATURE



MAX910 OUTPUT LOW VOLTAGE vs. TEMPERATURE

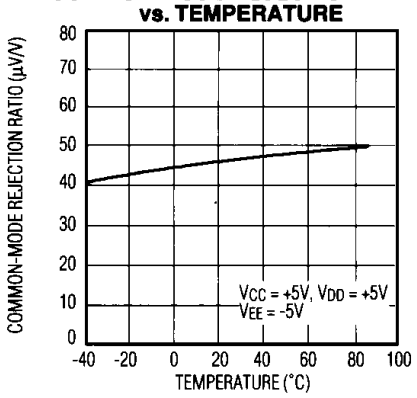


MAX910 OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT

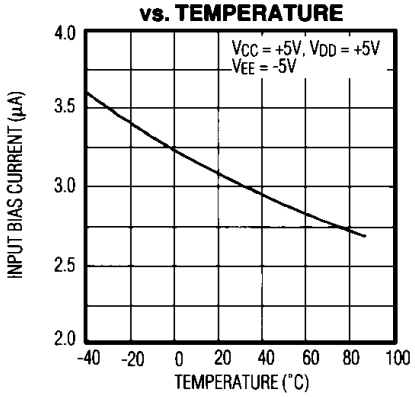


Typical Operating Characteristics (continued)

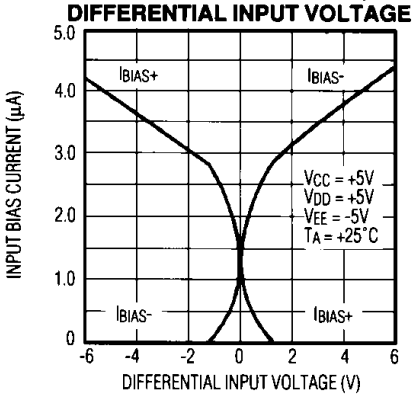
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



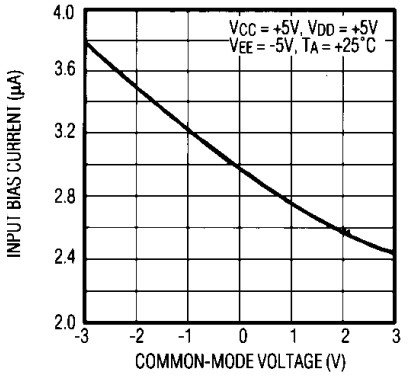
INPUT BIAS CURRENT vs. TEMPERATURE



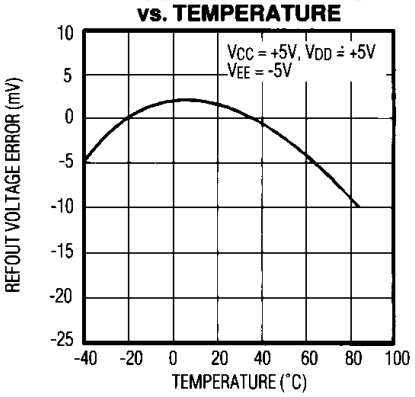
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



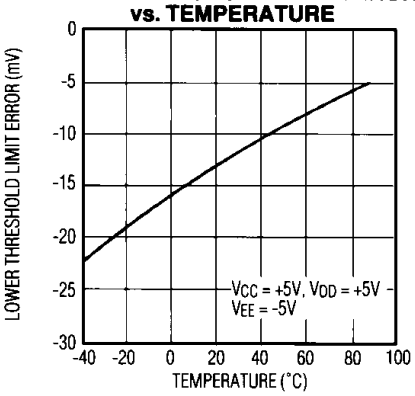
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



REFOUT VOLTAGE ERROR vs. TEMPERATURE



LOWER THRESHOLD LIMIT ERROR vs. TEMPERATURE



High-Speed, Threshold-Programmable Voltage Comparators

Pin Description

MAX910	MAX911	NAME	FUNCTION
1-4, 21-24	1-4 21-24	D4-D7, D0-D3	8-Bit DAC TTL Logic Inputs
5	5	CMP LATCH	Comparator Latch Input. A TTL logic low latches the comparator output. The comparator remains transparent to input changes when driven high or left floating.
6	6	V_{CC}	Analog Positive Supply. Connect to +5V analog supply.
7	7	V_{EE}	Analog Negative Supply. Connect to -5V or -5.2V analog supply.
8	8	REFIN	Reference Input. Connect to REFOUT or External Reference.
9	9	REFOUT	+2.56V Reference Output. Connect to REFIN for V_{TH+} = +2.56V.
10	10	RA	320Ω Span Resistor. Connect to TH OUT for 2.55V threshold range and 10mV resolution.
11	11	RB	640Ω Span Resistor. Connect to TH OUT for 5.1V range with 20mV resolution.
12	12	TH OUT	Threshold Output Voltage. Connect to span resistors RA or RB, and to either comparator input.
13	13	CMP IN+	Comparator Noninverting Input
14	14	CMP IN-	Comparator Inverting Input
15, 20	15, 20	GND	Analog power supply ground; separated from comparator's digital output ground (CMP GND).
16	16	TH CTRL	Reference Trim Input to the 8-bit DAC. Connect to the wiper of a 10kΩ trimming potentiometer between 500kΩ stop resistors for lower threshold output voltage (V_{TH-}) trimming (Figure 1).
17		CMP OUT	TTL Comparator Output
	17	Q OUT	ECL Comparator Output
18	18	CMP GND	Comparator Ground. Connect to digital ground.
19		V_{DD}	Positive Digital Supply. Connect to +5V digital supply.
	19	$\overline{Q}$ OUT	Complementary ECL Comparator Output

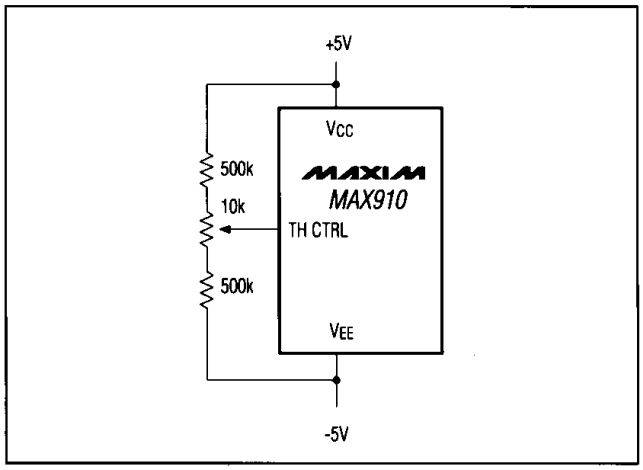


Figure 1. The lower limit of TH OUT is trimmed up to ±50mV, by connecting a 10kΩ trim pot between 500kΩ stop resistors across V_{CC} and V_{EE} with the trim pot wiper to TH CTRL.

Detailed Description

The MAX910 and MAX911 voltage comparators differ in logic compatibility. The MAX910 has a TTL compatible output, while the MAX911 output is fully differential and ECL compatible (Figures 2 and 3). Both comparators have an 8-bit, multiplying-current DAC, internal +2.56V reference, and two span resistors.

The Comparator

The comparator input common-mode range is specified between ±3V to accommodate a wide range of threshold voltages, although either comparator input can be driven to the V_{CC} or V_{EE} power-supply rails without damage. A TTL compatible latch-enable function (CMP LATCH) is supplied on both the MAX910 and MAX911. The comparator is transparent to changes at the input terminals as long as CMP LATCH is driven high or left floating. As soon as CMP LATCH is taken low, the comparator output latches. The output remains latched until CMP LATCH is again driven high or allowed to float.

The MAX910 TTL comparator, with a propagation delay of 8ns and a fan-out of four, drives low-power Schottky TTL gates and 15pF of parasitic board capacitance without significant speed degradation. The MAX911 has 4ns propagation delay, and comparator output specifications that are directly compatible with the MECL 10k series. For best performance, terminate the differential ECL outputs of the MAX911 with 50Ω pull-down resistors to a -2V supply. Both the MAX910 and MAX911 respond to 100MHz signals.

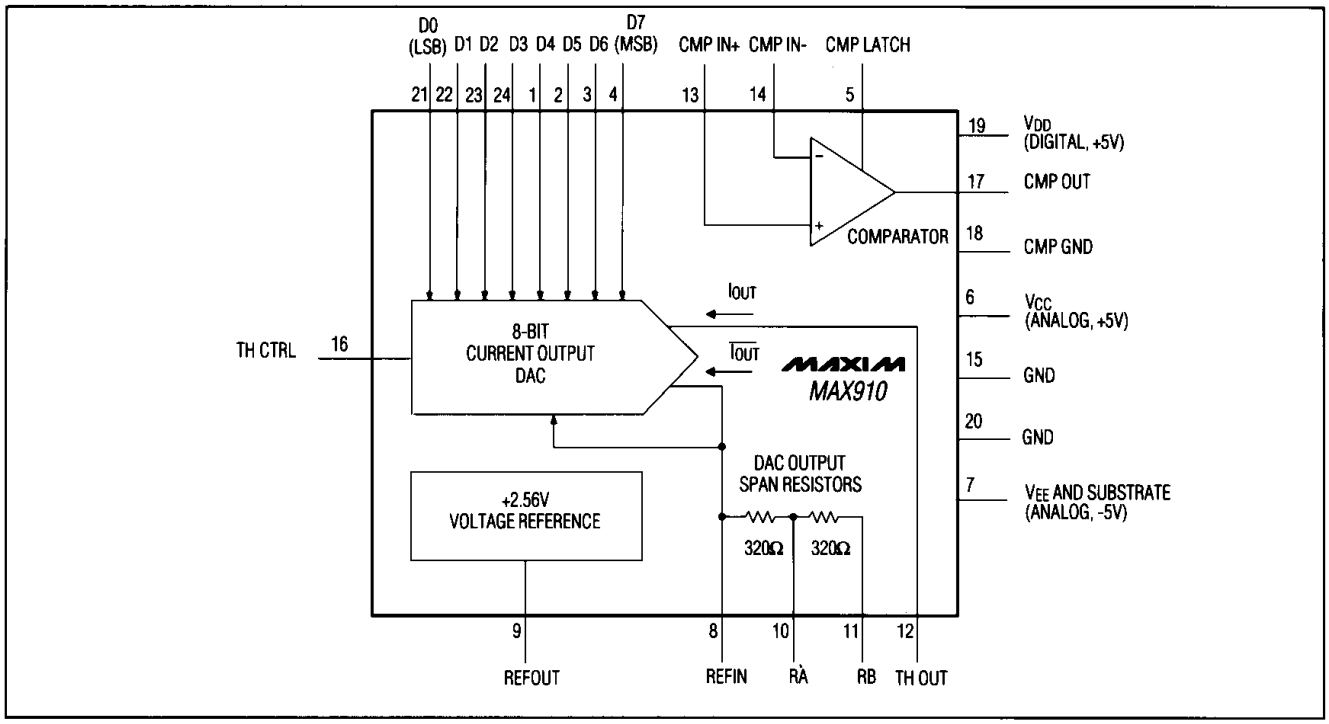


Figure 2. MAX910 Functional Diagram

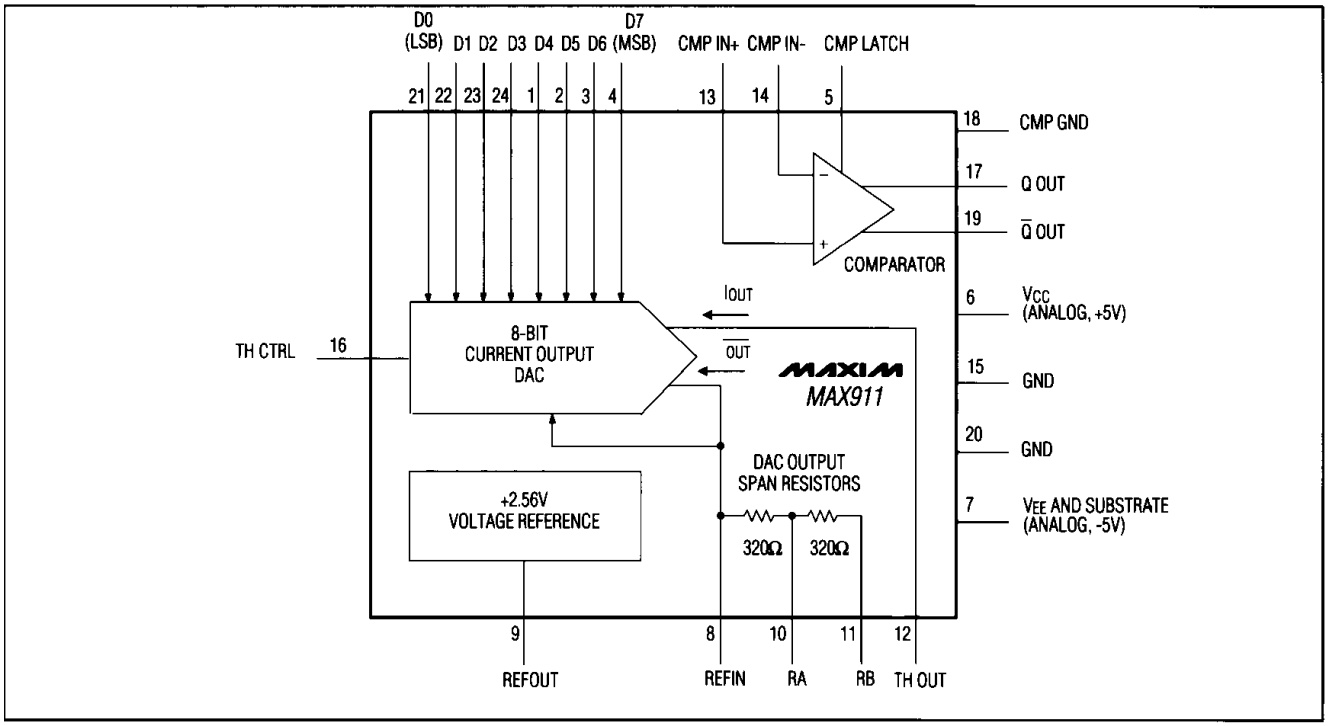


Figure 3. MAX911 Functional Diagram

High-Speed, Threshold-Programmable Voltage Comparators

Threshold Out (TH OUT)

The complementary outputs of the internal 8-bit DAC sink a full-scale output current of 8mA, which translates to either a 2.56V or a 5.12V range, depending on which span resistor input (RA or RB) connects to TH OUT. The digital code divides the output current between the I_{OUT} and $\overline{I_{OUT}}$ DAC outputs (Figures 2 and 3). With the digital input code set to all 0s, TH OUT sinks the full-scale current (less 1LSB) from I_{OUT}, and $\overline{I_{OUT}}$ sinks no current. When the input code is set to all 1s, the reverse is true: REFIN sinks the full-scale output current from $\overline{I_{OUT}}$, and TH OUT sinks no current. Intermediate input codes divide the output current between the two DAC outputs accordingly.

The DAC output current flowing through the DAC output span resistor RA or RB develops the voltage available on TH OUT. Span resistor choice determines the full-scale voltage range and resolution of TH OUT (Table 1). Note that the full-scale output current always flows into REFIN (Pin 8) regardless of the input code. This minimizes glitching on REFIN as the threshold voltage is updated.

Updating the TTL input digital code D0-D7 changes the voltage available on TH OUT.

REFIN must be terminated in a suitable voltage source. Accomplish this by connecting REFIN to REFOUT, or to an external voltage reference. The voltage termination determines the upper end of the threshold range (V_{TH+}). Table 1 lists the range and resolution of TH OUT for different pin connections in Figure 4.

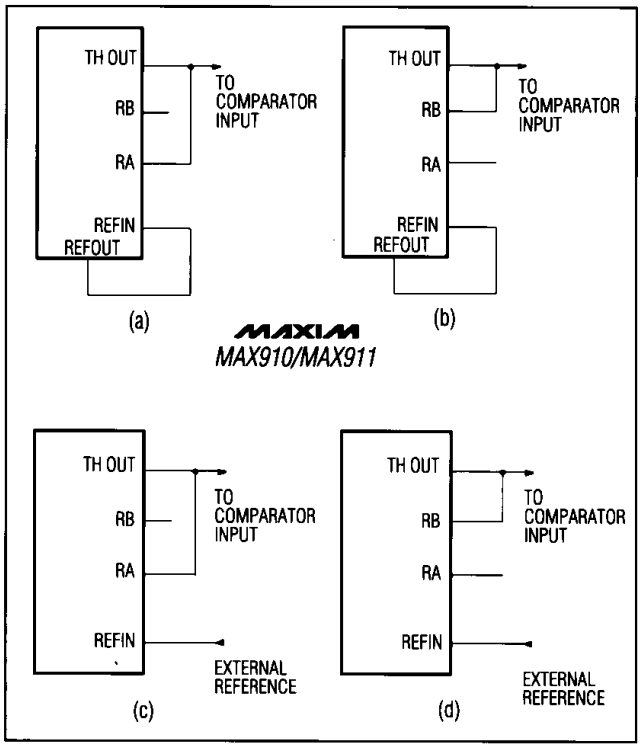


Figure 4. Configuration for the TH OUT Voltage Ranges and Resolutions Listed in Table 1

Using an External Reference

For applications requiring higher precision, connect an external reference to REFIN. The voltage applied at REFIN sets V_{TH-} and V_{TH+}. V_{TH-} and V_{TH+} must not exceed the comparator common-mode input range, and must source at least 10mA.

Choose the external reference and span resistors such that V_{TH-} is at least 2V above V_{EE}. V_{TH-} is determined by REFIN, TH CTRL, and R_{SPAN} (RA, RB):

$$V_{TH-} = V_{REFIN} - \left[\left[\frac{255}{256} \times \frac{R_{SPAN}}{320\Omega} \right] \times [V_{REFIN} - V_{TH\ CTRL}] \right]$$

Where R_{SPAN} = 320Ω when TH OUT is connected to RA;

= 640Ω when TH OUT is connected to RB.

For example, selecting R_{SPAN} = 320Ω and delivering +3V to REFIN yields a 0V to +3V threshold range. TH OUT connects to either comparator input.

Table 1. TH OUT Voltage Range and Resolution

CONNECT REFIN TO:	SPAN RESISTOR (Ω)	V_{TH+}(V)	V_{TH-}(V)	RESOLUTION	PIN CONNECTION
REFOUT (+2.56V)	RA (320)	+2.56	0.01	1LSB = 10mV	Figure 4a
REFOUT (+2.56V)	RB (640)	+2.56	-2.54	1LSB = 20mV	Figure 4b
V_{EXTREF}	RA (320)	V_{EXTREF}	V_{EXTREF} x (1/256)	1LSB = V_{EXTREF}/256	Figure 4c
V_{EXTREF}	RB (640)	V_{EXTREF}	-V_{EXTREF} x (254/256)	1LSB = 2 x V_{EXTREF}/256	Figure 4d

Note: V_{EXTREF} = External Reference Voltage

High-Speed, Threshold-Programmable Voltage Comparators

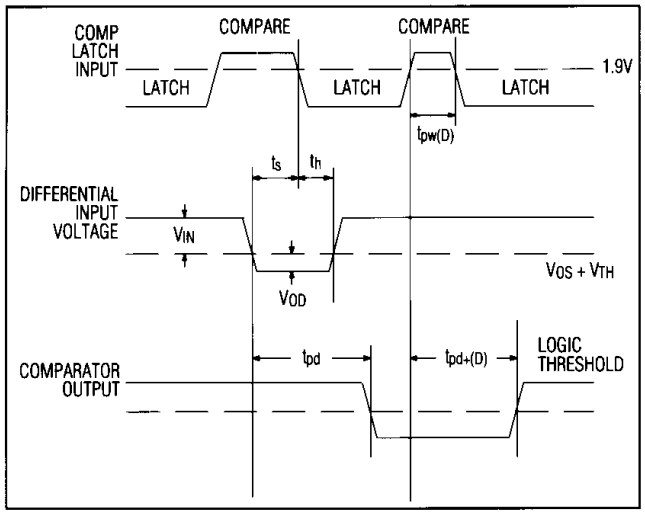


Figure 5. Comparator Timing Diagram

Definition of Terms

V_{OS} **Input Offset Voltage:** That voltage which must be applied between the two comparator input terminals to obtain TTL logic threshold (+1.4V) at the comparator output for the MAX910, or ECL logic threshold (-1.3V) at the comparator output for the MAX911.

V_{IN} **Input Voltage Pulse Amplitude;** usually set to 100mV for comparator specifications.

V_{OD} **Input Voltage Overdrive;** usually set to 5mV and in opposite polarity to V_{IN} for comparator specifications.

t_{pd+} **Input to Output High Delay:** The propagation delay measured from the time the input signal crosses the input offset voltage to the logic threshold of an output low-to-high transition.

t_{pd-} **Input to Output Low Delay:** The propagation delay measured from the time the input signal crosses the input offset voltage to the logic threshold of an output high-to-low transition.

$t_{pd+(D)}$ **Latch Disable to Output High Delay:** The propagation delay measured from the comparator latch signal crossing the TTL threshold in a low-to-high transition, to the point of the output crossing the logic threshold in a low-to-high transition.

$t_{pd-(D)}$ **Latch Disable to Output Low Delay:** The propagation delay measured from the comparator latch signal crossing the TTL threshold in a low-to-high transition, to the point of the output crossing the logic threshold in a high-to-low transition.

t_s **Setup Time:** The time before the comparator latch signal's negative transition that an input must be present to be acquired and held at the output.

t_h **Hold Time:** The time an input signal must remain unchanged after the negative transition of the comparator latch signal in order to be acquired and held at the output.

$t_{pw(D)}$ **Latch-Disable Pulse Width:** The time the comparator latch signal must remain high in order to acquire and hold an input signal change.

$t_{s(VTH)}$ **Threshold Settling Time:** The time required for the threshold voltage to be changed from V_{TH-} to V_{TH+} or from V_{TH+} to V_{TH-} and settle to within ±1/2LSB of V_{TH+} or V_{TH-}.

High-Speed, Threshold-Programmable Voltage Comparators

Applications Information

Board Layout

A printed circuit board with a good, low inductance ground plane is mandatory. Connect analog GND to the ground plane as close to the device as possible. The comparator ground (CMP GND) must be connected to the digital ground plane or bus. Connect the two grounds together at the power supply. Place all decoupling capacitors (small 100nF ceramic type are a good choice) as close as possible to the device power-supply pins. The power return side should be short and straight to the ground plane. Separate positive supplies for analog (V_{CC}) and digital (V_{DD}) are also recommended. Choose decoupling and terminating components with suitable bandwidths.

To avoid unwanted parasitic feedback, keep the comparator input and output trace and lead lengths short. Separate the digital lines driving D0-D7 as far from the analog lines as possible. Solder the device directly to the printed circuit board rather than using a socket to minimize stray capacitance.

Minimize parasitic capacitance between TH OUT, RA, RB, and CMP IN by keeping the connections short. Parasitic capacitance on this node degrades threshold voltage settling time.

Typical Application Circuits

Adding Hysteresis to the MAX910

For applications requiring fast response to slow-moving inputs, add hysteresis by connecting a resistor from CMP OUT to TH OUT (Figure 6).

$$\text{Hysteresis} = \frac{V_{OH} - V_{OL}}{1 + \frac{R_{FB}}{R_{SPAN}}}$$

where V_{OH} = Comparator Output Threshold High

V_{OL} = Comparator Output Threshold Low

R_{FB} = Feedback Resistor

R_{SPAN} = 320Ω with TH OUT connected to RA

= 640Ω with TH OUT connected to RB

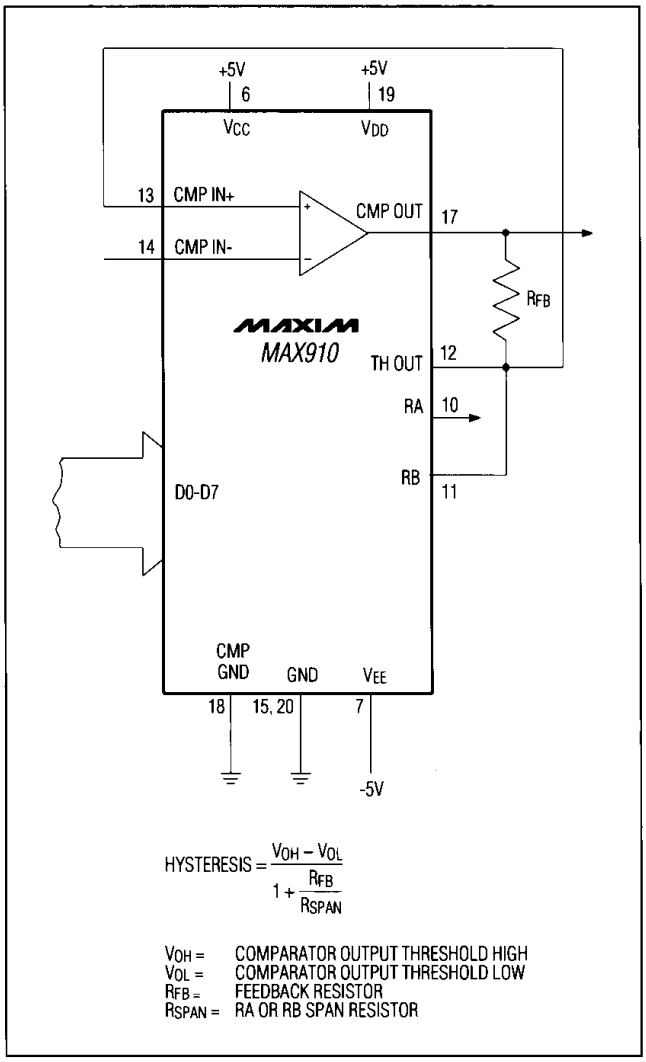


Figure 6. Adding Hysteresis to the MAX910

Window Comparator Circuit

Two MAX911s detect the upper and lower threshold limits of a logic output from a device under test (DUT) in an automatic test equipment application (Figure 7). One device is programmed for the upper threshold limit while the other detects the lower limit. Either the MAX910 or MAX911 may be used in this application depending on the propagation delay and output compatibility requirements.

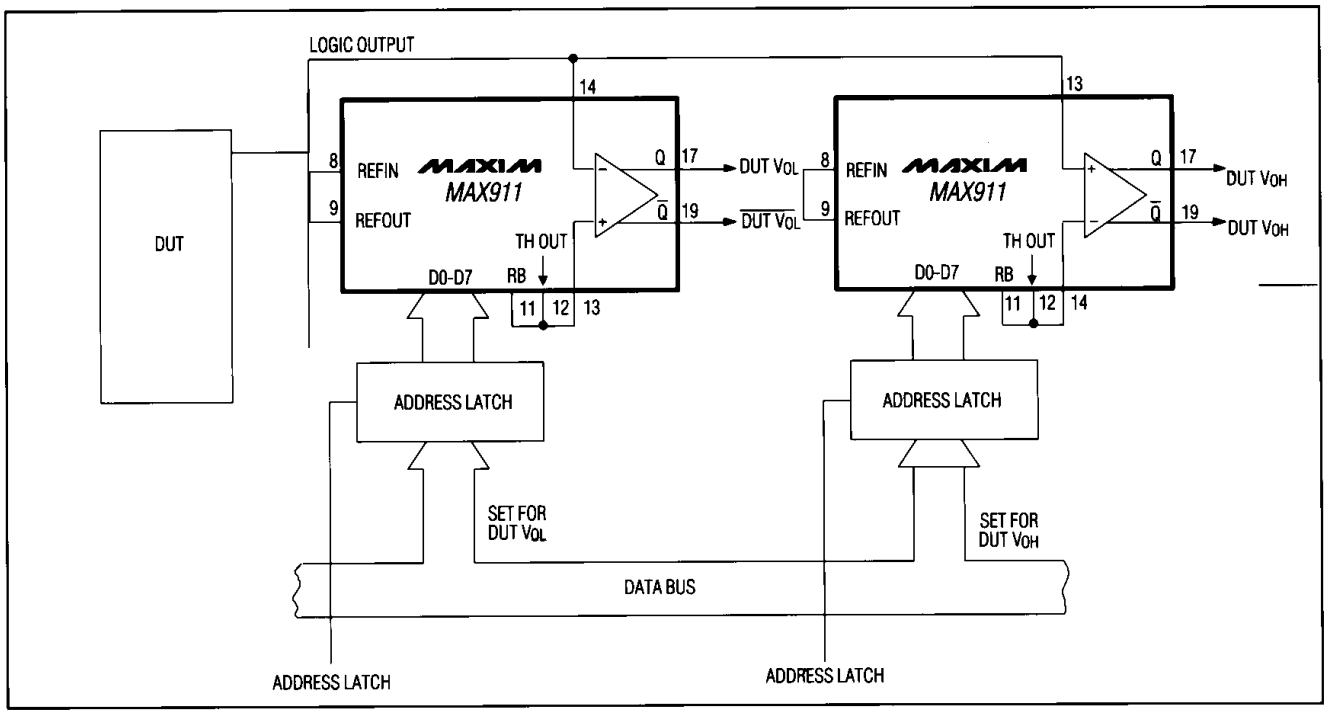
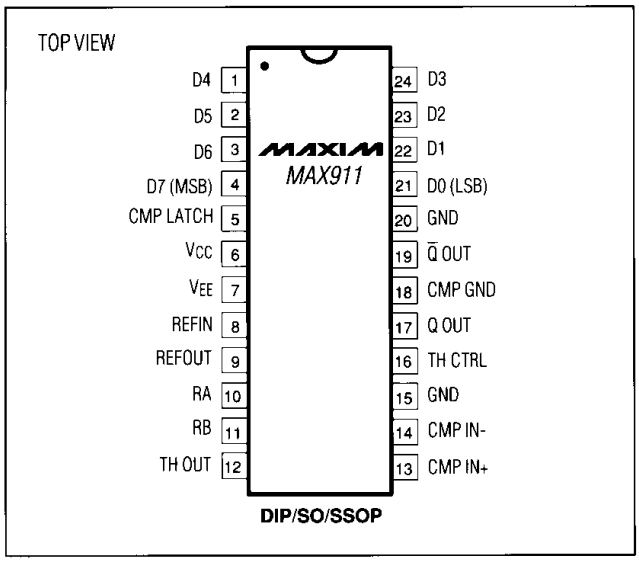


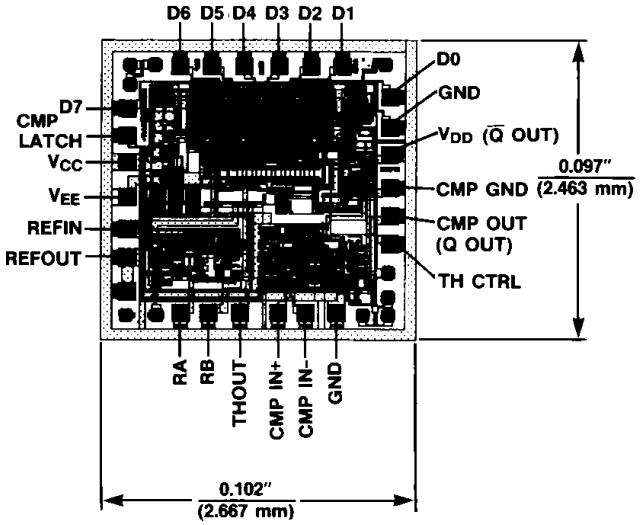
Figure 7. Automatic Test Equipment Logic Threshold Detector

High-Speed, Threshold-Programmable Voltage Comparators

Pin Configurations (continued)



Chip Topography



( ) ARE FOR MAX911 ONLY.
SUBSTRATE CONNECTED TO V_{EE}.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX911CAG	0°C to +70°C	24 SSOP**
MAX911CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX911CWG	0°C to +70°C	24 Wide SO
MAX911C/D	0°C to +70°C	Dice*

* *Dice are specified at T_A = +25°C, DC parameters only.*
** *Contact factory for pricing and availability.*

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