2-MHz 600-mA Step-Down DC-DC Converter With Mode Control

Check for Samples: LM3676

FEATURES

- **16µA Typical Quiescent Current**
- **600mA Maximum Load Capability**
- **2MHz Typical PWM Fixed Switching Frequency**
- **Automatic PFM/PWM Mode Switching or Forced PWM Mode**
- **Available in Fixed Output Voltages and Adjustable Version**
- **8-Lead Non-Pullback WSON Package**
- **Internal Synchronous Rectification for High Efficiency**
- **Internal Soft Start**
- **0.01µA Typical Shutdown Current**
- **Operates From a Single Li-Ion Cell Battery**
- **Only Three Tiny Surface-Mount External Components Required (One Inductor, Two Ceramic Capacitors)**
- **Current Overload and Thermal Shutdown Protection**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **MP3 Players**
- **WLAN**
- **Portable Instruments**
- **Digital Still Cameras**
- **Portable Hard Disk Drives**

DESCRIPTION

The LM3676 step-down DC-DC converter is optimized for powering low voltage circuits from a single Li-Ion cell battery and input voltage rails from 2.9V to 5.5V. It provides up to 600mA load current, over the entire input voltage range. There are several different fixed voltage output options available as well as an adjustable output voltage version.

The LM3676 has a mode-control pin that allows the user to select continuous Pulse Width Modulation (PWM) mode over the complete load range or an intelligent PFM-PWM mode that changes modes depending on the load. PWM mode offers superior efficiency under high load conditions (>100mA) and the lowest output noise performance. In Auto mode, PFM-PWM, hysteretic PFM extends the battery life through reduction of the quiescent current to 16µA (typ.) during light loads and system standby.

The LM3676 is available in a 8-lead non-pullback WSON package in leaded (PB) and lead-free (NO PB) versions. A high switching frequency of 2 MHz (typ) allows use of tiny surface-mount components, an inductor and two ceramic capacitors.

TYPICAL APPLICATION CIRCUITS

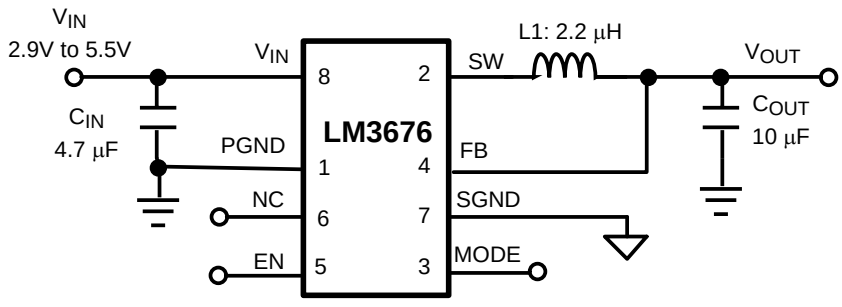


Figure 1. Typical Application Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

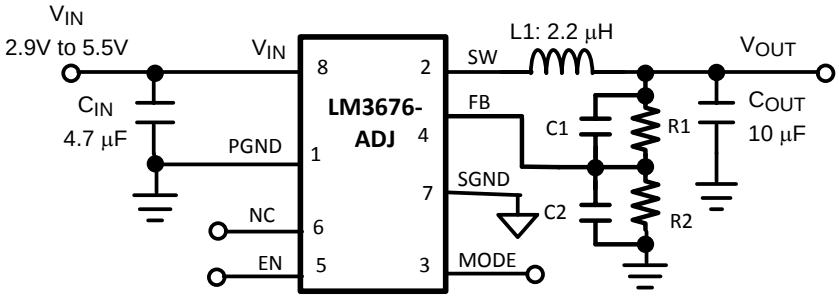


Figure 2. Typical Application Circuit for ADJ Version

PIN DIAGRAM

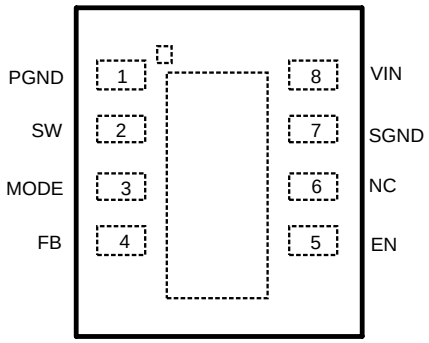


Figure 3. Top View
WSON-8 Package
Package Number NGQ0008A

PIN DESCRIPTIONS (8-Lead WSON)

Pin No.	Name	Description
1	PGND	Power Ground Pin.
2	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
3	MODE	Mode Control Pin: > 1.0V selects continuous PWM mode ; <0.4V selects Auto (PFM-PWM) mode. Do not leave this pin floating.
4	FB	Feedback analog input. Connect directly to the output filter capacitor for fixed voltage versions. For adjustable version external resistor dividers are required (see Figure 2). The internal resistor dividers are disabled for the adjustable version.
5	EN	Enable pin. The device is in shutdown mode when voltage to this pin is <0.4V and enabled when >1.0V. Do not leave this pin floating.
6	NC	Not Connected. Leave Pin Floating. Do Not Connect to other pins
7	SGND	Signal Ground Pin.
8	VIN	Power Supply input. Connect to the input filter capacitor (see Figure 1).

ORDERING INFORMATION[1][2]

LM3676 (8-Lead WSON)	
Ordering Information	**Voltage Option (V)**
LM3676SD-1.5	1.5
LM3676SDX-1.5	
LM3676SD-1.5/NOPB	
LM3676SDX-1.5/NOPB	
LM3676SD-1.8	1.8
LM3676SDX-1.8	
LM3676SD-1.8/NOPB	
LM3676SDX-1.8/NOPB	
LM3676SD-3.3	3.3
LM3676SDX-3.3	
LM3676SD-3.3/NOPB	
LM3676SDX-3.3/NOPB	
LM3676SD-ADJ	Adjustable
LM3676SDX-ADJ	
LM3676SD-ADJ/NOPB	
LM3676SDX-ADJ/NOPB	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Absolute Maximum Ratings[1][2]

V_{IN} Pin: Voltage to GND		−0.2V to 6.0V
FB, SW, EN, Mode Pin:		(GND−0.2V) to (V_{IN} + 0.2V)
Continuous Power Dissipation [3]		Internally Limited
Junction Temperature (T_{J-MAX})		+125°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec.)		260°C
ESD Rating [4]	Human Body Model	2 kV
	Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings may not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 150°C (typ.) and disengages at T_J= 130°C (typ.).
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1) (2)

Input Voltage Range	2.9V to 5.5V
Recommended Load Current	0mA to 600 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings may not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In Applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX}), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction to ambient thermal resistance of the package (θ_{JA}) in the application, as given by the following equation: $T_{A-MAX} = T_{J-MAX} - (\theta_{JA} \times P_{D-MAX})$. Refer to Dissipation rating table for P_{D-MAX} values at different ambient temperatures.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) for 4 layer board (1)	56°C/W

(1) Junction to ambient thermal resistance (θ_{JA}) is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design. Specified value of 130 °C/W for WSON is based on a 4 layer, 4" x 3", 2/1/1/2 oz. Cu board as per JEDEC standards is used.

Electrical Characteristics (1) (2) (3)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the full operating junction temperature range (−30°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LM3676SD with V_{IN} = 3.6V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{FB}	Feedback Voltage (Fixed / Adj) (4)		**-4**		**+4**	%
	Line Regulation	2.9V ≤ V_{IN} ≤ 5.5V I_O = 10 mA		0.031		%/V
	Load Regulation	100 mA ≤ I_O ≤ 600 mA V_{IN}= 3.6V		0.0013		%/mA
V_{REF}	Internal Reference Voltage			0.5		V
I_{SHDN}	Shutdown Supply Current	EN = 0V		0.01	**2**	µA
I_Q	DC Bias Current into V_{IN}	No load, device is not switching (FB forced higher than programmed output voltage)		16	**35**	µA
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET			380	500	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for NFET			250	400	mΩ
I_{LIM}	Switch Peak Current Limit (5)	Open Loop	**830**	1020	**1200**	mA
V_{IH}	Logic High Input for EN and Mode Pin		**1.0**			V
V_{IL}	Logic Low Input for EN and Mode Pin				**0.4**	V
I_{EN}	Enable (EN) Input Current			0.01	**1**	µA
I_{Mode}	Mode Pin Input Current			0.01	**1**	µA
F_{OSC}	Internal Oscillator Frequency	PWM Mode	**1.6**	2	**2.6**	MHz

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers represent the most likely norm.
(3) The parameters in the electrical characteristic table are tested at V_{IN}= 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) Test condition: for V_{OUT} less than 2.5V, V_{IN} = 3.6V; for V_{OUT} greater than or equal to 2.5V, $V_{IN} = V_{OUT}$ + 1V.
(5) Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Electrical Characteristic table reflects open loop data (FB=0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

Dissipation Ratings

θ_{JA}	$T_A \leq$ 25°C Power Rating	T_A= 60°C Power Rating	T_A= 85°C Power Rating
56°C/W (4 layer board) 8 Lead non-pullback WSON package	1.78W	1.16W	714mW

BLOCK DIAGRAM

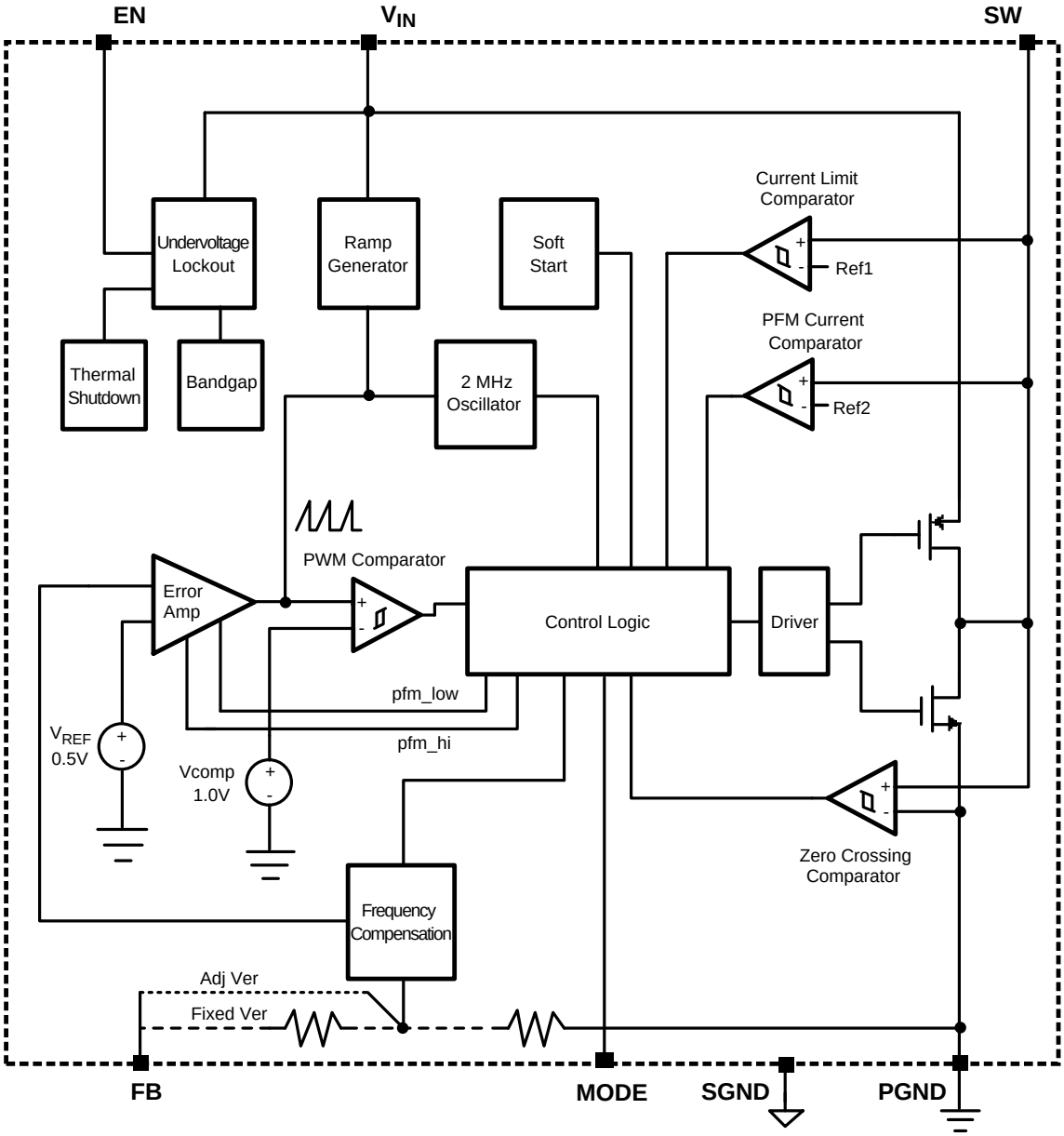


Figure 4. Simplified Functional Diagram

Typical Performance Characteristics

Circuit of LM3676, V_{IN}= 3.6V, V_{OUT}= 1.5V, T_A= 25°C, unless otherwise noted.

Quiescent Supply Current vs. Supply Voltage

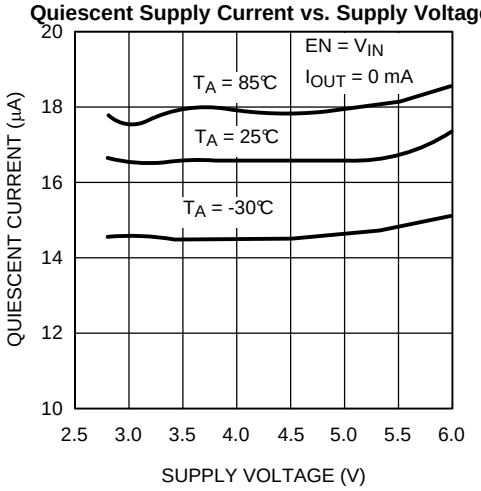


Figure 5.

Shutdown Current vs. Temp

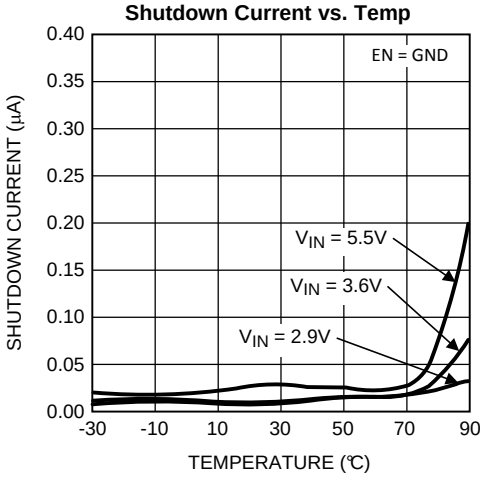


Figure 6.

Feedback Bias Current vs. Temp

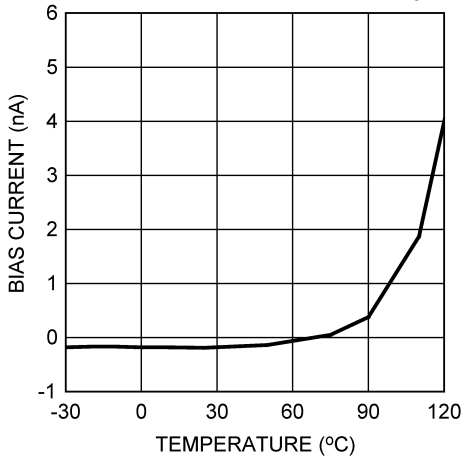


Figure 7.

Switching Frequency vs. Temperature

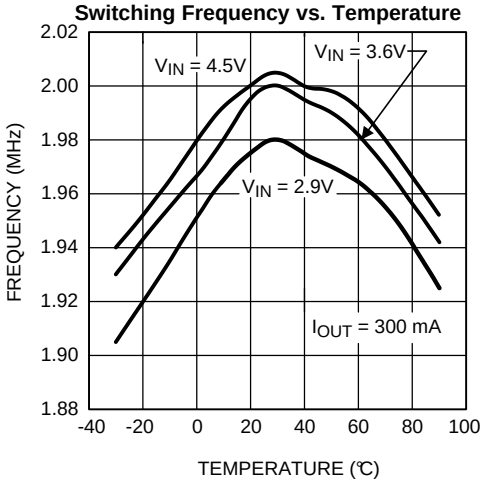


Figure 8.

$R_{DS(ON)}$ vs. Temperature

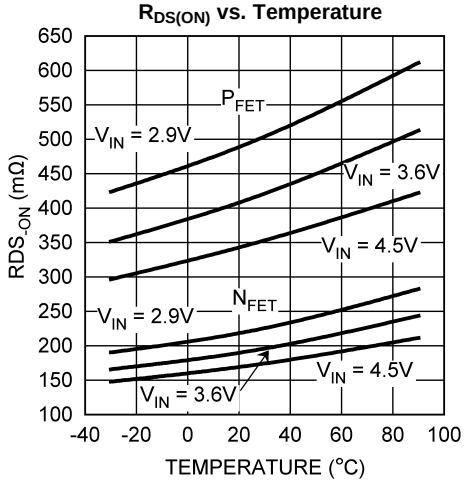


Figure 9.

Open/Closed Loop Current Limit vs. Temperature

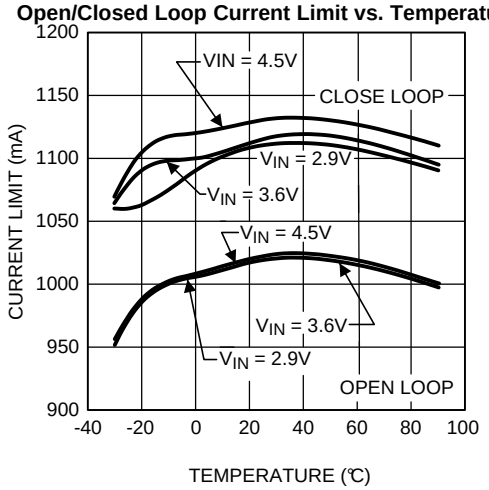


Figure 10.

Typical Performance Characteristics (continued)

Circuit of LM3676, V_{IN}= 3.6V, V_{OUT}= 1.5V, T_A= 25°C, unless otherwise noted.

Output Voltage vs. Supply Voltage (V_{OUT} = 1.5V)

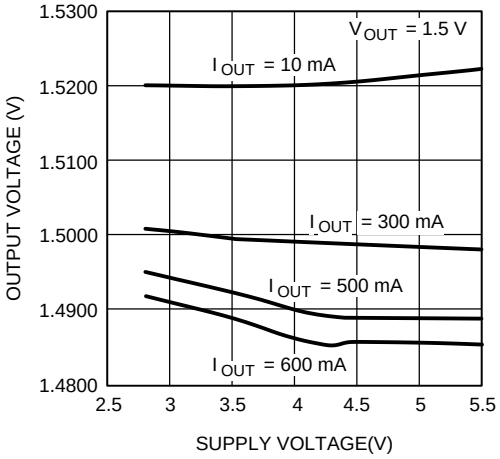


Figure 11.

Output Voltage vs. Temperature (V_{OUT} = 1.5V)

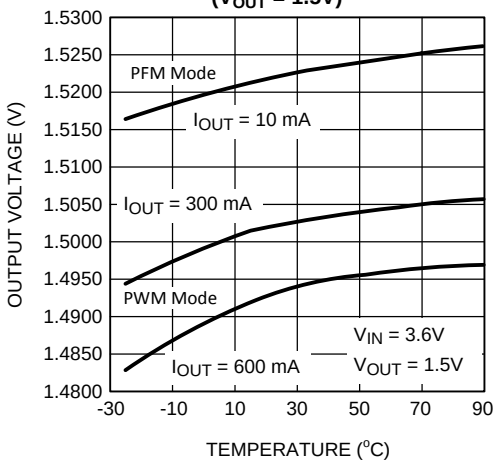


Figure 12.

Output Voltage vs. Output Current (V_{OUT} = 1.5V)

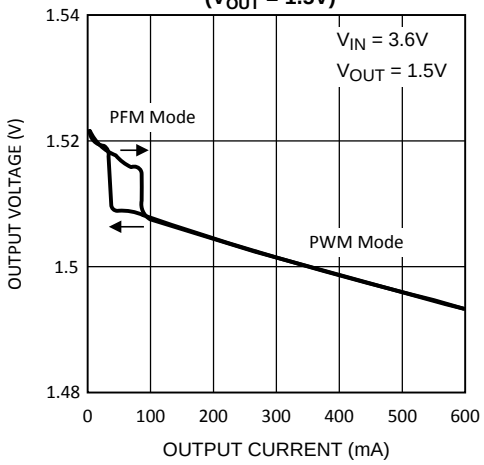


Figure 13.

Line Transient Response V_{OUT} = 1.5V (PWM Mode)

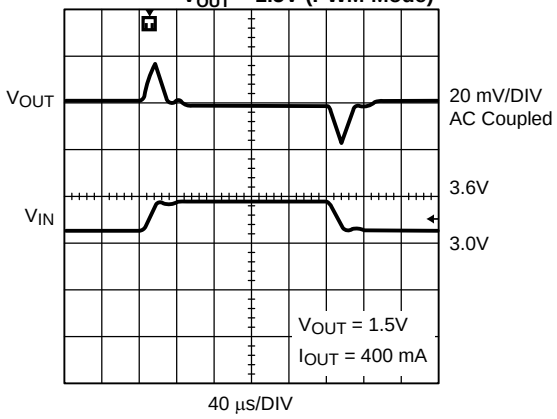


Figure 14.

Efficiency vs. Output Current (V_{OUT} = 1.5V, L = 2.2 µH)

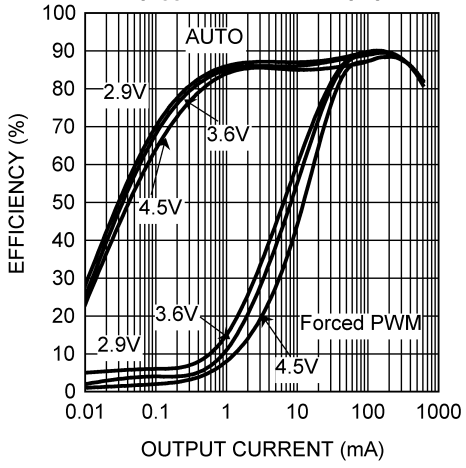


Figure 15.

Efficiency vs. Output Current (V_{OUT} = 3.3V, L = 2.2 µH)

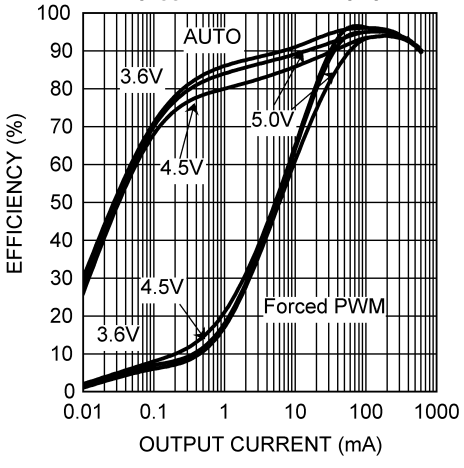


Figure 16.

Typical Performance Characteristics (continued)

Circuit of LM3676, V_{IN}= 3.6V, V_{OUT}= 1.5V, T_A= 25°C, unless otherwise noted.

Load Transient Response (V_{OUT} = 1.5V)
(PFM Mode 0.5mA to 50mA)

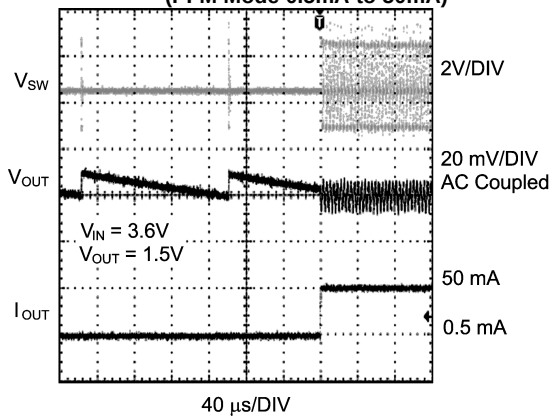


Figure 17.

Load Transient Response (V_{OUT} = 1.5V)
(PFM Mode 50mA to 0.5mA)

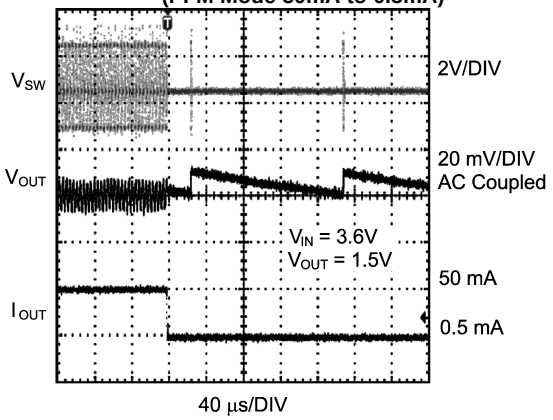


Figure 18.

Mode Change by Load Transients
V_{OUT} = 1.5V (PFM to PWM)

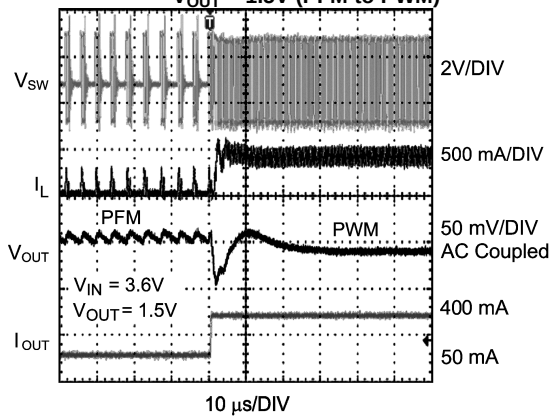


Figure 19.

Mode Change by Load Transients
V_{OUT} = 1.5V (PWM to PFM)

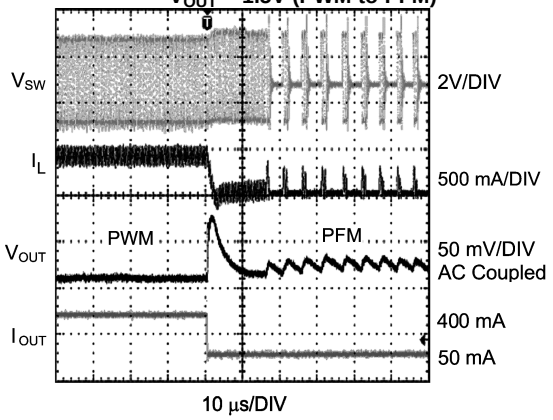


Figure 20.

Mode Change by Mode Pin
V_{OUT} = 1.5V (PFM to PWM)

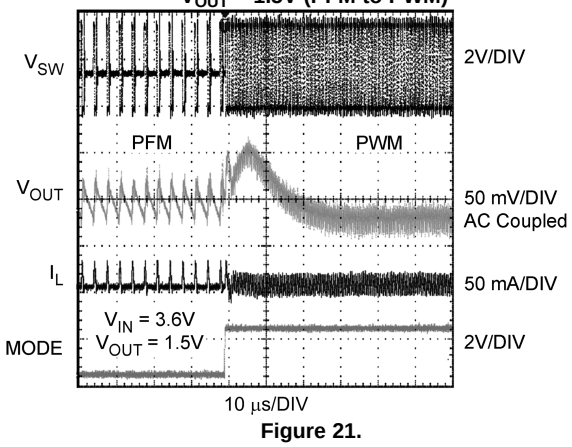


Figure 21.

Mode Change by Mode Pin
V_{OUT} = 1.5V (PWM to PFM)

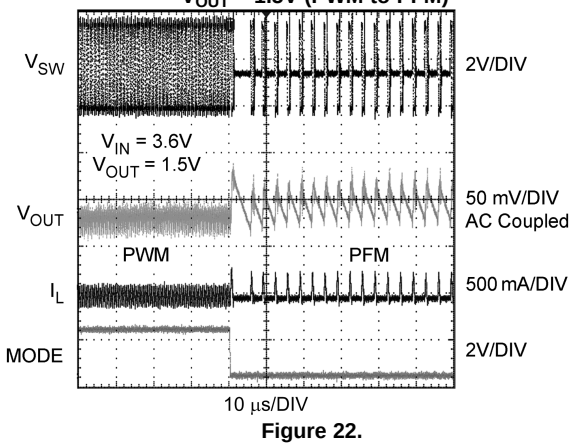


Figure 22.

Typical Performance Characteristics (continued)

Circuit of LM3676, V_{IN}= 3.6V, V_{OUT}= 1.5V, T_A= 25°C, unless otherwise noted.

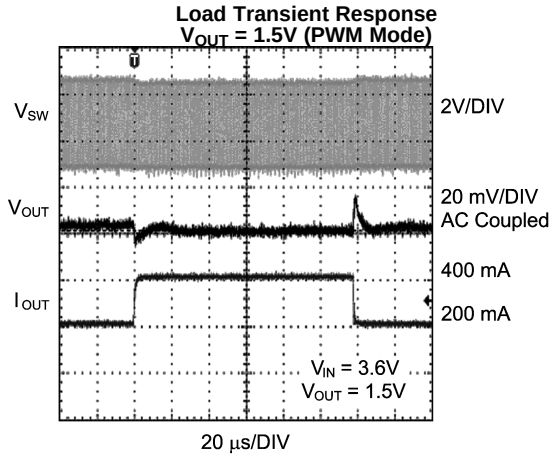


Figure 23.

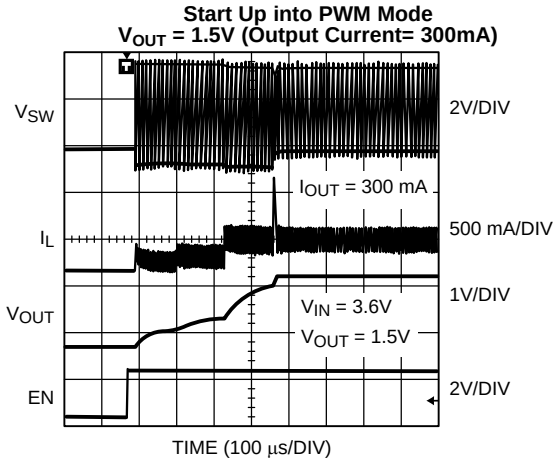


Figure 24.

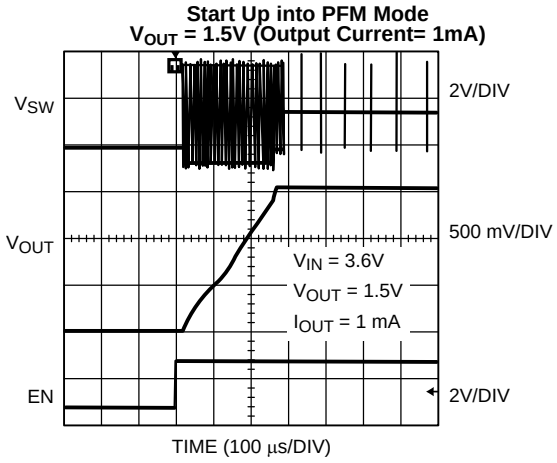


Figure 25.

OPERATION DESCRIPTION

DEVICE INFORMATION

The LM3676, a high efficiency step down DC-DC switching buck converter, delivers a constant voltage from a single Li-Ion battery and input voltage rails from 2.9V to 5.5V to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3676 has the ability to deliver up to 600 mA depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

There are three modes of operation depending on the current required and Mode pin - PWM (Pulse Width Modulation), PFM (Pulse Frequency Modulation), and shutdown. The device operates in PWM mode if the load current > 80 mA or when the Mode pin is set high. When the mode pin is set low, Auto mode, lighter load current causes the device to automatically switch into PFM for reduced current consumption (I_Q = 16 µA typ) and prolong battery life . Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.01 µA typ).

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection. As shown in Figure 1, only three external power components are required for implementation.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage is 2.9V or higher.

CIRCUIT OPERATION

During the first portion of each switching cycle, the control block in the LM3676 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{IN}–V_{OUT})/L, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of - V_{OUT}/L.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

MODE PIN

Setting the Mode pin low (<0.4V) places the LM3676 in Auto mode. During Auto mode the device automatically switches between PFM-PWM depending on the load. Setting Mode high (>1.0V) places the part in Forced PWM. The part is in forced PWM regardless of the load. Do not leave the Mode pin floating.

PWM OPERATION

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

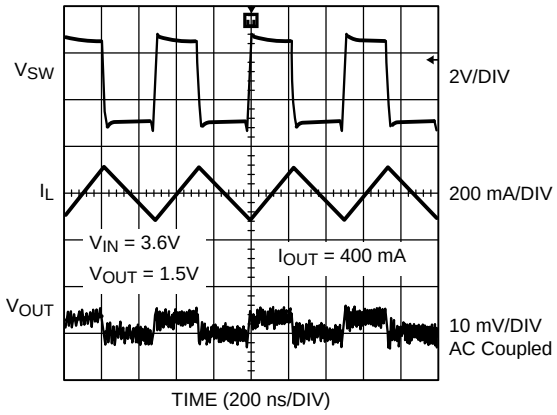


Figure 26. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, the LM3676 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the LM3676 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1020 mA (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold. This allows the inductor current more time to decay, thereby preventing runaway.

PFM OPERATION

At very light load, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A. The NFET current reaches zero.

B. The peak PMOS switch current drops below the I_{MODE} level, (Typically I_{MODE} < 30mA + V_{IN}/42 Ω).

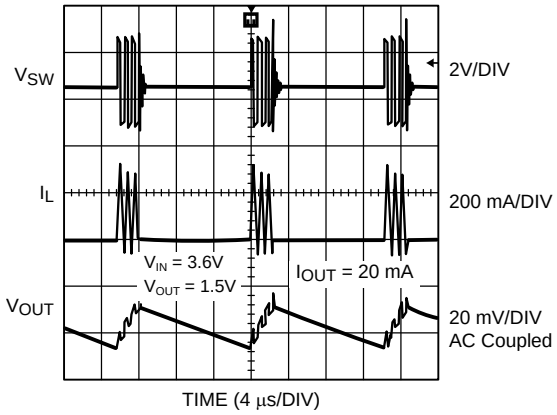


Figure 27. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between ~0.6% and ~1.7% above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 112mA + V_{IN}/27Ω .

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 28), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 16µA (typ), which allows the part to achieve high efficiency under extremely light load conditions.

If the load current should increase during PFM mode (see Figure 28) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode. When V_{IN} =2.9V the part transitions from PWM to PFM mode at ~35mA output current and from PFM to PWM mode at ~85mA , when V_{IN}=3.6V, PWM to PFM transition happens at ~50mA and PFM to PWM transition happens at ~100mA, when V_{IN} =4.5V, PWM to PFM transition happens at ~65mA and PFM to PWM transition happens at ~115mA.

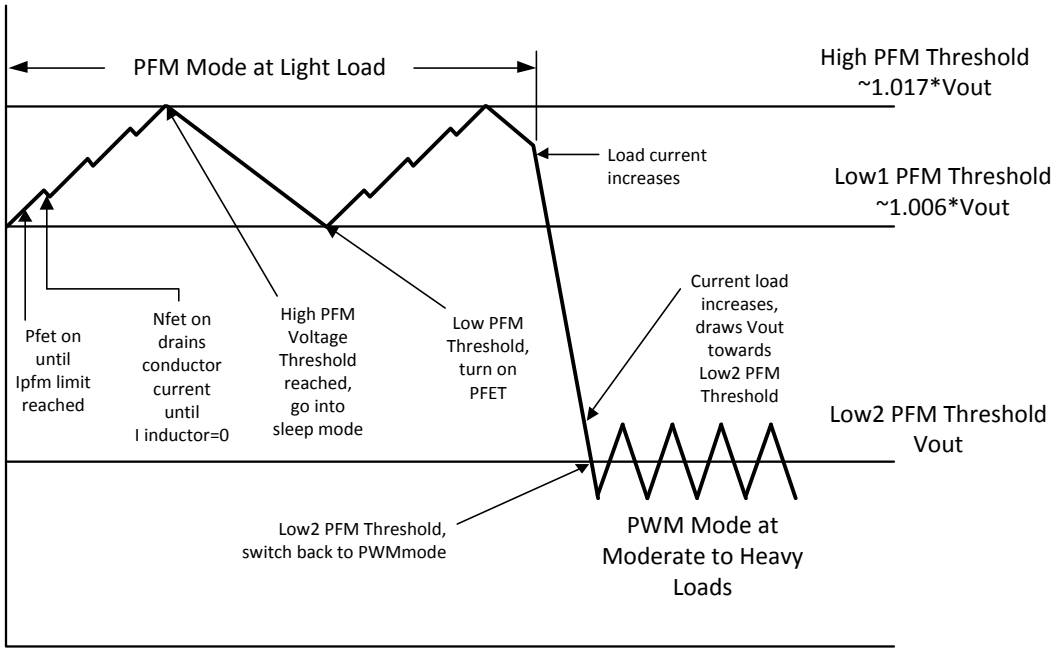


Figure 28. Operation in PFM Mode and Transfer to PWM Mode

SHUTDOWN MODE

Setting the EN input pin low (<0.4V) places the LM3676 in shutdown mode. During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the LM3676 are turned off. Setting EN high (>1.0V) enables normal operation. It is recommended to set EN pin low to turn off the LM3676 during system power up and undervoltage conditions when the supply is less than 2.9V. Do not leave the EN pin floating.

SOFT START

The LM3676 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after Vin reaches 2.9V. Soft start is implemented by increasing switch current limit in steps of 70mA, 140mA, 280mA and 1020mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with a 10µF output capacitor and 300mA load is 400µs and with 1mA load is 275µs.

LDO - LOW DROP OUT OPERATION

The LM3676-ADJ can operate at 100% duty cycle (no switching; PMOS switch completely on) for low drop out support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV.

The minimum input voltage needed to support the output voltage is

$V_{IN,\ MIN} = I_{LOAD} * (R_{DSON\ (P)} + R_{INDUCTOR}) + V_{OUT}$

I_{LOAD} = Load current

$R_{DSON\ (P)}$ = Drain to source resistance of PFET switch in the triode region

$R_{INDUCTOR}$ = Inductor resistance

APPLICATION INFORMATION

OUTPUT VOLTAGE SELECTION FOR LM3676-ADJ

The output voltage of the adjustable parts can be programmed through the resistor network connected from V_{OUT} to FB, then to GND. V_{OUT} is adjusted to make the voltage at FB equal to 0.5V. The resistor from FB to GND (R2) should be 200 kΩ to keep the current drawn through this network well below the 16 µA quiescent current level (PFM mode) but large enough that it is not susceptible to noise. If R2 is 200 kΩ, and V_{FB} is 0.5V, the current through the resistor feedback network will be 2.5 µA. The output voltage of the adjustable parts ranges from 1.1V to 3.3V.

The formula for output voltage selection is:

$$V_{OUT} = V_{FB} * \left(1 + \frac{R1}{R2}\right) \quad (1)$$

- V_{OUT}: output voltage (volts)
- V_{FB} : feedback voltage = 0.5V
- R1: feedback resistor from V_{OUT} to FB
- R2: feedback resistor from FB to GND

For any output voltage greater than or equal to 1.1V, a zero must be added around 45 kHz for stability. The formula for calculation of C1 is:

$$C1 = \frac{1}{(2 * \pi * R1 * 45\ kHz)} \quad (2)$$

For output voltages higher than 2.5V, a pole must be placed at 45 kHz as well. If the pole and zero are at the same frequency the formula for calculation of C2 is:

$$C2 = \frac{1}{(2 * \pi * R2 * 45\ kHz)} \quad (3)$$

The formula for location of zero and pole frequency created by adding C1 and C2 is given below. By adding C1, a zero as well as a higher frequency pole is introduced.

$$Fz = \frac{1}{(2 * \pi * R1 * C1)} \quad (4)$$

$$Fp = \frac{1}{2 * \pi * (R1 \| R2) * (C1+C2)} \quad (5)$$

See Table 1.

Table 1. LM3676-ADJ Configurations For Various V_{OUT} (Circuit of Figure 2)

V_{OUT}(V)	R1(kΩ)	R2 (kΩ)	C1 (pF)	C2 (pF)	L (µH)	C_{IN} (µF)	C_{OUT}(µF)
1.1	240	200	15	none	2.2	4.7	10
1.2	280	200	12	none	2.2	4.7	10
1.3	320	200	12	none	2.2	4.7	10
1.5	357	178	10	none	2.2	4.7	10
1.6	442	200	8.2	none	2.2	4.7	10
1.7	432	178	8.2	none	2.2	4.7	10
1.8	464	178	8.2	none	2.2	4.7	10
1.875	523	191	6.8	none	2.2	4.7	10
2.5	402	100	8.2	none	2.2	4.7	10
2.8	464	100	8.2	33	2.2	4.7	10
3.3	562	100	6.8	33	2.2	4.7	10

INDUCTOR SELECTION

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. **The minimum value of inductance to ensure good performance is 1.76µH at I_{LIM} (typ) dc current over the ambient temperature range.** Shielded inductors radiate less noise and should be preferred.

There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right) \quad (6)$$

- I_{RIPPLE}: average to peak inductor current
- I_{OUTMAX}: maximum load current (600mA)
- V_{IN}: maximum input voltage in application
- L : min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f : minimum switching frequency (1.6Mhz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 1200mA.

A 2.2 µH inductor with a saturation current rating of at least 1200 mA is recommended for most applications.The inductor's resistance should be less than 0.3Ω for good efficiency. Table 2 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

Table 2. Suggested Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	D.C.R (max)
DO3314-222MX	Coilcraft	3.3 x 3.3 x 1.4	200 mΩ
LPO3310-222MX	Coilcraft	3.3 x 3.3 x 1.0	150 mΩ
ELL5GM2R2N	Panasonic	5.2 x 5.2 x 1.5	53 mΩ
CDRH2D14-2R2	Sumida	3.2 x 3.2 x 1.55	94 mΩ

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 4.7 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. **The minimum input capacitance to ensure good performance is 2.2µF at 3V dc bias; 1.5µF at 5V dc bias including tolerances and over ambient temperature range.** The input filter capacitor supplies current to the PFET switch of the LM3676 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

The worst case is when $V_{IN} = 2 * V_{OUT}$ (7)

OUTPUT CAPACITOR SELECTION

A ceramic output capacitor of 10 µF, 6.3V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The minimum output capacitance to ensure good performance is 5.75µF at 1.8V dc bias including tolerances and over ambient temperature range. The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and by the R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follow:

$$V_{PP-C} = \frac{I_{RIPPLE}}{4*f*C} \quad (8)$$

Voltage peak-to-peak ripple due to ESR can be expressed as follow:

$V_{PP-ESR} = (2 * I_{RIPPLE}) * R_{ESR}$

Because these two components are out of phase the rms (root mean squared) value can be used to get an approximate value of peak-to-peak ripple.

The peak-to-peak ripple voltage, rms value can be expressed as follow:

$$V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2} \quad (9)$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 3. Suggested Capacitors and Their Suppliers

Model	Type	Vendor	Voltage Rating	Case Size Inch (mm)
4.7 µF for C_{IN}				
C2012X5R0J475K	Ceramic, X5R	TDK	6.3V	0805 (2012)
JMK212BJ475K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
GRM21BR60J475K	Ceramic, X5R	Murata	6.3V	0805 (2012)
C1608X5R0J475K	Ceramic, X5R	TDK	6.3V	0603 (1608)
10 µF for C_{OUT}				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3V	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3V	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3V	0805 (2012)
C1608X5R0J106K	Ceramic, X5R	TDK	6.3V	0603 (1608)

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

Good layout for the LM3676 can be implemented by following a few simple design rules below. See Figure 29 for top layer board layout.

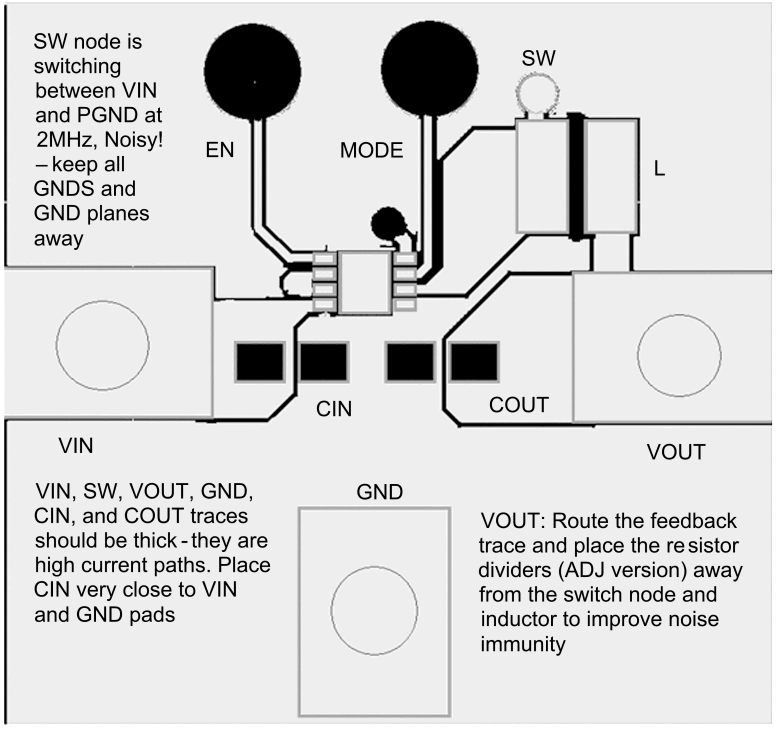


Figure 29. Top Layer of Board Layout for LM3676

1. *Place the LM3676, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor through the LM3676 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3676 by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. *Connect the ground pins of the LM3676 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3676 by giving it a low-impedance ground connection. Connect SGND to PGND at one single point within the board layout.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.

5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3676 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3676SD-1.8/NOPB	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-30 to 85	S009B
LM3676SD-1.8/NOPB.A	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-30 to 85	S009B
LM3676SD-3.3/NOPB	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-30 to 85	S010B
LM3676SD-3.3/NOPB.A	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-30 to 85	S010B
LM3676SD-ADJ/NOPB	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-30 to 85	S008B
LM3676SD-ADJ/NOPB.A	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-30 to 85	S008B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

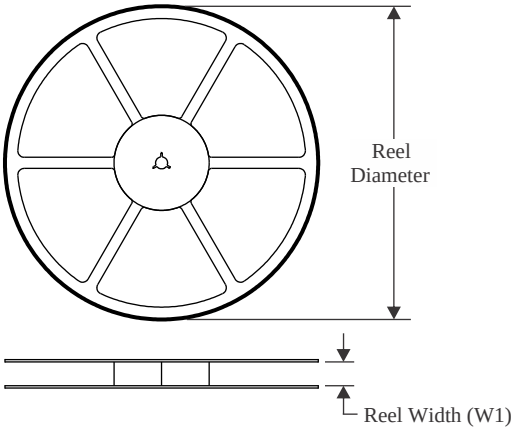
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

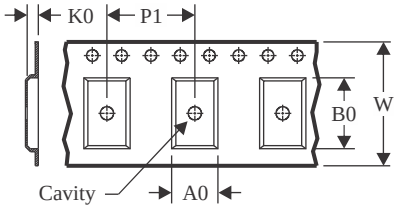
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

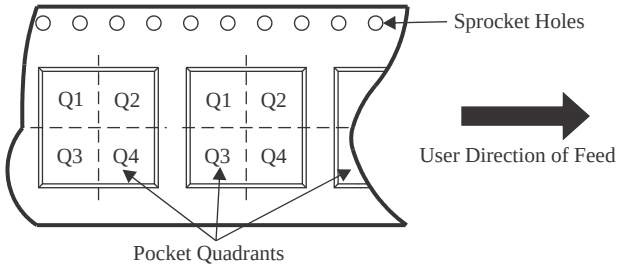


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

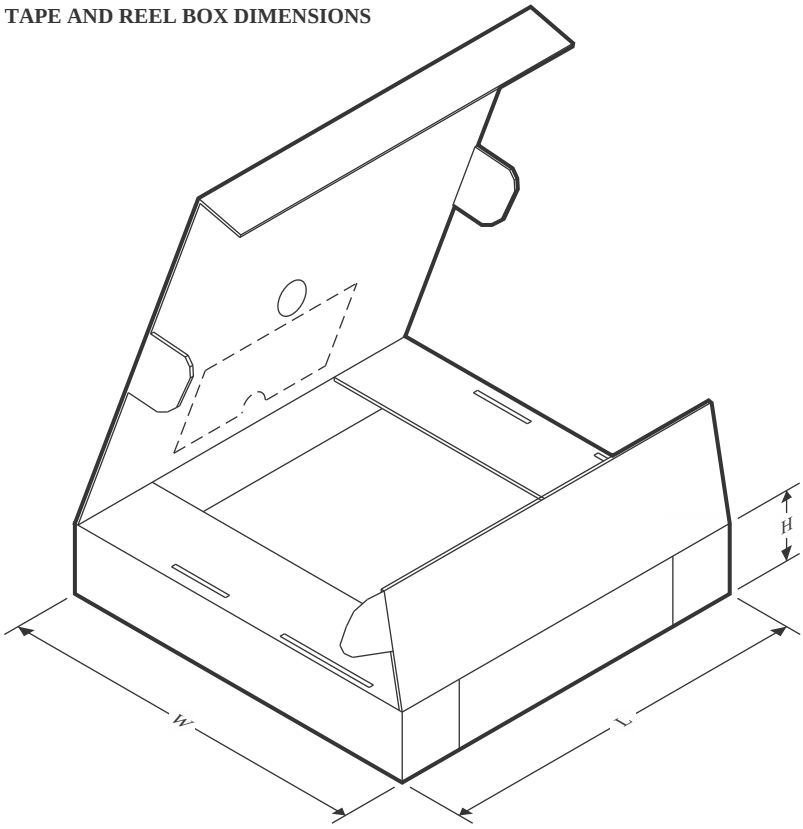
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3676SD-1.8/NOPB	WSON	NGQ	8	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3676SD-3.3/NOPB	WSON	NGQ	8	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3676SD-ADJ/NOPB	WSON	NGQ	8	1000	177.8	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

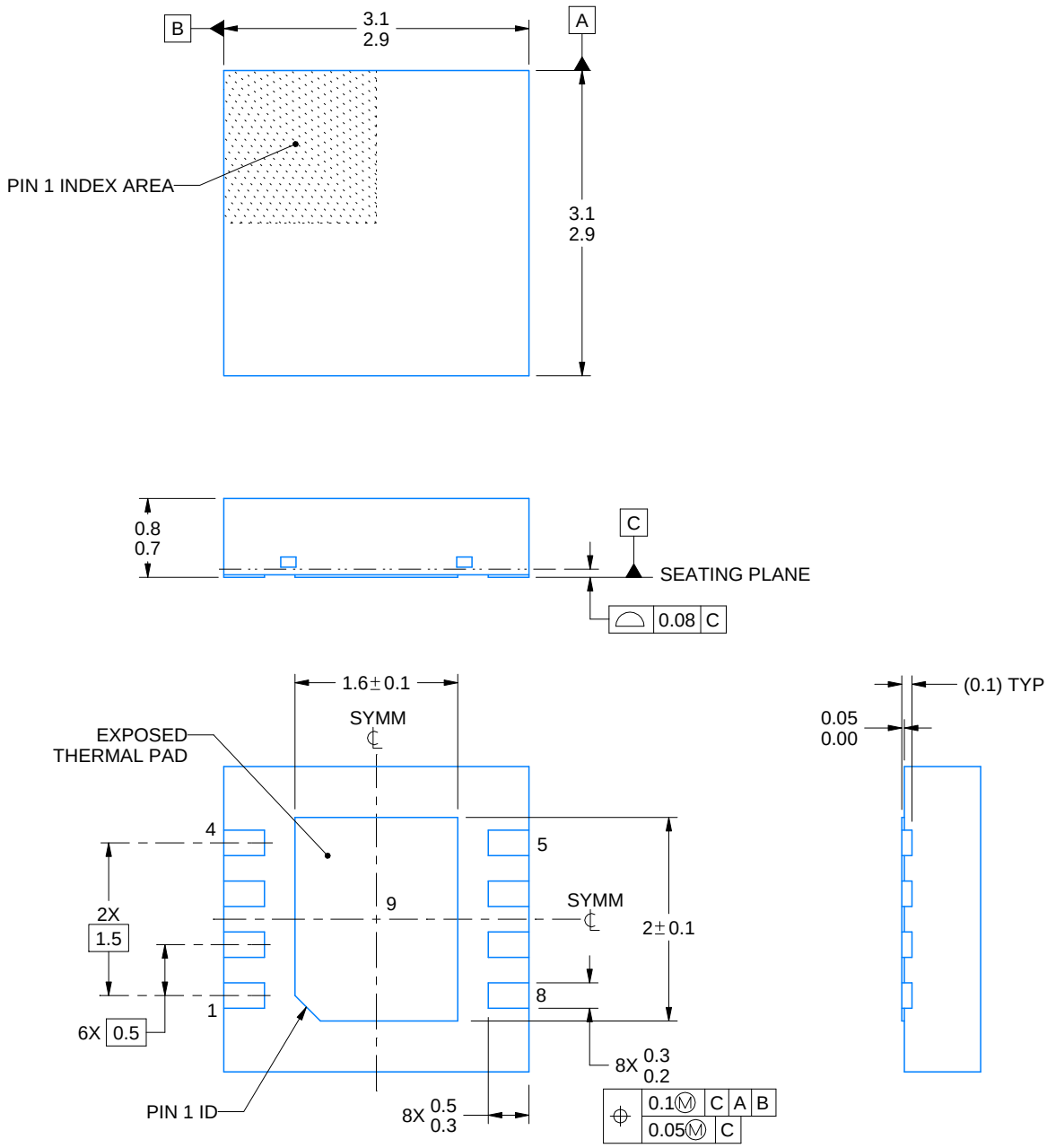
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3676SD-1.8/NOPB	WSON	NGQ	8	1000	208.0	191.0	35.0
LM3676SD-3.3/NOPB	WSON	NGQ	8	1000	208.0	191.0	35.0
LM3676SD-ADJ/NOPB	WSON	NGQ	8	1000	208.0	191.0	35.0

PACKAGE OUTLINE

NGQ0008A

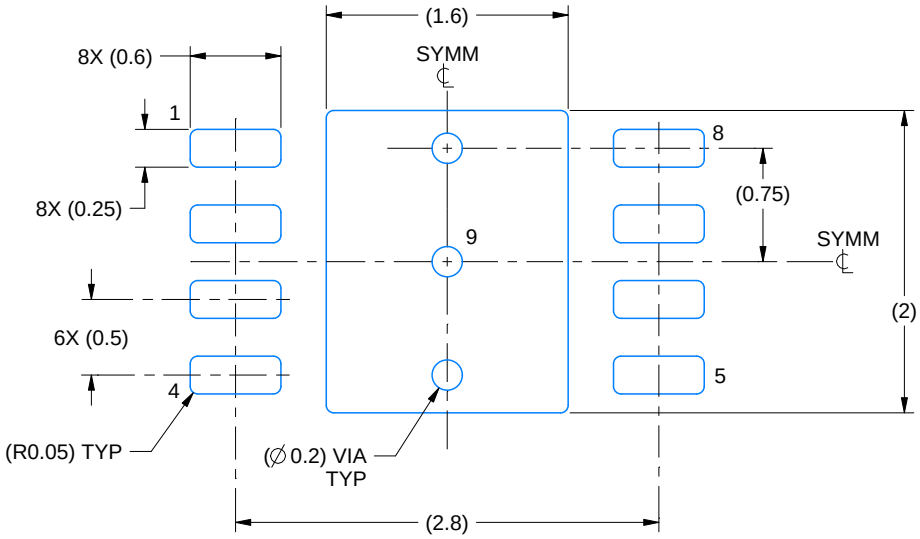
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

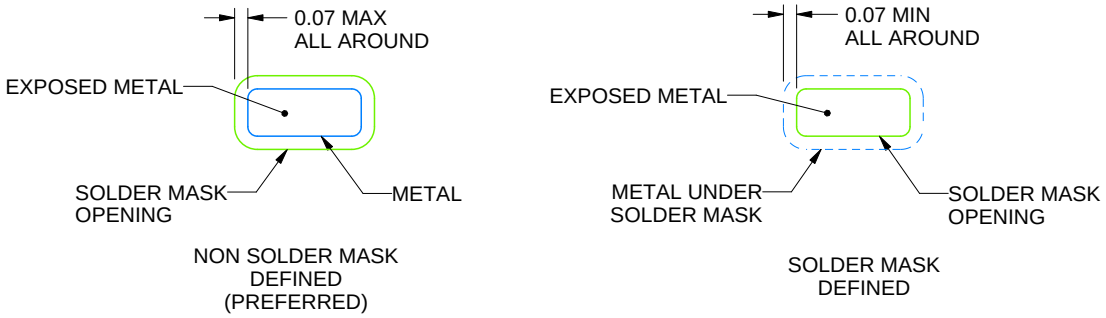


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

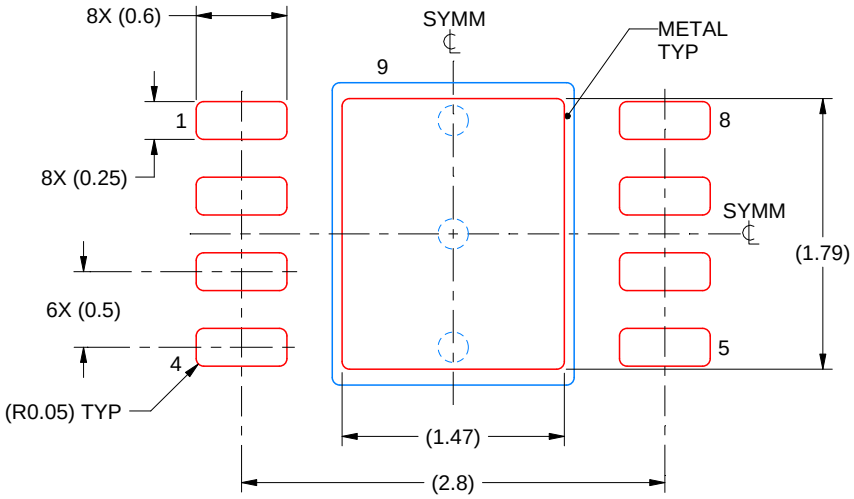


SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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