LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-2.5V, 3.3V LVPECL/ECL FANOUT BUFFER

ICS853S314I

General Description

The ICS853S314I is a low skew 1-to-4 Differential Fanout Buffer, designed with clock distribution in mind, accepting two clock sources into an input MUX. The MUX is controlled by a CLK_SEL pin. This makes the ICS853S314I very versatile, in that, it can operate as both a differential clock buffer as well as a signal-level translator and fanout buffer.

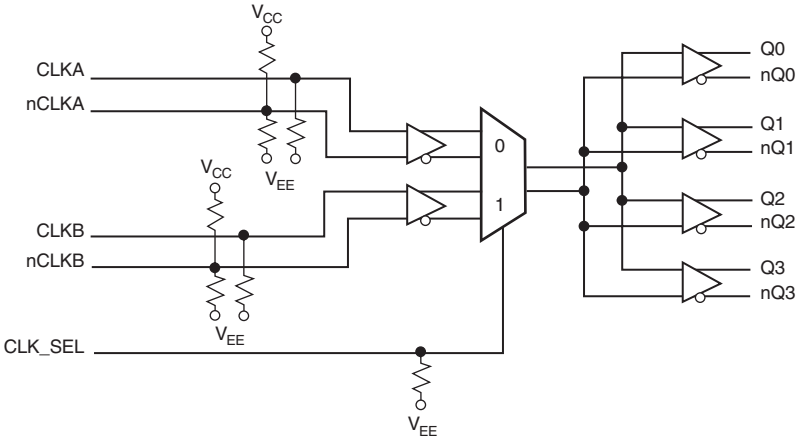
The device is designed on a SiGe process and can operate at frequencies in excess of 2.7GHz. This ensures negligible jitter introduction to the timing budget which makes it an ideal choice for distributing high frequency, high precision clocks across back planes and boards in communication systems. Internal temperature compensation guarantees consistent performance across various platforms.

Features

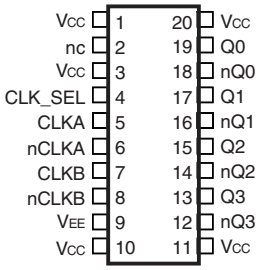
- Four differential ECL/LVPECL level outputs
- One differential ECL/LVPECL or single-ended input (CLKA)
  One differential HSTL or single-ended input (CLKB)
- Maximum output frequency: 2.7GHz
- Additive phase jitter, RMS: 0.138ps (typical) @ 156.25MHz,
- Output skew: 50ps (maximum)
- Part-to-part skew: 150ps (maximum)
- LVPECL and HSTL mode operating voltage supply range:
  V_{CC} = 2.5V±5% or 3.3V±5%, V_{EE} = 0V

  ECL mode operating voltage supply range:
  V_{EE} = -3.3V±5% or -2.5V±5%, V_{CC} = 0V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS853S314I
20-Lead, 209-MIL SSOP
5.30mm x 7.20mm x 1.75mm body package
F Package
Top View

20-Lead TSSOP
4.4mm x 6.5mm x 0.925mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 3, 10 11, 20	V_{CC}	Power		Positive supply pins.
2	nc	Unused		No connect.
4	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLKB, nCLKB inputs. When LOW, selects CLKA, nCLKA inputs.
5	CLKA	Input	Pulldown	Default non-inverting differential clock input. LVPECL/ECL interface levels.
6	nCLKA	Input	Pullup/ Pulldown	Default inverting differential clock input. LVPECL/ECL interface levels.
7	CLKB	Input	Pulldown	Alternative non-inverting differential clock input. HSTL interface levels.
8	nCLKB	Input	Pullup/ Pulldown	Alternative inverting differential clock input. HSTL interface levels.
9	V_{EE}	Power		Negative supply pin.
12, 13	nQ3, Q3	Output		Differential output pair. LVPECL/ECL interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVPECL/ECL interface levels.
16, 17	nQ1, Q1	Output		Differential output pair. LVPECL/ECL interface levels.
18, 19	nQ0, Q0	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			75		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ

TABLE 3. GENERAL SPECIFICATIONS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Output Termination Voltage			V_{CC} - 2		V
MM	ESD Protection (Machine Model)		200			V
HBM	ESD Protection (Human Body Model)		4000			V
CDM	ESD Protection (Charged Device Model)		2000			V
LU	Latch-up Immunity		200			mA

Absolute Maximum Ratings

Supply Voltage, V_{CC}	3.9V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-3.9V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.3V to V_{CC} + 0.3 V
Inputs, V_I (ECL mode)	0.3V to V_{EE} - 0.3V
Outputs, I_O	
Continuous Current	50mA
Package Thermal Impedance, θ_{JA}	
20 Lead SSOP	80.8°C/W (0 lfpm)
20 Lead TSSOP	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. LVPECL/HSTL DC Characteristics, V_{CC} = 2.5V±5% or 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Control Input CLK_SEL						
V_{IL}	Input Low Voltage		V_{CC} -1.810		V_{CC} -1.475	V
V_{IH}	Input High Voltage		V_{CC} -1.165		V_{CC} -0.880	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			100	µA
Clock Input Pair CLKA, nCLKA (LVPECL differential signals)						
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.1		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 2		1.0		V_{CC} -0.3	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			100	µA
Clock Input Pair CLKB, nCLKB (HSTL differential signals)						
V_{DIF}	Differential Input Voltage; NOTE 3	V_{CC} = 3.3V	0.4			V
		V_{CC} = 2.5V	0.4			V
V_X	Differential Crosspoint Voltage; NOTE 4		0	0.68 - 0.9	V_{CC} -1.0	V
I_{IN}	Input Current	$V_{IN} = V_X$ ± 0.2V			200	µA
LVPECL Clock Outputs (Q0:Q3, nQ0:nQ3)						
V_{OH}	Output High Voltage		V_{CC} -1.2	V_{CC} -1.005	V_{CC} -0.7	V
V_{OL}	Output Low Voltage	V_{CC} = 3.3V±5%	V_{CC} -1.9	V_{CC} -1.705	V_{CC} -1.5	V
		V_{CC} = 2.5V±5%	V_{CC} -1.9	V_{CC} -1.705	V_{CC} -1.3	V
Supply Current						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current				92	mA

NOTE 1: V_{PP} is the minimum differential input voltage swing required to maintain device functionality.

NOTE 2: V_{CMR} is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} specification.

NOTE 3: V_{DIF} is the minimum differential HSTL input voltage swing required for device functionality.

NOTE 4: V_X is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X range and the input swing lies within the V_{PP} specification.

TABLE 4B. ECL DC CHARACTERISTICS, V_{CC} = 0V, V_{EE} = -2.5V±5% OR -3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Control Input CLK_SEL						
V_{IL}	Input Low Voltage		-1.810		-1.475	V
V_{IH}	Input High Voltage		-1.165		-0.880	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			100	µA
Clock Input Pair CLKA,/nCLKA (ECL differential signals)						
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.1		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 2		V_{EE} + 1.0		-0.3	V
I_{IN}	Input Current	$V_{IN} = V_{IL\ or}$ $V_{IN} = V_{IH}$			100	µA
ECL Clock Outputs (Q0:Q3, nQ0:nQ3)						
V_{OH}	Output High Voltage		-1.2	-1.005	-0.7	V
V_{OL}	Output Low Voltage	V_{EE} = -3.3V±5%	-1.9	-1.705	-1.5	V
		V_{EE} = -2.5V±5%	-1.9	-1.705	-1.3	V
Supply Current						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current				92	mA

NOTE 1: V_{PP} is the minimum differential input voltage swing required to maintain device functionality.

NOTE 2: V_{CMR} is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} specification.

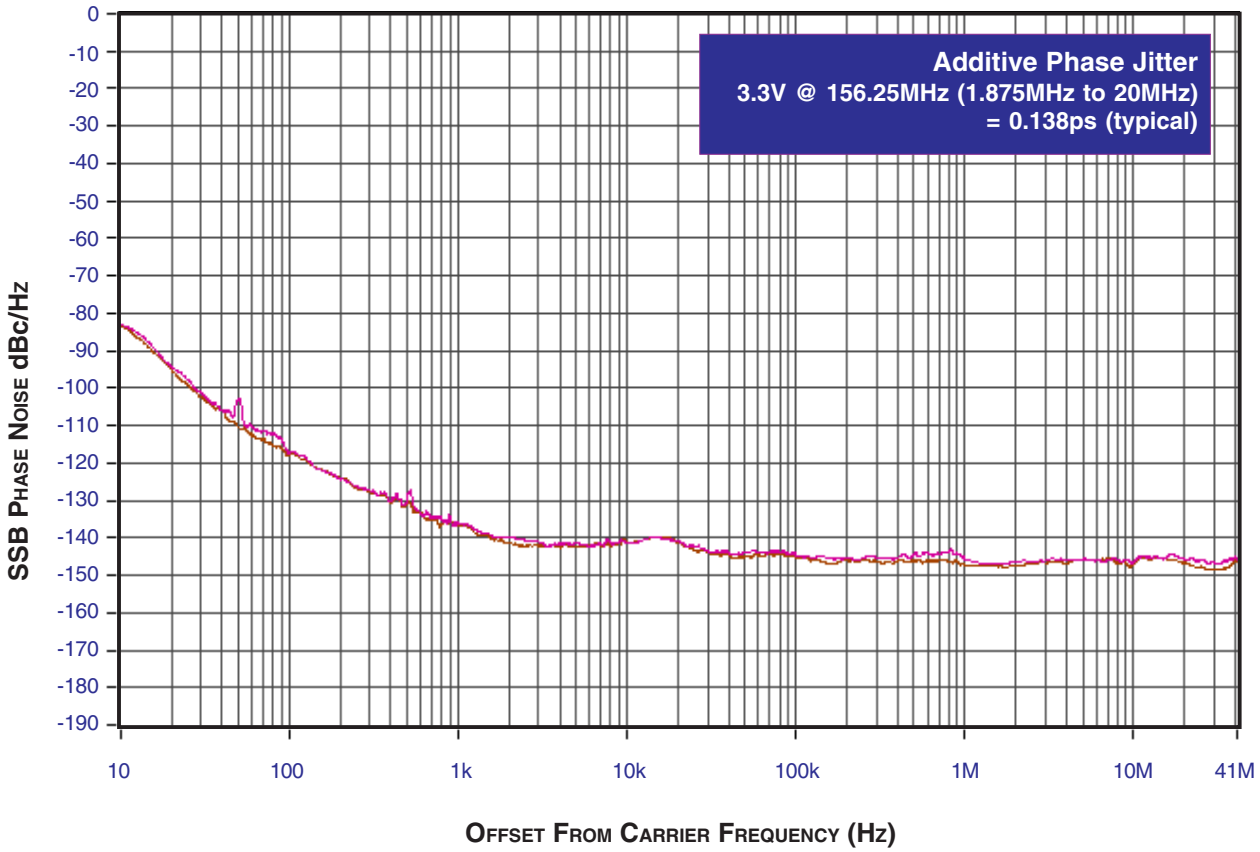
TABLE 5. AC CHARACTERISTICS, (LVPECL/HSTL): V_{CC} = 3.3V±5% OR 2.5V±5%, V_{EE} = 0V, OR (ECL): V_{EE} = -3.3V±5% OR -2.5V±5%, V_{CC} = 0V; T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Differential Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Differential Input Crosspoint Voltage; NOTE 2		V_{EE} + 1.0		V_{CC} - 0.3	V
f_{CLK}	Input Frequency; NOTE 3				2.7	GHz
t_{PD}	Propagation Delay, CLKA or CLKB to Output Pair		280		650	ps
V_{DIF}	HSTL Differential Input Voltage; NOTE 4		0.4		1.0	V
V_X	HSTL Input Differential Crosspoint Voltage; NOTE 5		V_{EE} + 0.01		V_{CC} - 1.0	V
V_O(pp)	Differential Output Voltage (peak-to-peak)	f_O < 300MHz	0.45	0.72	0.95	V
		f_O < 1.5GHz	0.3	0.55	0.95	V
*t*sk(o)	Output Skew				50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 6				150	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz @ 3.3V, (1.875MHz - 20MHz)		0.138		ps
		312.5MHz @ 3.3V, (1.875MHz - 20MHz)		0.092		ps
*t*sk(p)	Output Pulse Skew; NOTE 7	660MHz			75	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	0.05		0.3	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
NOTE 1: V_{PP} is the minimum differential ECL/LVPECL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
NOTE 2: V_{CMR} is the crosspoint of the differential ECL/LVPECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} specificatiion. Violation of V_{CMR} or V_{PP} impacts the device propagation delay, device and part-to-part skew.
NOTE 3: The ICS853S314I is fully operational up to 2.7GHz and is characterized up to 1.5GHz.
NOTE 4:V_{DIF} is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
NOTE 5: V_X is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X range and the input swing lies within the V_{DIF} specification. Violation of V_X or V_{DIF} impacts the device propgation delay, device and part-to-part skew.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 7: Output pulse skew is the absolute value of the difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

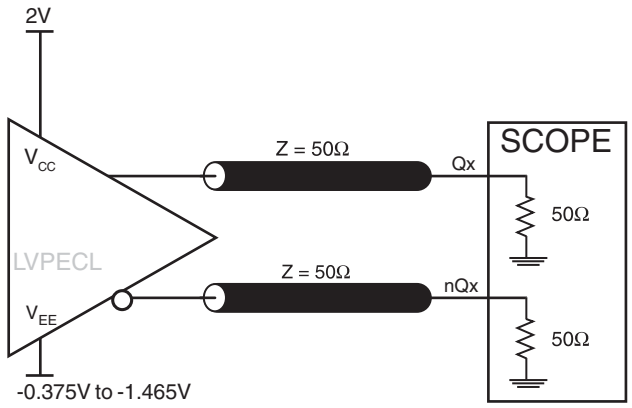
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

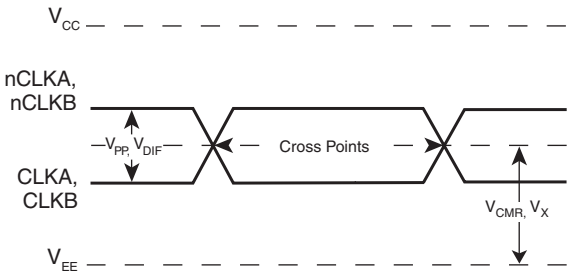


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

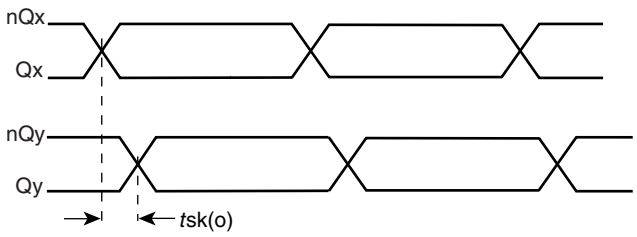
Parameter Measurement Information



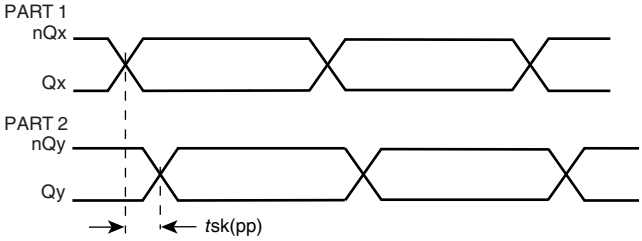
2.5V/3.3V Output Load AC Test Circuit



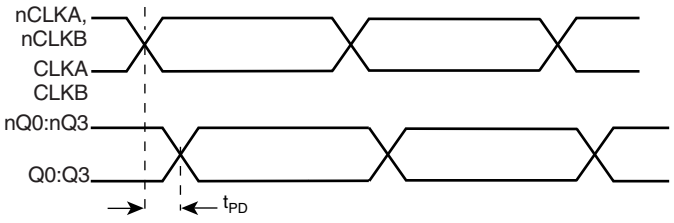
Differential Input Level



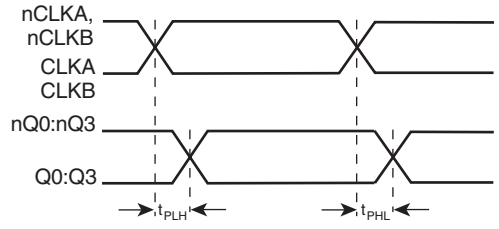
Output Skew



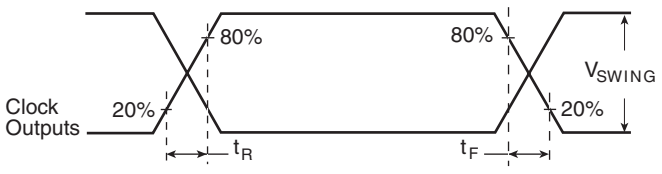
Part-to-Part Skew



Propagation Delay



Output Pulse Skew



Output Rise/Fall Time

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLKx/nCLKx INPUT:
For applications not requiring the use of the differential input, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

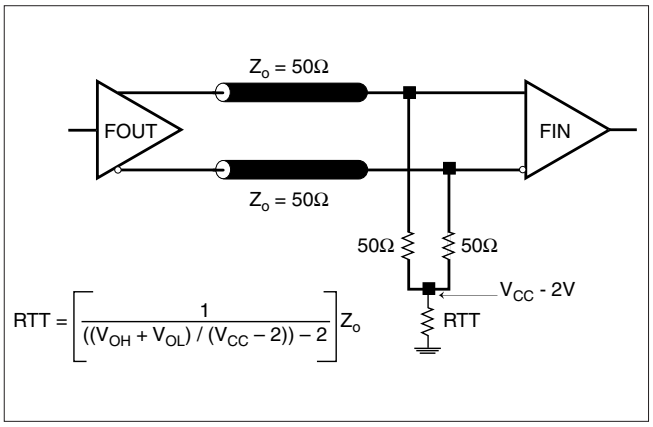


FIGURE 1A. LVPECL OUTPUT TERMINATION

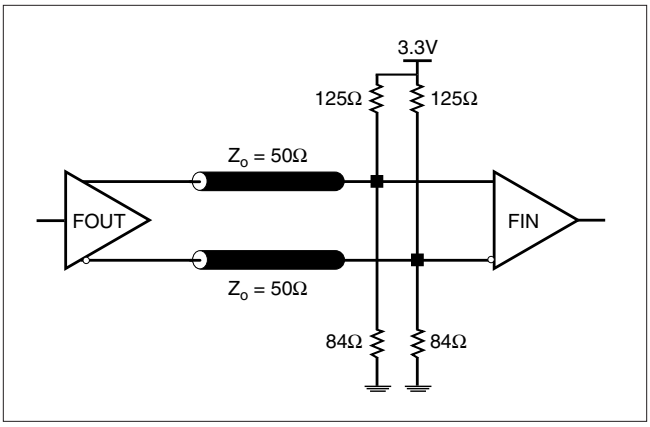


FIGURE 1B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 2A and *Figure 2B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 2B can be eliminated and the termination is shown in *Figure 2C.*

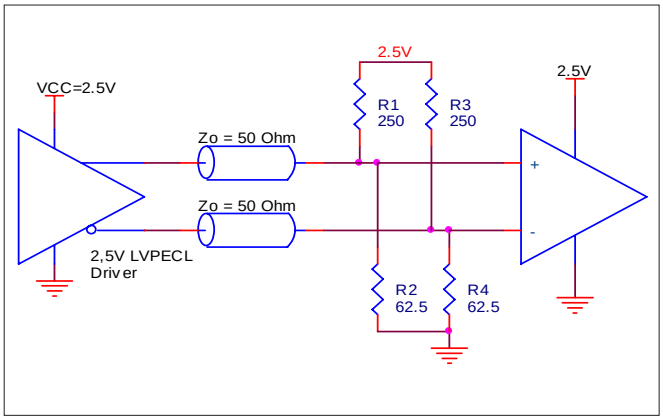


FIGURE 2A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

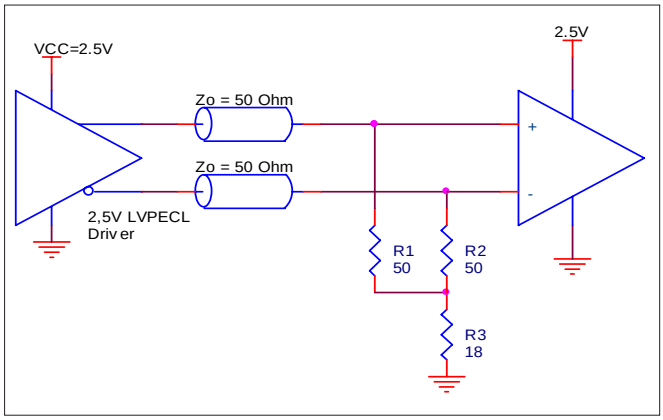


FIGURE 2B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

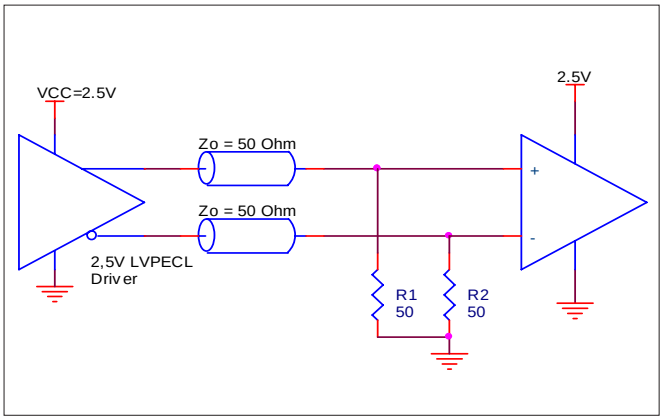


FIGURE 2C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853S314I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853S314I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 92mA = **318.78mW**
- Power (outputs)$_{MAX}$ = **33mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 33mW = **132mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 318.78mW + 132mW = **450.78mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.450W * 90.4°C/W = 125°C. This is within the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6A. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	94.8°C/W	90.4°C/W	88.3°C/W

TABLE 6B. THERMAL RESISTANCE θ_{JA} FOR 20-PIN SSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	80.8°C/W	73.2°C/W	69.2°C/W

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 3.*

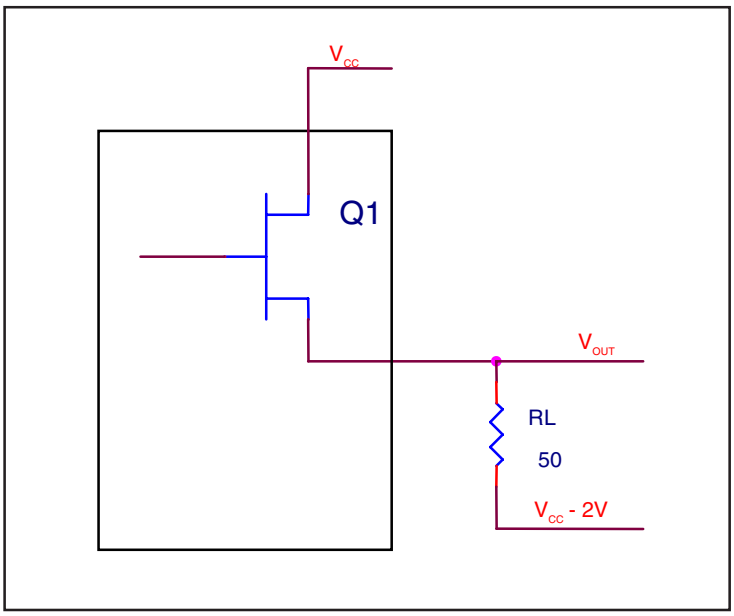


FIGURE 3. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.7V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.7V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.5V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.5V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.7V)/50\Omega] * 0.7V =$ **18.0mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.5V)/50\Omega] * 1.5V =$ **15mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33mW**

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD SSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	80.8°C/W	73.2°C/W	69.2°C/W

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

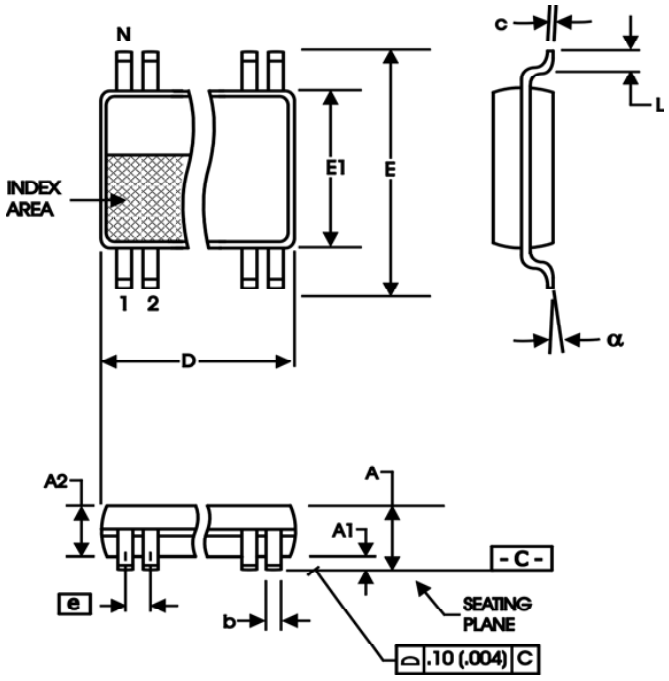
θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	94.8°C/W	90.4°C/W	88.3°C/W

TRANSISTOR COUNT

The transistor count for ICS853S314I is: 450 (approximately)

Pin compatible with CY2DP314

Package Outline - F Suffix for 20 Lead SSOP



Package Outline - G Suffix for 20 Lead TSSOP

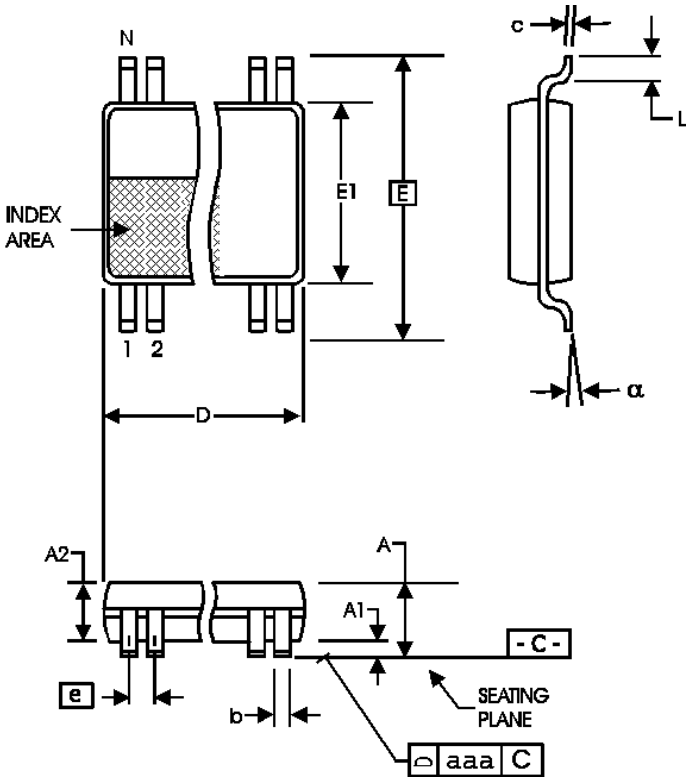


Table 8A. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.0
A1	0.05	--
A2	1.65	1.85
b	0.22	0.38
c	0.09	0.25
D	6.90	7.50
E	7.40	8.20
E1	5.0	5.60
e	0.65 BASIC	
L	0.55	0.95
α	0°	8°

Reference Document: JEDEC Publication 95, MO-150

Table 8B. Package Dimensions

Symbol	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S314AFI	ICS853S314AI	20 lead SSOP	tube	-40°C to 85°C
853S314AFIT	ICS853S314AI	20 lead SSOP	2500 tape & reel	-40°C to 85°C
853S314AFILF	ICS53S314AIL	20 lead "Lead-Free" SSOP	tube	-40°C to 85°C
853S314AFILFT	ICS53S314AIL	20 lead "Lead-Free" SSOP	2500 tape & reel	-40°C to 85°C
853S314AGI	ICS53S14AGI	20 lead TSSOP	tube	-40°C to 85°C
853S314AGIT	ICS53S14AGI	20 lead TSSOP	2500 tape & reel	-40°C to 85°C
853S314AGILF	ICS3S314AGIL	20 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
853S314AGILFT	ICS3S314AGIL	20 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T9	14	Ordering Information Table - Added "Lead-Free" Marking.	1/24/09

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