CD74AC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCHS336 - MARCH 2003

 AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage

- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
 Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

M PACKAGE (TOP VIEW) 16 V_{CC} A/B 15 ∏ G 1А П 2 14 7 4A 1B **∏** 3 1Y 🛛 13 4B 2A 🛮 5 12 1 4Y 11 **∏** 3A 6 2B 🛚 2Y [7 10 **3** 3 3 B **GND** 9**∏** 3Y

description/ordering information

This quadruple 2-line to 1-line data selector/multiplexer is designed for 1.5-V to 5.5-V V_{CC} operation.

The CD74AC158 features a common strobe (\overline{G}) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. This device provides inverted data.

ORDERING INFORMATION

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC - M	Tube	CD74AC158M	AC158M

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each data selector/multiplexer)

	INPU	OUTPUT		
G	A/B	Α	В	Υ
Н	Х	Χ	Х	Н
L	L	L	Χ	Н
L	L	Н	X	L
L	Н	Χ	L	Н
L	Н	Χ	Н	L

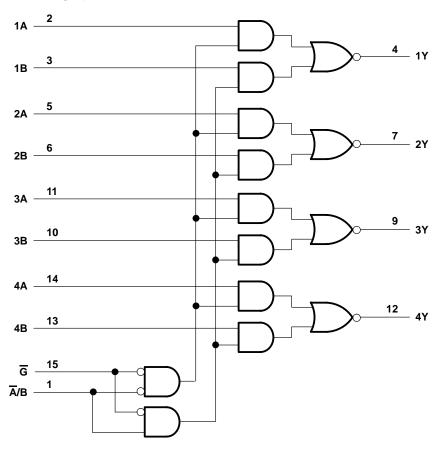


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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 6 V
Input clamp current, I _{IK} (V _I < 0 V or V _I > V _{CC}) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0 \text{ V or } V_O > V_{CC}$) (see Note 1)	±50 mA
Continuous output current, I_O ($V_O > 0$ V or $V_O < V_{CC}$)	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 2)	
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

			T _A = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Vcc	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
		V _{CC} = 1.5 V	1.2		1.2		1.2		
VIН	High-level input voltage	V _{CC} = 3 V	2.1		2.1		2.1		V
		V _{CC} = 5.5 V	3.85		3.85		3.85		
		V _{CC} = 1.5 V		0.3		0.3		0.3	
VIL	Low-level input voltage	VCC = 3 V		0.9		0.9		0.9	V
		V _{CC} = 5.5 V		1.65		1.65		1.65	
٧ _I	Input voltage		0	VCC	0	VCC	0	VCC	V
۷o	Output voltage		0	VCC	0	VCC	0	VCC	V
ІОН	High-level output current	V _{CC} = 4.5 V to 5.5 V		-24		-24		-24	mA
loL	Low-level output current	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		24		24		24	mA
Δt/Δν	langet transition rise or fall rate	V _{CC} = 1.5 V to 3 V		50		50		50	ns/V
ΔυΔν	Input transition rise or fall rate	V _{CC} = 3.6 V to 5.5 V		20		20		20	115/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	Vcc	T _A = 2	T _A = 25°C		C to °C	–40°C to 85°C		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	
			1.5 V	1.4		1.4		1.4		
		$I_{OH} = -50 \mu A$	3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
Voн	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -4 \text{ mA}$	3 V	2.58		2.4		2.48		V
		$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8		
		$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V			3.85				
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85		
			1.5 V		0.1		0.1		0.1	
		$I_{OL} = 50 \mu A$	3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
V_{OL}	VI = VIH or VIL	$I_{OL} = 12 \text{ mA}$	3 V		0.36		0.5		0.44	V
		$I_{OL} = 24 \text{ mA}$	4.5 V		0.36		0.5		0.44	
		$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V				1.65			
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V						1.65	
lį	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μΑ
ICC	$V_I = V_{CC}$ or GND,	IO = 0	5.5 V		8		160		80	μΑ
Ci					10		10		10	pF

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.



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switching characteristics over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°(125°		–40°0 85°		UNIT	
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX		
^t PLH	A or B	A on D					no	
^t PHL	AUB	Any Y		100	91		ns	
^t PLH	Ā/B	Any Y		161		147	ns	
^t PHL	А/В	Ally 1		161		147	110	
^t PLH	G	- AV		149		135	20	
^t PHL	g	Any Y		149		135	ns	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55° 125		–40° 85°	UNIT	
	(1141 01)	(6611 61)	MIN	MAX	MIN	MAX	
^t PLH	A or B	Any	2.8	11.2	3	12.8	20
^t PHL	AUB	Any Y	2.8	11.2	3	12.8	ns
t _{PLH}	- T	Any Y	4.5	18.1	4.9	16.5	ns
^t PHL	Ā/B	Ally 1	4.5	18.1	4.9	16.5	110
^t PLH	G	Any Y	4.2	16.7	4.5	15.2	nc
^t PHL	9	Ally 1	4.2	16.7	4.5	15.2	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

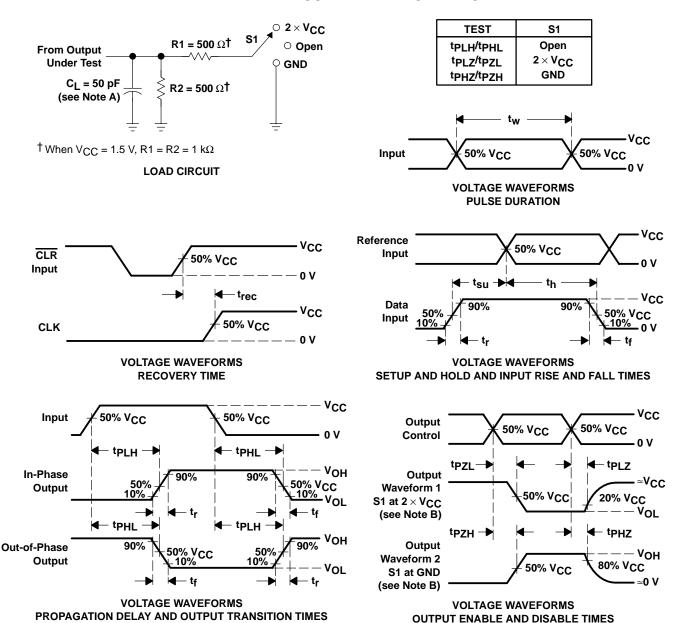
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°(125		–40°(85°	UNIT	
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	
^t PLH	A or B	Any Y	2	8	2.2	7.3	nc
^t PHL	A 01 B	Ally 1	2	8	2.2	7.3	ns
^t PLH	Ā/B	Any Y	3.2	12.9	3.5	11.7	nc
t _{PHL}	А/В	Ally 1	3.2	12.9	3.5	11.7	ns
t _{PLH}	G	Any Y	3	11.9	3.2	10.8	ns
t _{PHL}	9	Ally I	3	11.9	3.2	10.8	115

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TYP	UNIT
C _{pd}	Power dissipation capacitance	149	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f = 3$ ns, $t_f = 3$ ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. tpzL and tpzH are the same as ten.
- H. tpLz and tpHz are the same as tdis.
- I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





PACKAGE OPTION ADDENDUM

10-Jun-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC158M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC158M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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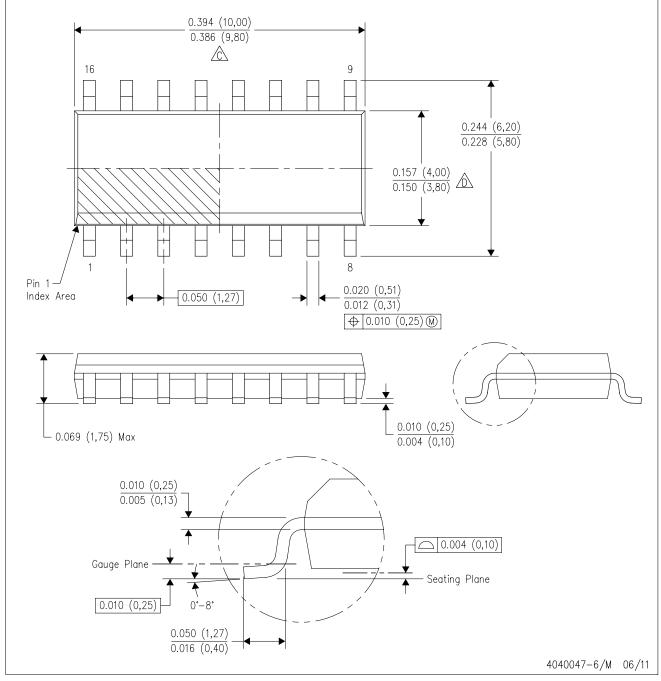




10-Jun-2014

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



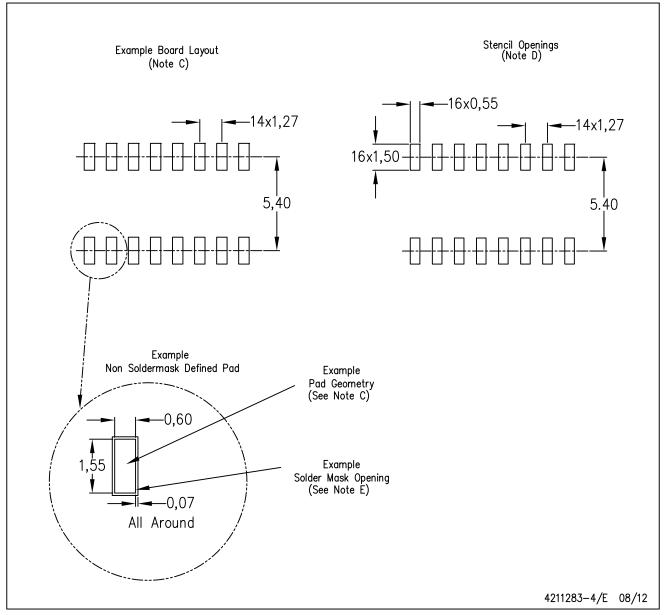
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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