50-A, 8-V TO 14-V INPUT, NON-ISOLATED WIDE-OUTPUT ADJUST POWER MODULE

FEATURES

- **50-A Output Current**
- **8-V to 14-V Input Voltage**
- **Wide-Output Voltage Adjust (0.8 V to 5.5 V)**
- **Efficiencies up to 96%**
- **On/Off Inhibit**
- **Differential Output Sense**
- **Output Overcurrent Protection (Nonlatching, Auto-Reset)**
- **Overtemperature Protection**
- **Auto-Track™ Sequencing**
- **Start Up Into Output Prebias**
- **Margin Up/Down Controls**
- **Operating Temperature: –40°C to 85°C**
- **Multi-Phase, Switch-Mode Topology**
- **Programmable Undervoltage Lockout (UVLO)**
- **Safety Agency Approvals: UL/cUL 60950, EN60950, VDE**

APPLICATIONS

- **Advanced Computing and Server Applications**

NOMINAL SIZE = 2.05 in x 1.05 in (52 mm x 26,7 mm)

DESCRIPTION

The PTH12040W is a high-performance 50-A rated, non-isolated, power module, which uses the latest multiphase switched-mode topology. This provides a small, ready-to-use module, that can power the most densly populated multiprocessor systems.

Operating from an input voltage range of 8 V to 14 V, the PTH12040W requires a single resistor to set the output voltage to any value over the range, 0.8 V to 5.5 V. The wide input voltage range makes the PTH12040W particularly suitable for advanced computing and server applications that utilize a loosely regulated 12-V intermediate distribution bus.

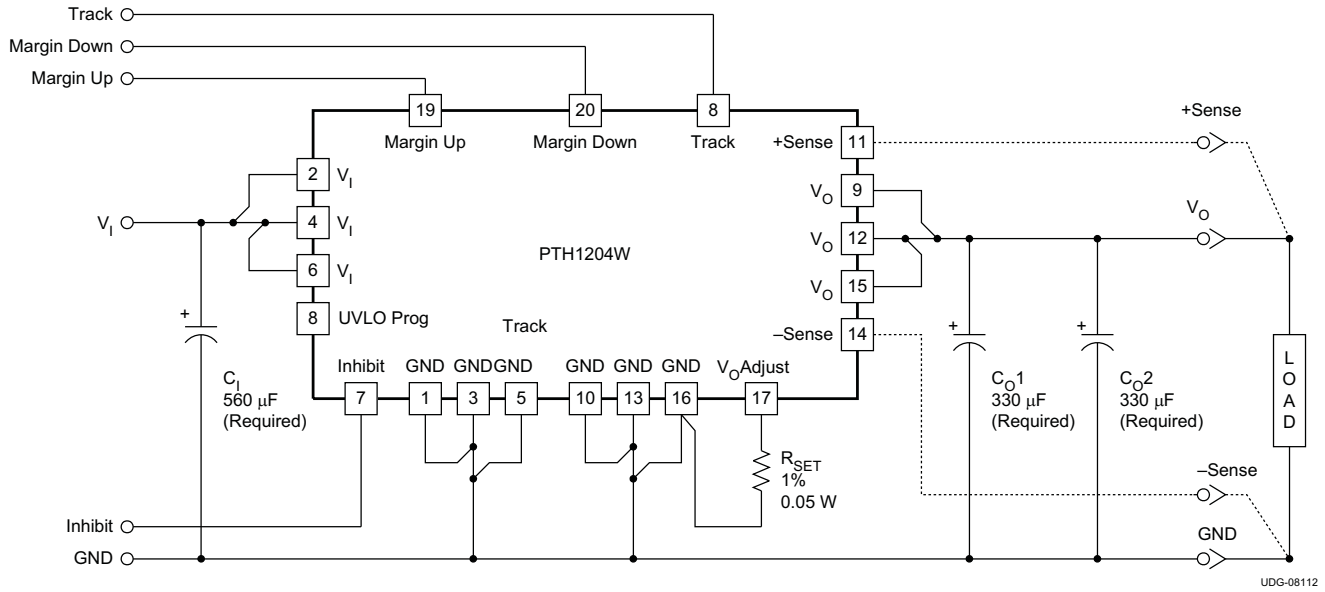
The modules incorporate a comprehensive list of features. They include on/off inhibit and margin up/down controls. A differential remote output voltage sense ensures tight load regulation, and an output overcurrent and overtemperature shutdown protect against most load faults. The programmable under-voltage lockout allows the turn-on and turn-off voltage thresholds to be customized.

The PTH12040W incorporates Auto-Track™. The Auto-Track feature of the PTH family allows the outputs of multiple modules to track a common voltage during power up and power down transitions. This simplifies power up and power down supply-voltage sequencing in a power supply system.

The modules use double-sided surface mount construction to provide a low profile and compact footprint. Package options include both through-hole and surface mount configurations.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

STANDARD APPLICATION



A. R_{SET} = Required to set the output voltage higher than the minimum value (see the elcetrical characheristics for values.)

B. C_I = Required 560-µF electrolytic capacitor. 1000 µF recommended.

C. C_O = Required 660-µF (or 680 µF) electrolytic capacitor.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

				UNIT
	Signal input voltages	Track control (pin 18)		–0.3 V to V_I + 0.3 V
T_A	Operating temperature range over V_I range			–40°C to 85°C
T_{wave}	Wave solder temperature	Surface temperature of module body or pins **(5 seconds maximum)**	PTH12040WAH	260°C (1)
			PTH12040WAD	
T_{reflow}	Solder reflow temperature	Surface temperature of module body or pins	PTH12040WAS	235°C (1)
			PTH12040WAZ	260°C (1)
T_{stg}	Storage temperature	Storage temperature of module removed from shipping package		–55°C to 125°C
T_{pkg}	Packaging temperature	Shipping Tray storage or bake temperature		45°C
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, 1/2 Sine, mounted		500 G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20–2000 Hz		15 G
	Weight			17 grams
	Flammability	Meets UL94V-O		

(1) During the soldering process, do not elevate peak temperature of the module, pins, or internal components above the stated maximum.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_I = 12 V, V_O = 3.3 V, C_I = 1000 µF, C_O = 660 µF, and I_O = $I_O$max (unless otherwise stated)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	Output current	60°C, 200 LFM airflow		0		50(1)	A
V_I	Input voltage range	Over I_O range		8(2)		14	V
$V_O$tol	Set-point voltage tolerance					±2(3)	%V_O
ΔReg_{temp}	Temperature variation	–40°C < T_A < 85°C			±0.5		%V_O
ΔReg_{line}	Line regulation	Over V_I range			±5		mV
ΔReg_{load}	Load regulation	Over I_O range			±5		mV
ΔReg_{tot}	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C				±3(3)	%V_O
ΔReg_{adj}	Output adjust range			0.8		5.5(2)	V
η	Efficiency	I_O = 35 A	R_{SET} = 205 Ω, V_O = 5.0 V		96%		
			R_{SET} = 1.5 kΩ, V_O = 3.3 V		95%		
			R_{SET} = 3.01 kΩ, V_O = 2.5 V		93%		
			R_{SET} = 4.99 kΩ, V_O = 2.0 V		92%		
			R_{SET} = 6.34 kΩ, V_O = 1.8 V		91%		
			R_{SET} = 9.76 kΩ, V_O = 1.5 V		90%		
			R_{SET} = 18.2 kΩ, V_O = 1.2 V		88%		
			R_{SET} = 38.3 kΩ, V_O = 1.0 V		86%		
			R_{SET} = open circuit, V_O = 0.8 V		82%		
V_R	V_O ripple (pk-pk)	20 MHz bandwidth	All voltages		15		mVpp
$I_O$trip	Overcurrent threshold	Reset, followed by auto-recovery			95		A
	Transient response	1 A/µs load step, 50 to 100% $I_O$max, C_O = 660 µF					
t_{rr}			Recovery time		70		µSec
ΔV_{tr}			V_O over/undershoot		150		mV
$V_O$adj	Margin up/down adjust	With Margin up/down control			±5%		
I_{IL}margin	Margin input current	Pin to GND			–8(4)		µA
I_{IL}track	Track input current (pin 18)	Pin to GND				–0.10(5)	mA
dV_{track}/dt	Track slew rate capability	$\|V_{TRACK} - V_O\|$ ≤ 50 mV and V_{TRACK} < V_O(nom)				1	V/ms
UVLO	Undervoltage lockout	Pin 8 open	On-threshold		7.5(6)		V
			Hysterisis		1(6)		
	Inhibit control (pin 7)	Referenced to GND					
V_{IH}	Input high voltage			2.5		Open(7)	V
V_{IL}	Input low voltage			–0.2		0.5	
I_{IL}inhibit	Input low current	Pin to GND			0.5		mA
$I_I$inh	Input standby current	Inhibit (pin 7) to GND			35		mA
f_s	Switching frequency	Over V_I and I_O ranges		0.9	1.05	1.2	MHz
C_I	External input capacitance			560(8)	1000		µF

(1) See SOA curves or consult factory for appropriate derating.
(2) When the set-point voltage is adjusted higher than 3.6 V, a 10-V minimum input voltage is recommended.
(3) The set-point voltage tolerance is affected by the tolerance of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(4) A small, low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.
(5) This control pin has an internal pull-up to 6.7 V. If left open-circuit, the module operates when input power is applied. A small, low leakage (<100 nA) MOSFET or open-drain/collector voltage supervisor IC is recommended for control. See the *Application Information* section for further guidance.
(6) Default voltages may be adjusted using the *UVLO Prog* control input. See the *Application Information* section for further guidance.
(7) This control pin has an internal pull-up to 5 V nominal. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET is recommended for control. Do not place an external pull-up on this pin. For further information, see the related application note.
(8) A minimum capacitance of 560-µF is required at the input for proper operation. For best results, 1000 µF is recommended. The capacitance must be rated for a minimum of 300 mArms of ripple current.

ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, V_I = 12 V, V_O = 3.3 V, C_I = 1000 µF, C_O = 660 µF, and I_O = $I_O$max (unless otherwise stated)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_O	External output capacitance	Capacitance value	Nonceramic	660(9)		14000(10)	µF
			Ceramic			400	
		Equivalent series resistance (non-ceramic)		2(11)			mΩ
MTBF	Reliability	Per Bellcore TR-332 50% stress, T_A = 40°C, ground benigh		2.5			10^6Hrs

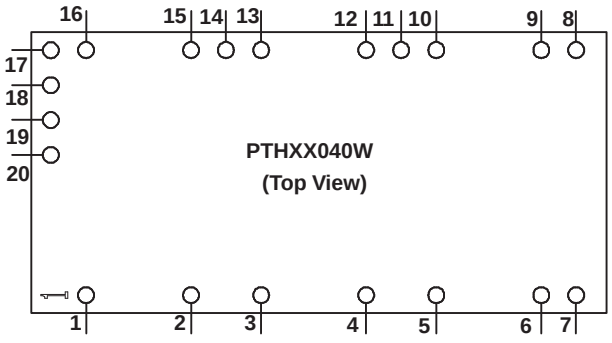
(9) A minimum value of output capacitance is required for proper operation. Adding additional capacitance at the load further improves transient response.
(10) This is the calculated maximum. The minimum ESR requirement often results in a lower value. See the *Application Information* section for further guidance.
(11) This is the typcial ESR for all the electrolytic (nonceramic) output capacitance. Use 4 mΩ as the minimum when using max-ESR values to calculate.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
GND	1, 3, 5, 10, 13, 16	The common ground connection for the V_I and V_O power connections. It is also the 0 V_{dc} reference for the control inputs.
V_I	2, 4, 6	The positive input voltage power node to the module, which is referenced to common GND.
V_O	9, 12, 15	The regulated positive power output with respect to the GND node.
Inhibit(1)	7	The Inhibit pin is an open-collector/drain negative logic input that is referenced to GND. Applying a lowlevel ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied.
V_O Adjust	17	A 1%, 0.05-W resistor must be connected between this pin and GND to set the output voltage higher than the minimum value. The set-point range for the output voltage is from 0.8 V to 5.5 V. The resistor required for a given output voltage may be calculated from the following formula. If left open circuit, the module output defaults to its lowest output voltage value. For further information on the adjustment and/or trimming of the output voltage, see the related Application Information section. $R_{set} = 10\ k\Omega \times \frac{0.8\ V}{V_O - 0.8\ V} - 1.696\ k\Omega$ The specification table gives the preferred resistor values for a number of standard output voltages.
+Sense	11	The sense inputs allow the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, +Sense should be connected to V_O. If it is left open, a low-value internal resistor ensures that the output remains in regulation.
–Sense	14	For optimal voltage accuracy, –Sense should be connected to the ground return at the load. If it is left open, a low-value internal resistor ensures that the output remains in regulation.
UVLO Prog	8	Connecting a resistor from this pin to signal ground allows the *on* threshold of the input undervoltage lockout (UVLO) to be adjusted higher than the default value. The hysterisis can also be independenly reduced by connecting a second resistor from this pin to V_I. For further information, see the Application Information section.
Track	18	This is an analog control input that allows the output voltage to follow another voltage during power up and power down sequences. The pin is active from 0 V, up to the nominal set-point voltage. Within this range, the module output follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its nominal output voltage. If unused, this input should be connected to V_I for a faster power up. For further information, see the Application Information section.
Margin Down(1)	20	When this input is asserted to GND, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is **not** TTL compatible. A lower percent change can be accommodated with a series resistor. For further information, see the Application Information section.
Margin Up(1)	19	When this input is asserted to GND, the output voltage is increased by 5%. The input requires an open collector (open-drain) interface. It is **not** TTL compatible. The percent change can be reduced with a series resistor. For further information, see the Application Information section.

(1) Denotes negative logic: Open = Normal operation / Ground = Function active



TYPICAL CHARACTERISTICS(1)(2)

Characteristic Data (V_I = 12 V)

EFFICIENCY VS LOAD CURRENT

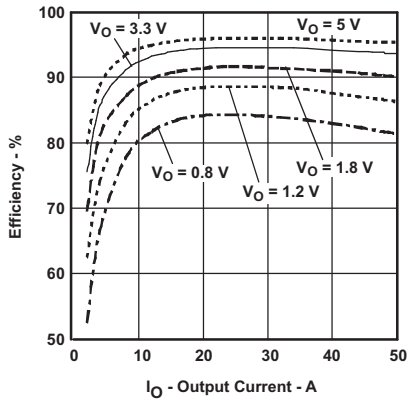


Figure 1.

POWER DISSIPATION VS LOAD CURRENT

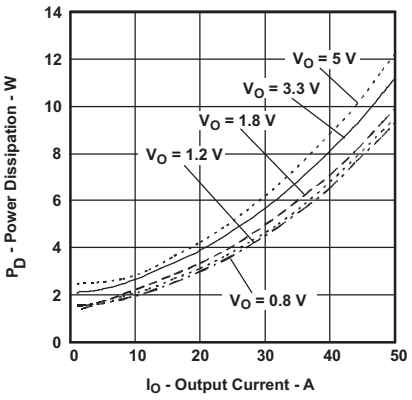


Figure 2.

TEMPERATURE DERATING VS OUTPUT CURRENT

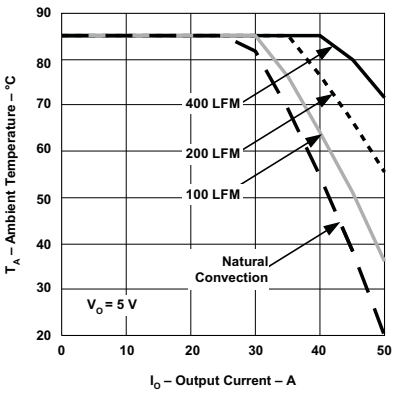


Figure 3.

TEMPERATURE DERATING VS OUTPUT CURRENT

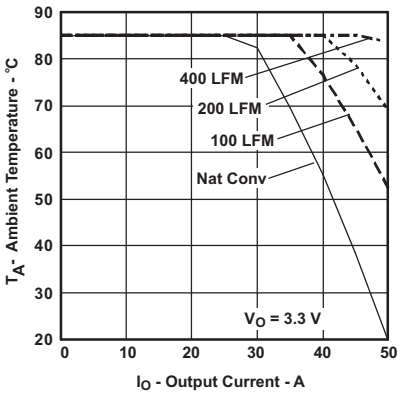


Figure 4.

TEMPERATURE DERATING VS OUTPUT CURRENT

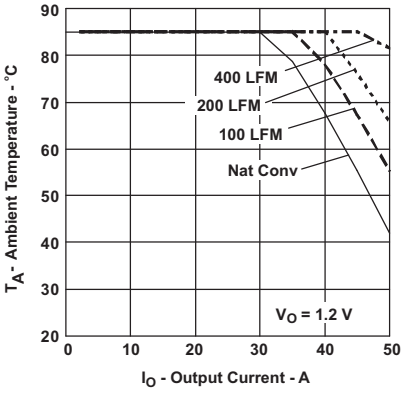


Figure 5.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1 and Figure 2.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4-inch x 4-inch, double-sided PCB with 1-oz. copper. For surface mount packages (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 3, Figure 4, and Figure 5.

TYPICAL CHARACTERISTICS(4)(5) (continued)

Characteristic Data (V_I = 8 V)(3)

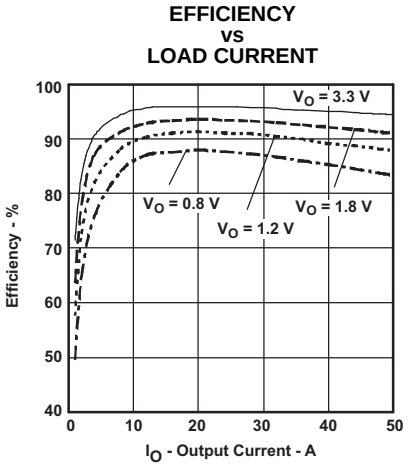


Figure 6.

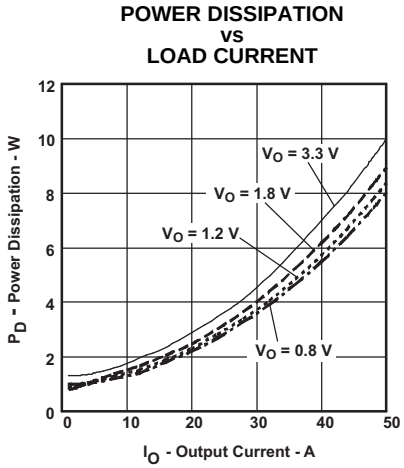


Figure 7.

(3) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6 , and Figure 7.

APPLICATION INFORMATION

Capacitor Recommendations for the PTH12040W Power Module

The PTH12040W is a state-of-the-art multi-phase power converter topology that uses three parallel switching and filter inductor paths between the common input and output filter capacitors. The three paths share the load current, operate at the same frequency, and are evenly displaced in phase.

With multiple switching paths the transient output current capability is significantly increased. This reduces the amount of external output capacitance required to support a load transient. As a further benefit, the ripple current, as seen by the input and output capacitors, is reduced in magnitude and effectively tripled in frequency.

Input Capacitor

The improved transient response of a multi-phase converter places a bigger burden on the transient capability of the input source. The size and value of the input capacitor is therefore determined by this converter's transient performance capability. The minimum amount of input capacitance required is 560 µF, with an RMS ripple current rating of 300 mA. This minimum value assumes that the converter is supplied with a responsive, low inductance input source. This source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes. For high-performance applications, or wherever the transient performance of the input source is limited, 1000 µF of input capacitance is recommended.

Ripple current, less than 100 mΩ of equivalent series resistance (ESR), and temperature are the main considerations when selecting input capacitors. The ripple current reflected from the input of the PTH12040W module is moderate to low. Therefore any good quality, computer-grade electrolytic capacitor, of either value suggested, has an adequate ripple current rating.

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement. When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered. Adding one or two ceramic capacitors to the input reduces high-frequency reflected ripple current.

Output Capacitors

The PTH12040W requires a minimum output capacitance of 660 µF (or 2 × 330 µF), with an ESR of 15 mΩ to 40 mΩ. This is necessary for the stable operation of the regulator. Additional capacitance can be added to improve the module's performance to load transients. High quality computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C. For operation below 0°C, tantalum, ceramic, or OS-CON type capacitors are necessary.

When using a combination of one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 2 mΩ (4 mΩ when calculating using the manufacturer's maximum ESR values). A list of preferred low-ESR type capacitors are identified in Table 1.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitors, with values between 10 µF and 100 µF, does not exceed 400 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum type capacitors are only used on the output bus, and are recommended for applications where the ambient operating temperature is less than 0°C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, many general purpose tantalum capacitors have higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable due to their reduced power dissipation and surge current ratings. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

When specifying OS-CON and polymer-tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

Capacitor Table

Table 1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

Note: This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Designing for Very Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the mnimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

Table 1. Input/Output Capacitors(1)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity		
	Working Voltage (V)	Value (µF)	Max. ESR at 100 kHz (Ω)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus	Vendor Part No.
Panasonic FC (Radial) FK (SMD)	25 25 16 35	1000 560 680 1000	0.043 0.065 0.080 0.060	1690 1205 850 1100	16 × 15 12,5 × 15 10 × 10,2 12,5 × 13,5	1 1 1 1	1 2 1 1	EEUFC1E102S EEUFC1E561S EEVFK1C681P EEVFK1V102Q
United Chemi-Con MVZ(SMD) LXZ, Aluminum (Radial) PS, Poly-Aluminum(Radial) PXA, Poly-Aluminum (SMD)	16 16 25 16 16	470 470 680 330 330	0.090 0.090 0.068 0.014 0.014	670 760 1050 5060 5050	10 × 10 10 × 12,5 10 × 16 10 × 12,5 10 × 12,2	2 2 1 2 2	2 2 1 ≤4 ≤4	MVZ25VC471MJ10TP LXZ16VB471M10X12LL LXZ16VB681M10X16LL 16PS330MJ12 PXA16VC331MJ12TP
Nichicon, Aluminum HD (Radial) PM (Radial)	25 25 35	560 680 560	0.060 0.038 0.048	1060 1430 1360	12,5 × 15 10 × 16 16 × 15	1 1 1	2 1 2	UPM1E561MHH6 UHD1C681MHR UPM1V561MHH6
Panasonic, Poly-Aluminum: SP-Cap	6.3	180	0.005	4100	7,3 × 5,7	N/R(2)	≤5	EEFSE09J181R (V_O ≤ 5.1 V)
Sanyo TPE, Poscap (SMD) SP, OS-CON (Radial) SVP, OS-CON (SMD)	 10 16 16	 330 470 330	 0.025 0.010 0.016	 3000 6000 4700	 7,3 × 5,7 10 × 13 11 × 12	 N/R(2) 3(3) 2	 ≤5 ≤4 ≤4	 10TPE330M 16SEPC470M 16SVP330M
AVX, Tantalum, Series III TPS (SMD)	10 10	470 330	0.045 0.045	1723 1723	7,3 ×5,7 ×4,1	N/R(2) N/R(2)	≤5(4) ≤5(4)	TPSE477M010R0045 (V_O ≤ 5.1 V) TPSE337M010R0045 (V_O ≤ 5.1 V)
Kemet, Poly-Tantalum T520 (SMD) T530 (SMD)	10 10 6.3 4	330 330 470 680	0.040 0.015 0.012 0.005	1800 3800 4200 5000	7,3 ×4,3 ×4,0	N/R(2) N/R(2) N/R(2) N/R(2)	2 ≤4 ≤3(4) ≤2	T520X337M010AS T530X337M010AS T530X477M006AS (V_O ≤ 5.1 V) T530X687M004ASE005 (V_O≤ 3.2V)
Vishay-Sprague 595D, Tantalum (SMD) 94SA, OS-CON (Radial)	 10 16	 470 1000	 0.100 0.015	 1440 9740	 7,2 × 6× 4,1 16 × 25	 N/R(2) 1	 2(4) ≤4	 595D477X0010R2T (V_O ≤ 5.1 V) 94SA108X0016HBP
Kemet, Ceramic X5R (SMD)	16 6.3	10 47	0.002 0.002	–	3225	1(5) N/R(2)	≤8 ≤8	C1210C106M4PAC C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3 6.3 16 16 16	100 47 47 22 10	–	–	3225	N/R(2) N/R(2) 1(5) 1(5) 1(5)	≤4 ≤ 8 ≤ 8 ≤ 8 ≤ 8	GRM32ER60J107M GRM32ER60J476M GRM32ER61C476K GRM32ER61C226K GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3 6.3 16 16	100 47 22 10	–	–	3225	N/R(2) N/R(2) 1(5) 1(5)	≤4 ≤ 8 ≤ 8 ≤ 8	C3225X5R0J107MT C3225X5R0J476MT C3225X5R1C226MT C3225X5R1C106MT

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products. In some instances, the capacitor product life cycle may be in decline and have short-term consideration for obsolescence.
RoHS, Lead-free and Material Details
Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.
(2) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.
(3) Total capacitance of 540 µF is acceptable based on the combined ripple current rating.
(4) The voltage rating of this capacitor only allows it to be used for utput voltages that are equal to or less than 5.1 V.
(5) Small ceramic capacitors may be used to complement electrolytic types at the input to further reduce high-frequency ripple current.

Adjusting the Output Voltage of the PTH12040W Wide-Output Adjust Power Module

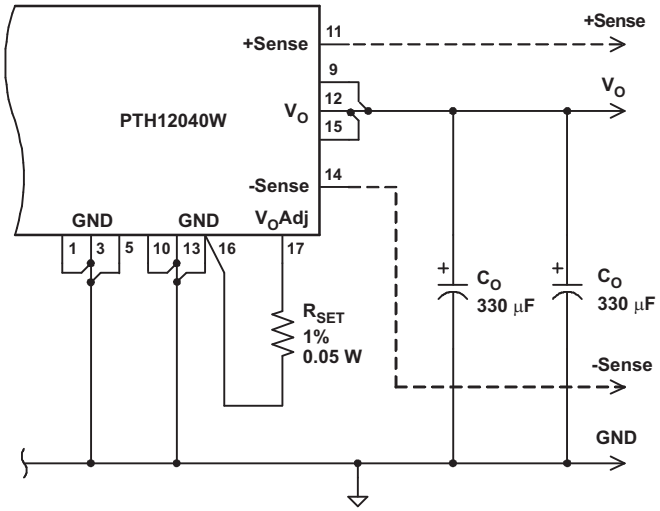
The V_O Adjust control (pin 17) sets the output voltage of the PTH12040W product. The adjustment range is from 0.8 V to 5.5 V. The adjustment method requires the addition of a single external resistor, RSET, that must be connected directly between the V_O Adjust and GND pins 1. Table 2 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides. Figure 8 shows the placement of the required resistor.

For other output voltages, the value of the required resistor can either be calculated, or simply selected from the range of values given in Table 3. The following formula can be used to calculate the adjust resistor value.

$$R_{set} = 10\ k\Omega \times \frac{0.8\ V}{V_O - 0.8\ V} - 1.696\ k\Omega \quad (1)$$

Table 2. Standard Values of R_{SET} for Common Output Voltages

	PTH12040W	
V_O (Required) (V)	R_{SET} (kΩ)	V_O (Actual) (V)
5.0	0.210	5.002
3.3	1.50	3.303
2.5	3.01	2.50
2.0	4.99	1.997
1.8	6.34	1.796
1.5	9.76	1.498
1.2	18.2	1.202
1.0	38.3	1.0
0.8	Open	0.8



(1) A 0.05-W rated resistor may be used. The tolerance should be 1%, and the temperature stability, 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pin 17 and the nearest GND pin (pin 16) using dedicated PCB traces.

(2) Never connect capacitors directly from V_o Adjust to either GND or V_O. Any capacitance added to the V_o Adjust pin affects the stability of the regulator.

Figure 8. V_O Adjust Resistor Placement

Table 3. Output Voltage Set-Point Resistor Values

V_O(V)	R_{SET} (kΩ)	V_O(V)	R_{SET}(kΩ)	V_O(V)	R_{SET}(kΩ)
0.80	Open	1.60	8.3	3.05	1.86
0.825	318	1.65	7.72	3.10	1.78
0.85	158	1.70	7.19	3.15	1.71
0.875	105	1.75	6.73	3.20	1.64
0.90	78.31	1.80	6.3	3.25	1.57
0.925	62.3	1.85	5.92	3.30	1.5
0.95	51.6	1.90	5.58	3.35	1.44
0.975	44	1.95	5.26	3.40	1.38
1.0	38.3	2.0	4.97	3.50	1.27
1.025	33.9	2.05	4.7	3.60	1.16
1.05	30.3	2.10	4.46	3.70	1.06
1.075	27.4	2.15	4.23	3.80	0.971
1.10	25	2.20	4.02	3.90	0.885
1.125	22.9	2.25	3.82	4.0	0.804
1.15	21.2	2.30	3.64	4.10	0.728
1.175	19.6	2.35	3.47	4.20	0.657
1.20	18.3	2.40	3.3	4.30	0.590
1.225	17.1	2.45	3.15	4.40	0.526
1.25	16.1	2.50	3.01	4.50	0.466
1.275	15.1	2.55	2.88	4.60	0.409
1.30	14.3	2.60	2.75	4.70	0.355
1.325	13.5	2.65	2.63	4.80	0.304
1.35	12.8	2.70	2.51	4.90	0.255
1.375	12.2	2.75	2.41	5.0	0.209
1.40	11.6	2.80	2.3	5.10	0.164
1.425	11.1	2.85	2.21	5.20	0.122
1.45	10.6	2.90	2.11	5.30	0.082
1.475	10.2	2.95	2.02	5.40	0.043
1.50	9.73	3.0	1.94	5.50	0
1.55	8.97				

Adjusting the Undervoltage Lockout (UVLO) of the PTH12040W Power Modules

The PTH12040W power modules incorporate an input undervoltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a clean, monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the regulator's input source during the power-up sequence.

The UVLO characteristic is defined by the on-threshold (V_{THD}) and hysterisis (V_{HYS}) voltages. Below the *on* threshold, the Inhibit control is overriden, and the module does not produce an output. The hysterisis voltage is the difference between the *on* and *off* threshold voltages. It ensures a clean power-up, even when the input voltage is rising slowly. The hysterisis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

UVLO Adjustment

The UVLO feature of the PTH12040W module allows for limited adjustment of both the on threshold and hysterisis voltages. The adjustment is made via the *UVLO Prog* control pin. When the UVLO Prog pin is left open circuit, the on threshold and hysterisis voltages are internally set to their default values. The *on* threshold has a nominal voltage of 7.5 V, and the hysterisis 1 V. This ensures that the module produces a regulated output when the minimum input voltage is applied (see specifications). The combination correlates to an *off* threshold of approximately 6.5 V. The adjustments are limited. The on threshold can only be adjusted higher, and the hysterisis voltage can only be reduced in magnitude.

The *on* threshold might need to be raised if the module is powered from a tightly regulated 12-V bus. This would prevent it from operating if the input bus failed to completely rise to its specified regulation voltage. The hysterisis should not be changed unless absolutely necessary. A generous amount of hysterisis ensures that the module exhibits a clean startup. Therefore, adjustment of the hysterisis should only be considered if there is a system requirement to specifically set the off threshold voltage (in addition to the on threshold). Depending on the load regulation of the input source, the hysterisis should not be adjusted below 0.5 V without careful consideration.

Adjustment Method

The resistors, R_{THD} and R_{HYS} (see Figure 9), provide the adjustment of the on-threshold and hysterisis voltages. R_{THD} connects between the UVLO Prog control pin and GND, and R_{HYS} is connected between the UVLO Prog and V_I. R_{THD} alone is used to adjust the on-threshold voltage **higher**. However, to adjust the hystersis to a **lower** value requires **both** the R_{HYS} and R_{THD} resistors to be placed in the circuit.

The recommended adjustment method requires that any change to the hysterisis be determined first. If the hysterisis is changed, then a value for R_{THD} **must** also be calculated. This is irrespective of whether a change is required to the value of V_{THD}. If there is no change to V_{HYS}, then a resistor should not be placed in the R_{HYS} location. R_{HYS} should then be assigned an infinite value for calculating the value of R_{THD}.

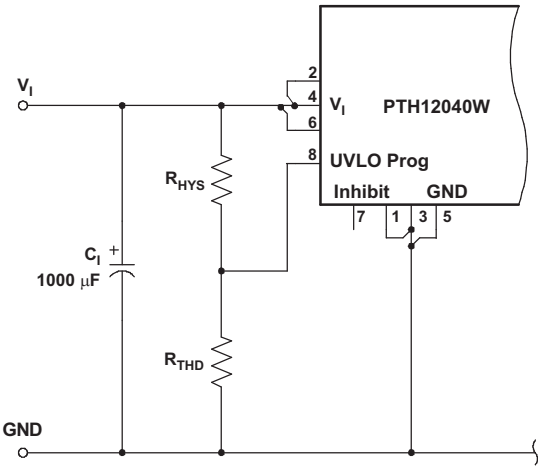


Figure 9. UVLO Program Resistor Placement

Hysterisis Adjust

The hysterisis voltage, $V_{HYS,}$ is the difference between the *on* and *off* threshold values. The default value is 1 V and it can only be adjusted to a lower value.

Caution should be used when changing the hysterisis voltage to a lower value, as it could induce start-up oscillations.

Any change in the hysterisis voltage requires both R_{HYS} and R_{THD} resistors be in place. Adding R_{HYS} alone does not have the desired effect. The value for R_{HYS} must first be calculated using Equation 2. The value identified for R_{HYS} must then be used to determine a value for R_{THD}, using Equation 3.

$$R_{HYS} = \frac{26.1 \times H_{HYS}}{0.365 \times \left(1 - V_{HYS}\right)} \text{ k}\Omega \quad (2)$$

Threshold Adjust

Equation 3 determines the value of R_{THD} required to adjust V_{THD} to a new value. The default value is 7.5 V, and it may only be adjusted to a higher value. If the hysterisis value has been adjusted, then a value for R_{THD} must also be calculated. (This is irrespective of whether V_{THD} is being adjusted.) If there has been no adjustment for the hysterisis voltage, the term $1/R_{HYS}$ in Equation 3, may be assigned the value, *0*.

$$R_{THD} = \frac{39.2 \text{ k}\Omega}{39.2\left[\left(1/R_{HYS} + 0.014\right)\left(V_{THD}/2.5 - 1\right) - 0.0027\right] - 1} \quad (3)$$

Calculated Values

Table 4 shows a matrix of standard resistor values for R_{HYS} and R_{THD}, for different options of the on-threshold (V_{THD}) and hysterisis (V_{HYS}) voltages. For most applications, only the on-threshold voltage should need to be adjusted. In this case select only a value for R_{THD} from far right-hand column.

The hysterisis should only be adjusted if there is a specific requirement to independently adjust the off-threshold, separately from the on-threshold voltage. In this case, a value for both R_{HYS} and R_{THD} must be selected from Table 4. This is irrespective of whether the on-threshold voltage is being adjusted.

Table 4. Calculated Values of R_{HYS} and R_{THD}, for Various Values of V_{HYS} and V_{THD}

	V_{HYS}	0.5 V	0.6 V	0.7 V	0.8 V	0.9 V	1 V (default)
V_{THD} (V)	R_{HYS} (kΩ)	71.5	107	165	287	649.0	N/A
8.0		30.1	43.2	63.4	97.6	169 .0	402.0
8.5		25.5	36.5	51.1	73.2	110.0	187.0
9.0		23.2	30.9	42.2	57.6	82.5	124.0
9.5		20.0	27.4	36.5	48.7	64.9	90.9
10.0	R_{THD} (kΩ)	18.2	24.3	31.6	41.2	54.9	73.2
10.5		16.2	21.5	28.0	36.5	46.4	60.4
11.0		15.0	19.6	25.5	32.4	41.2	52.3
11.5		14.0	18.2	23.2	28.0	36.5	45.3
12.0		12.7	16.5	21.0	26.1	32.4	40.2

Features of the PTH Family of Non-Isolated Wide Output Adjust Power Modules

POLA™ Compatibility

The PTH/PTV family of nonisolated, wide-output adjustable power modules from Texas Instruments are optimized for applications that require a flexible, high performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, non-isolated modules with the same footprint and form factor. POLA parts are also assured to be interoperable, thereby providing customers with second-source availability.

All POLA products include Auto-Track™. This feature was specifically designed to simplify the task of sequencing the supply voltages in a power system. This and other features are described in the following sections.

Soft-Start Power Up

The Auto-Track feature allows the power-up of multiple PTH modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, V_I (see Figure 10).

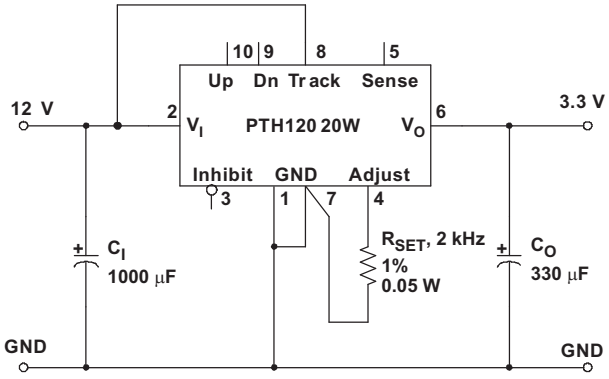


Figure 10. Power-Up Application Circuit

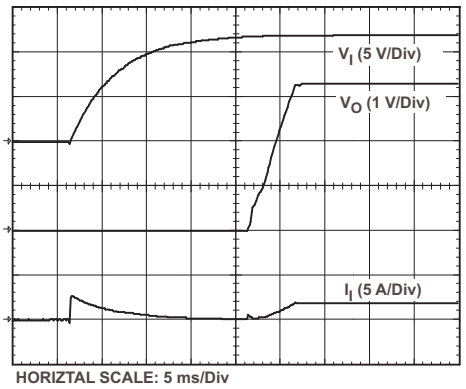


Figure 11. Power-Up Waveforms

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 8 ms–15 ms) before allowing the output voltage to rise.

The output then progressively rises to the module's setpoint voltage. Figure 11 shows the soft-start power-up characteristic of the 18-A output product (PTH12020W), operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 25 ms.

Overtemperature Protection (OTP)

The PTH12020, PTH12030, and PTH12040 products have overtemperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10°C below the trip point.

Note: The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and reduces the long-term reliability of the module. Always operate the regulator within the specified safe operating area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempt to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Output On/Off Inhibit

For applications requiring output voltage on/off control, each series of the PTH family incorporates an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 12 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit input has its own internal pull-up to a potential of 5 V to 13.2 V (see footnotes to electrical characteristics table). The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

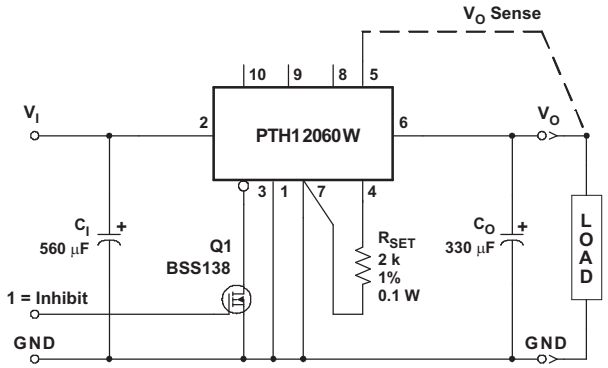


Figure 12. Inhibit Control Circuit

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 25 ms. Figure 13 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1 V_{DS}. The waveforms were measured with a 5-A constant current load.

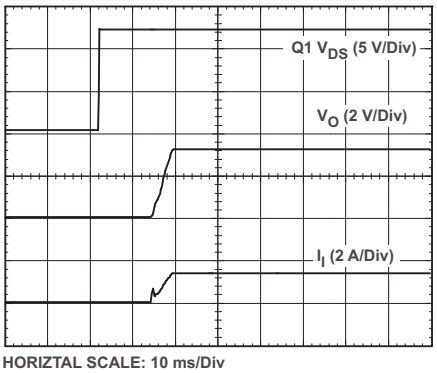


Figure 13. Power-Up from Inhibit Control

Remote Sense

Products with this feature incorporate an output voltage sense pin, V_O Sense. A remote sense improves the load regulation performance of the module by allowing it to compensate for any *IR* voltage drop between its output and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance.

To use this feature simply connect the V_O Sense pin to the V_O node, close to the load circuit. If a sense pin is left open-circuit, an internal low-value resistor (15-Ω or less) connected between the pin and and the output node, ensures the output remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_O and GND pins, and that measured from V_O Sense to GND, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin (1). This control range is limited to between 0 V and the module set-point voltage. Once the Track-pin voltage is raised above the set-point voltage, the module output remains at its set-point (2). As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit (3). For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their Track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 14.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization (4), enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

Figure 14 shows how the TL7712A supply voltage supervisor IC (U3) can be used to coordinate the sequenced power PTH12040W modules. The output of the TL7712A supervisor becomes active above an input voltage of 3.6 V, enabling it to assert a ground signal to the common Track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 28 ms after the input voltage has risen above U3's voltage threshold, which is 10.95 V. The 28-ms time period is controlled by the capacitor C3. The value of 2.2 µF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the Track control voltage is allowed to rise. When U3 removes the ground signal, the Track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

Figure 15 shows the output voltage waveforms from the circuit of Figure 14 after input voltage is applied to the circuit. The waveforms, V_O1 and V_O2, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK}, V_O1, and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common Track control. This pulls the Track inputs to zero volts, forcing the output of each module to follow, as shown in Figure 16. In order for a simultaneous power-down to occur, the Track inputs must be pulled low before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that a valid input voltage is no longer present, their outputs can no longer follow the voltage applied at their Track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the maximum output capacitance and the Auto-Track slew rate.

Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
4. The module cannot follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power has been applied.

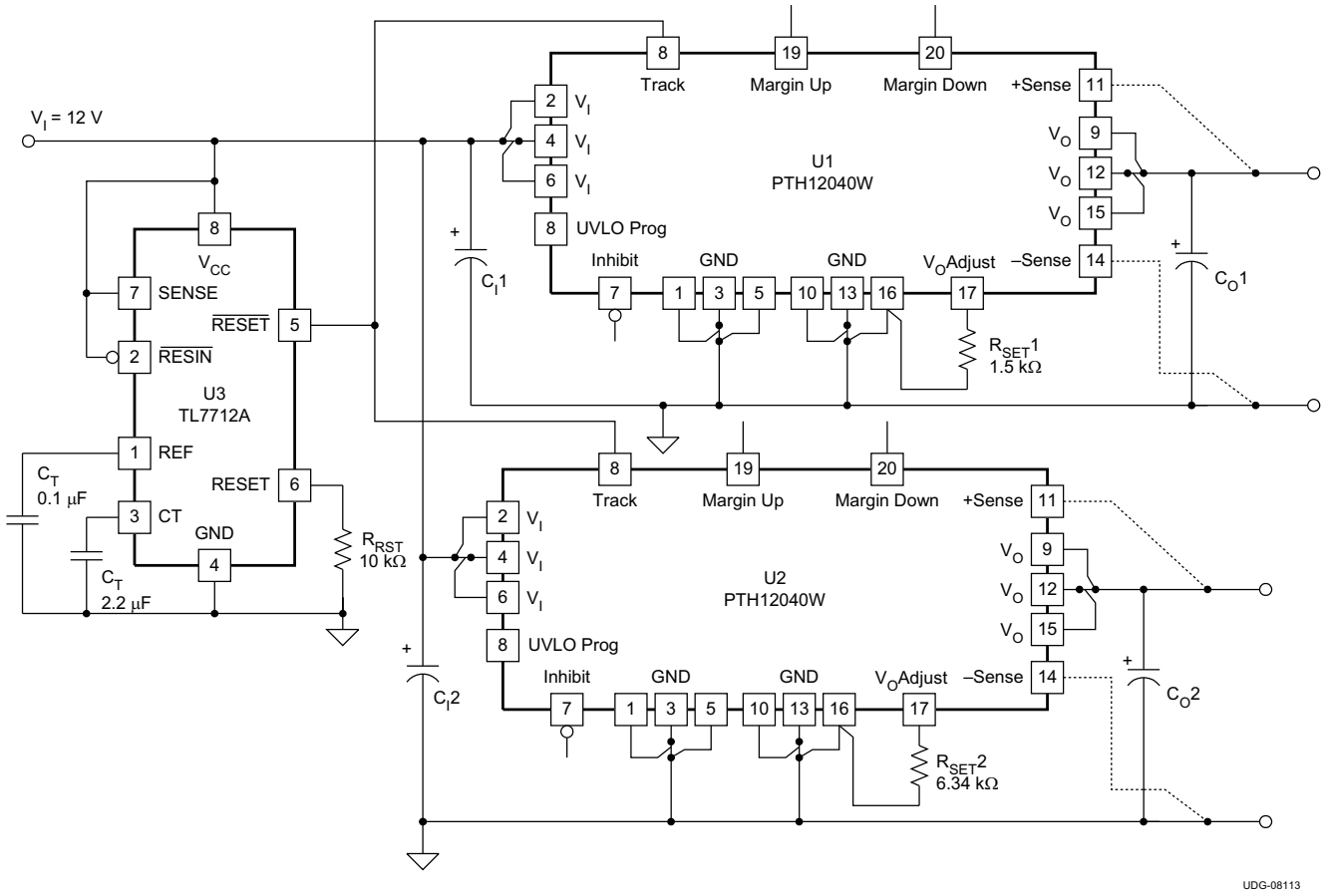


Figure 14. Sequenced Power Up and Power Down Using Auto-Track

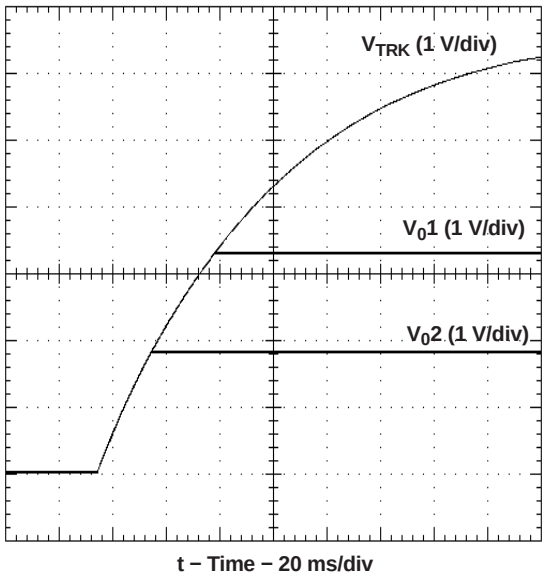


Figure 15. Simultaneous Power Up With Auto-Track Control

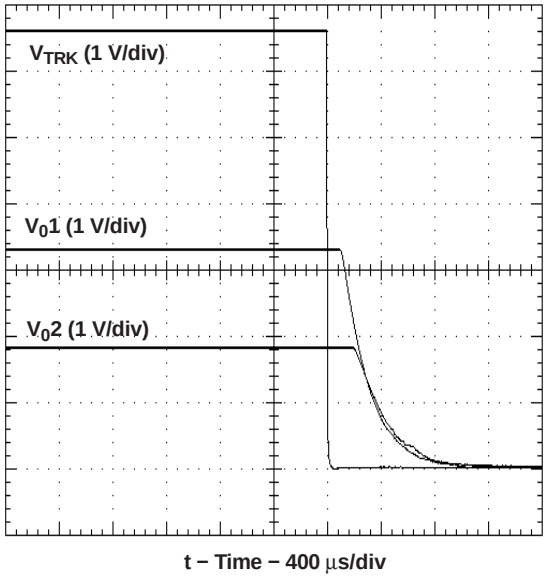


Figure 16. Simultaneous Power Down With Auto-Track Control

Margin Up/Down Controls

The PTH12060, PTH12010, PTH12020, PTH12030, and PTH12040 products incorporate Margin Up and Margin Down control inputs. These controls allow the output voltage to be momentarily adjusted,[1] either up or down, by a nominal 5%. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5% change is applied to the adjusted output voltage, as set by the external resistor, R_{SET} at the V_O Adjust pin.

The 5% adjustment is made by pulling the appropriate margin control input directly to the GND terminal [2]. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose[3]. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs (see R_D and R_U in Figure 17). The value of the resistor can be selected from Table 5, or calculated using Equation 4. For the same amount of adjustment, the resistor value calculated for R_U and R_D is the same.

$$R_U = \left(\left(\frac{499}{\Delta\%}\right) - 99.8\right) k\Omega \quad \text{or} \quad R_D = \left(\left(\frac{499}{\Delta\%}\right) - 99.8\right) k\Omega \tag{4}$$

Where Δ% = The desired amount of margin adjust in percent.

Table 5. Margin Up/Down Resistor Values

PERCENT ADJUST (%)	R_U / R_D(kΩ)
5	0
4	24.9
3	66.5
2	150
1	397

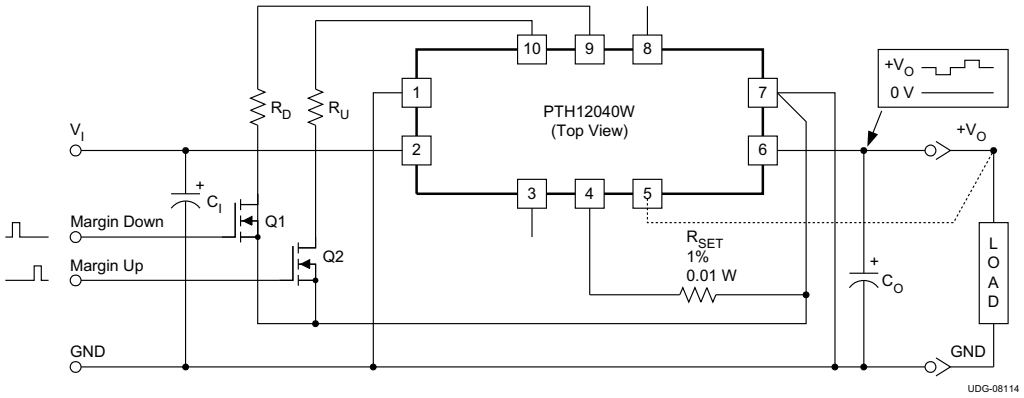


Figure 17. Margin Up/Down Application Schematic

Margin Up/Down Notes

1. The Margin Up and Margin Down controls were not intended to be activated simultaneously. The affects on the output voltage may not completely cancel, resulting in the possibility of a higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module's signal GND (the GND connection recommended for R_{SET}). This produces a more accurate adjustment at the load circuit terminals. The transistors Q1 and Q2 should be located close to the regulator.
3. The Margin Up and Margin Down control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

Prebias Startup Capability

The capability to start up into an output prebias condition is available to all the 12-V input series of PTH/PTV power modules. A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The 12-V input PTH modules all incorporate synchronous rectifiers, but do not sink current during startup, or whenever the Inhibit pin is held low. Start up includes an initial delay (approximately 8–15 ms), followed by the rise of the output voltage under the control of the module's internal soft-start mechanism; see Figure 18.

Conditions for PreBias Holdoff

For the module to allow an output prebias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a prebias voltage when the Inhibit pin is held low, and whenver the output is allowed to rise under soft-start control. Power up under soft-start control occurs upon the removal of the ground signal to the Inhibit pin (with input voltage applied), or when input power is applied with Auto-Track disabled[1]. To further ensure that the regulator doesn't sink output current, (even with a ground signal applied to its Inhibit), the input voltage must always be greater than the applied prebias source. This condition must exist throughout the power-up sequence.

The soft-start period is complete when the output begins rising above the prebias voltage. Once it is complete the module functions as normal, and sinks current if a voltage higher than the nominal regulation value is applied to its output.

Note: If a prebias condition is not present, the soft-start period is complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module's Track control pin, whichever is lowest.

Demonstration Circuit

Figure 19 shows the startup waveforms for the demonstration circuit shown in Figure 20. The initial rise in V_O2 is the prebias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the PTH12010L module (I_O2) is negligible until its output voltage rises above the applied pre-bias.

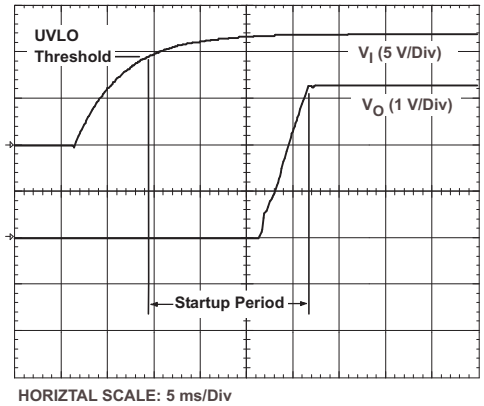


Figure 18. PTH12020W Startup

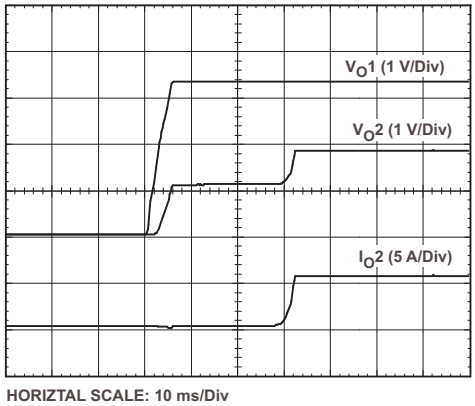


Figure 19. Pre-Bias Startup Waveforms

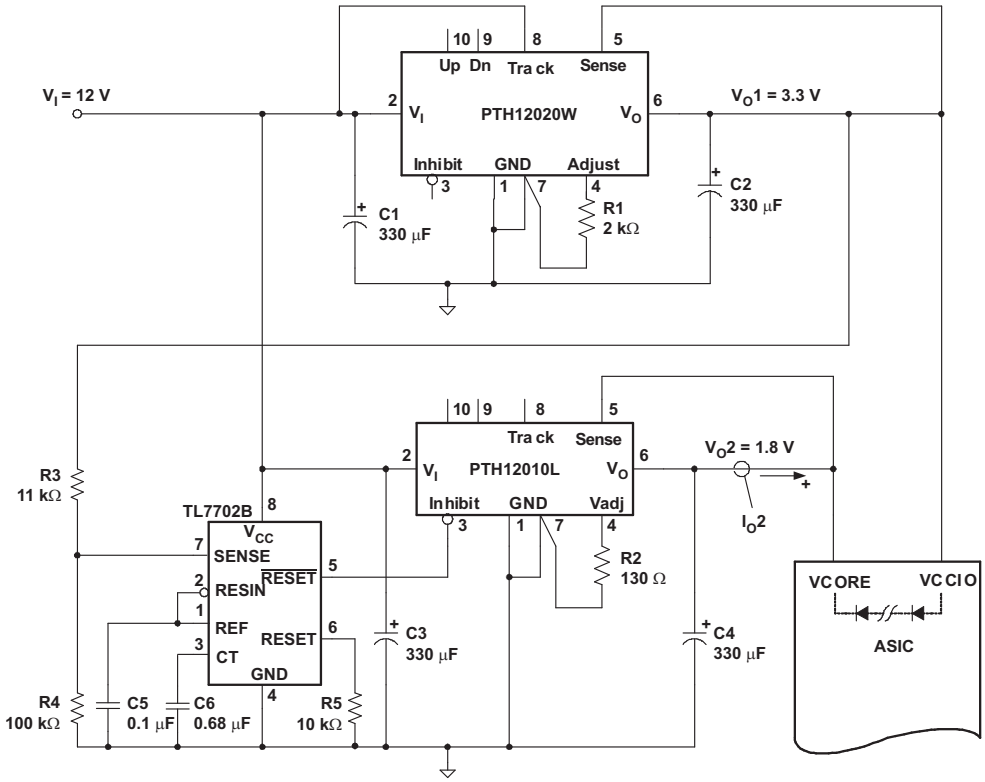


Figure 20. Application Circuit Demonstrating Prebias Startup

Note

1. The prebias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the voltage applied to the Track control pin, the output sinks current during the period that the Track control voltage is below that of the back-feeding source. For this reason, it is recommended that Auto-Track be disabled when not being used. This is accomplished by connecting the Track pin to the input voltage, V_I. This raises the Track pin voltage well above the set-point voltage prior to the module's start up, thereby defeating the Auto-Track feature.

PACKAGING INFORMATION

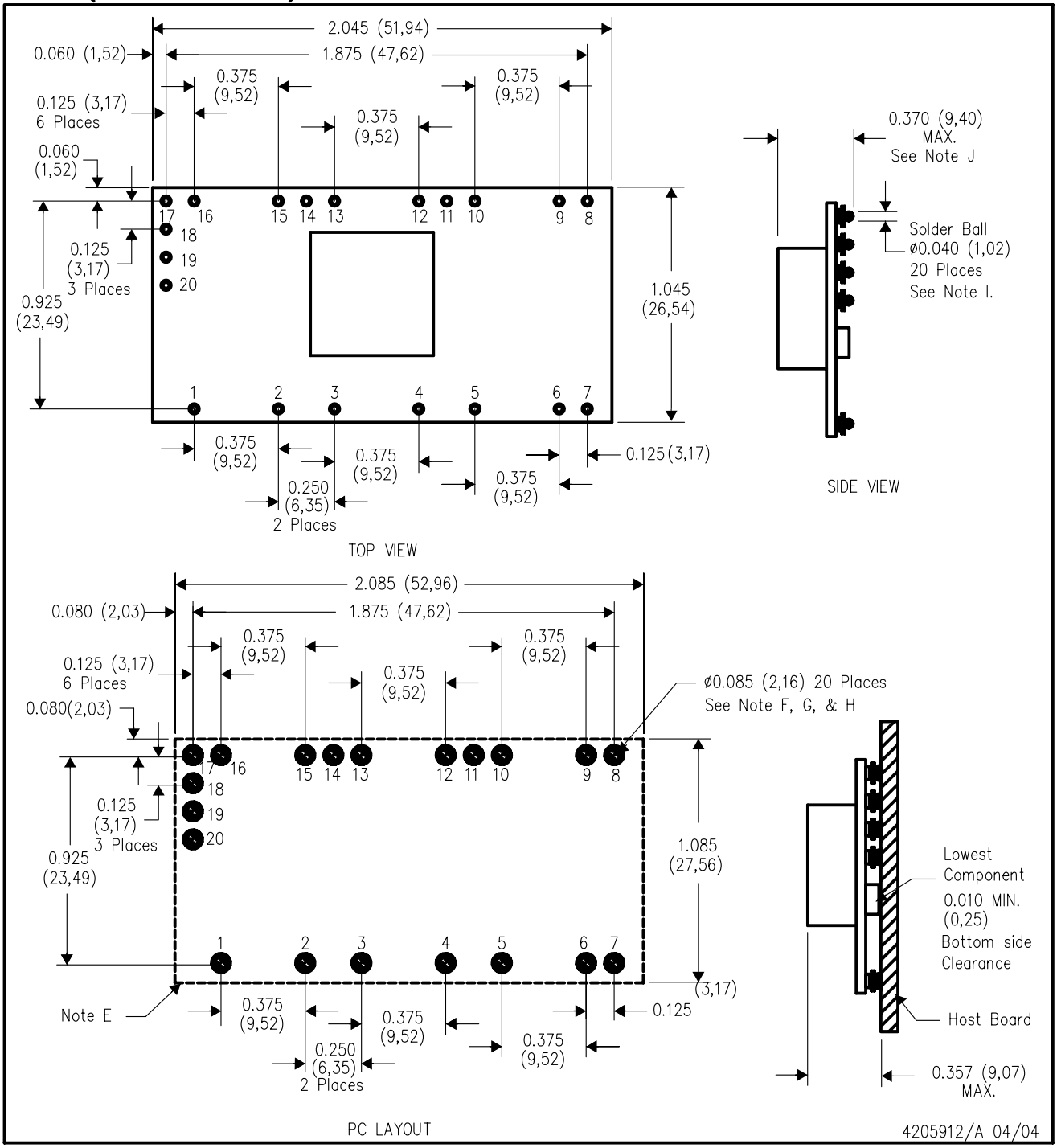
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PTH12040WAD	ACTIVE	DIP MOD ULE	EVF	20	12	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTH12040WAH	ACTIVE	DIP MOD ULE	EVF	20	12	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PTH12040WAS	ACTIVE	DIP MOD ULE	EVG	20	12	TBD	Call TI	Level-1-235C-UNLIM/ Level-3-260C-168HRS
PTH12040WAZ	ACTIVE	DIP MOD ULE	EVG	20	12	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

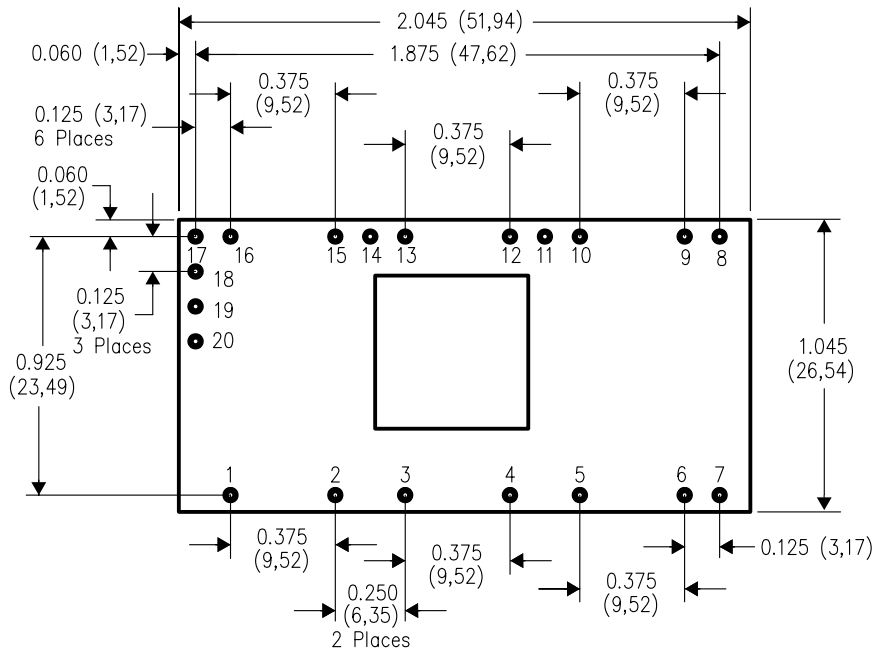
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

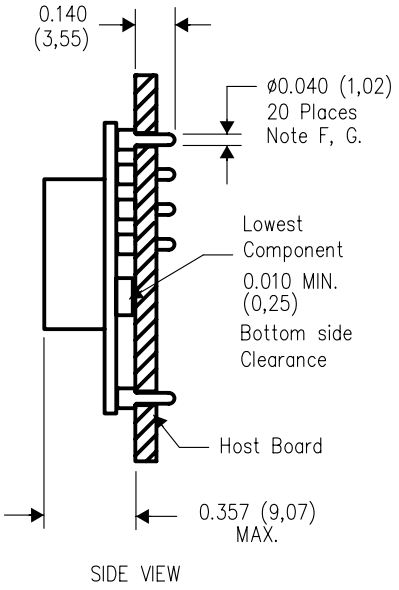
EVG (R–PDSS–T20) DOUBLE SIDED MODULE

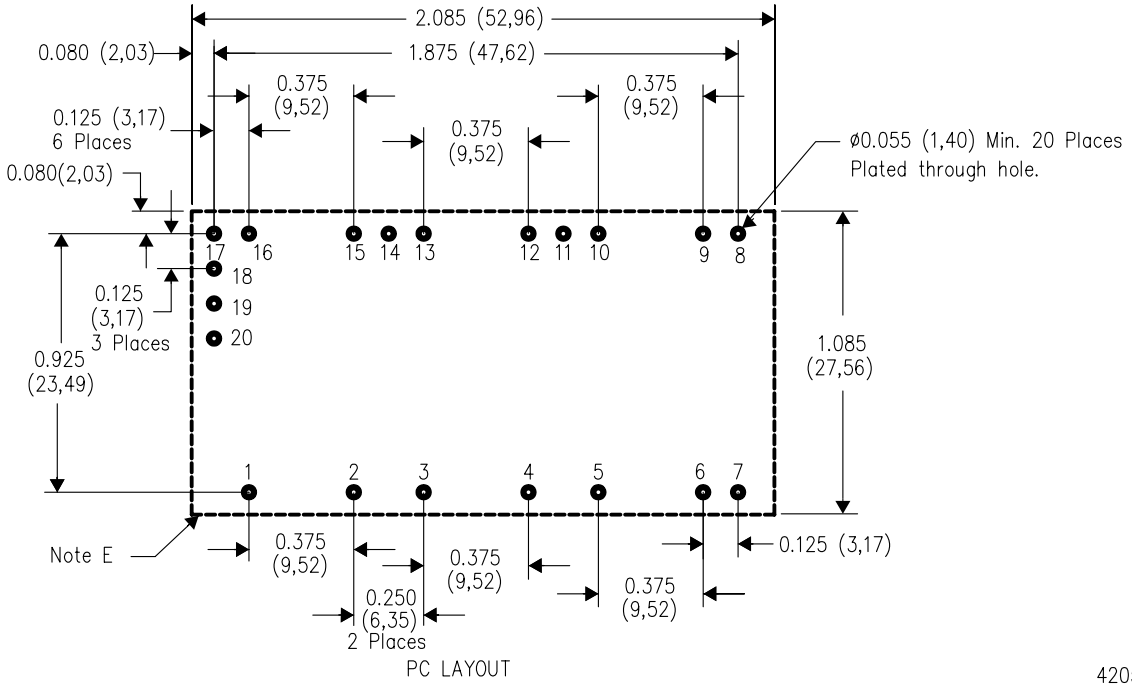


NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

EVF (R–PDSS–T20) DOUBLE SIDED MODULE







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NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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