

12-Bit Octal-Channel ADC Family Up to 65MSPS

Check for Samples: [ADS5281](#), [ADS5282](#)

FEATURES

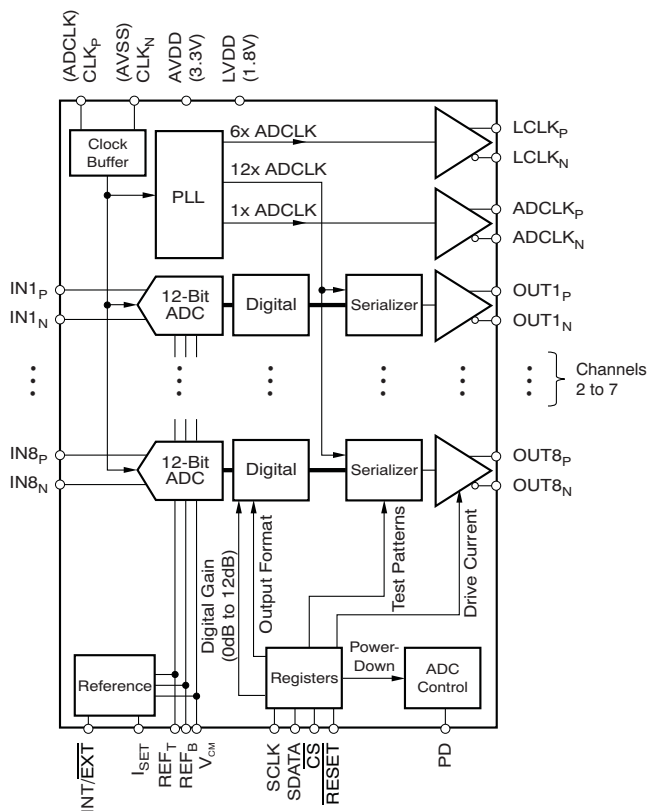
- **Speed and Resolution Grades:**
 - **ADS5281: 12-bit, 50MSPS**
 - **ADS5282: 12-bit, 65MSPS**
- **Power Dissipation:**
 - **48mW/Channel at 30MSPS**
 - **55mW/Channel at 40MSPS**
 - **64mW/Channel at 50MSPS**
 - **77mW/Channel at 65MSPS**
- **70dBFS SNR at 10MHz IF**
- **Analog Input Full-Scale Range: $2V_{PP}$**
- **Low-Frequency Noise Suppression Mode**
- **6dB Overload Recovery In One Clock**
- **External and Internal (Trimmed) Reference**
- **3.3V Analog Supply, 1.8V Digital Supply**
- **Single-Ended or Differential Clock:**
 - **Clock Duty Cycle Correction Circuit (DCC)**
- **Programmable Digital Gain: 0dB to 12dB**
- **Serialized DDR LVDS Output**
- **Programmable LVDS Current Drive, Internal Termination**
- **Test Patterns for Enabling Output Capture**
- **Straight Offset Binary or Two's Complement Output**
- **Package Options:**
 - **9mm × 9mm QFN-64**
 - **HTQFP-80 PowerPAD™ Compatible with [ADS527x](#) Family**

APPLICATIONS

- **Medical Imaging**
- **Wireless Base-Station Infrastructure**
- **Test and Measurement Instrumentation**

DESCRIPTION

The ADS528x is a family of high-performance, low-power, octal channel analog-to-digital converters (ADCs). Available in either a 9mm × 9mm QFN package or an HTQFP-80 package, with serialized low-voltage differential signaling (LVDS) outputs and a wide variety of programmable features, the ADS528x is highly customizable for a diversity of applications and offers an unprecedented level of system integration. An application note, XAPP774 (available at www.xilinx.com), describes how to interface the serial LVDS outputs of TI's ADCs to Xilinx® field-programmable gate arrays (FPGAs). The ADS528x family is specified over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RELATED PRODUCTS

MODEL	RESOLUTION (BITS)	SAMPLE RATE (MSPS)	CHANNELS
ADS5281	12	50	8
ADS5282	12	65	8
ADS5287	10	65	8
ADS5270	12	40	8
ADS5271	12	50	8
ADS5272	12	65	8
ADS5273	12	70	8
ADS5242	12	65	4

Table 1. ORDERING INFORMATION^{(1) (2)}

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY ⁽³⁾
ADS5281	HTQFP-80 (PowerPAD)	PFP	–40°C to +85°C	ADS5281I	ADS5281IPFP	Tray
					ADS5281PFPR	Tape and Reel
	QFN-64	RGC		AZ5281	ADS5281IRGCT	Tape and Reel
					ADS5281IRGCR	Tape and Reel
ADS5282	QFN-64	RGC	–40°C to +85°C	AZ5282	ADS5282IRGCT	Tape and Reel
					ADS5282IRGCR	Tape and Reel

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) These devices meet the following planned eco-friendly classification:
Green (RoHS and No Sb/Br): Texas Instruments defines *Green* to mean Pb-free (RoHS compatible) and free of bromine (Br)- and antimony (Sb)-based flame retardants. Refer to the [Quality and Lead-Free \(Pb-Free\) Data](#) web site for more information. These devices have a Cu NiPdAu lead/ball finish.
- (3) Refer to the Package Option Addendum at the end of this document for specific transport media and quantity information.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

	ADS528x	UNIT
Supply voltage range, AVDD	–0.3 to +3.9	V
Supply voltage range, LVDD	–0.3 to +2.2	V
Voltage between AVSS and LVSS	–0.3 to +0.3	V
External voltage applied to REF _T pin	–0.3 to +3	V
External voltage applied to REF _B pin	–0.3 to +2	V
Voltage applied to analog input pins	–0.3 to minimum [3.6, (AVDD + 0.3)]	V
Voltage applied to digital input pins	–0.3 to minimum [3.9, (AVDD + 0.3)]	V
Peak solder temperature	+260	°C
Junction temperature	+125	°C
Storage temperature range	–65 to +150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to *absolute maximum conditions* for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

PARAMETER		ADS528x			UNIT
		MIN	TYP	MAX	
SUPPLIES, ANALOG INPUTS, AND REFERENCE VOLTAGES					
AVDD	Analog supply voltage	3.0	3.3	3.6	V
LVDD	Digital supply voltage	1.7	1.8	1.9	V
	Differential input voltage range		2		V _{PP}
	Input common-mode voltage		V _{CM} ± 0.05		V
REF _T	External reference mode		2.5		V
REF _B	External reference mode		0.5		V
CLOCK INPUTS					
	ADCLK input sample rate 1/ t _C	10		50, 65	MSPS
	Input clock amplitude differential (V _{CLKP} –V _{CLKN}) peak-to-peak				
	Sine wave, ac-coupled		3.0		V _{PP}
	LVPECL, ac-coupled		1.6		V _{PP}
	LVDS, ac-coupled		0.7		V _{PP}
	Input clock CMOS, single-ended (V _{CLKP})				
	V _{IL}			0.6	V
	V _{IH}	2.2			V
	Input clock duty cycle		50		%
DIGITAL OUTPUTS					
	ADCLK _P and ADCLK _N outputs (LVDS)	10	1x (sample rate)	50, 65	MHz
	LCLK _P and LCLK _N outputs (LVDS)	60	6x (sample rate)	300, 390	MHz
C _{LOAD}	Maximum external capacitance from each pin to LVSS		5		pF
R _{LOAD}	Differential load resistance between the LVDS output pairs		100		Ω
T _A	Operating free-air temperature	–40		+85	°C

(1) All conditions are common to the ADS528x family.

INITIALIZATION REGISTERS

After the device has been powered up, the following registers must be written to (in the exact order listed below) through the serial interface as part of an initialization sequence.⁽¹⁾

	ADDRESS (hex)	DATA (hex)
Initialization Register 1 ⁽¹⁾	03	0002
Initialization Register 2 ⁽¹⁾	01	0010
Initialization Register 3 ⁽¹⁾	C7	8001
Initialization Register 4 ⁽¹⁾	DE	01C0

(1) It is no longer necessary to write these initialization registers. However, customers who have already included them in their software can continue to use them. Programming these registers does not affect device performance.

If the analog input is ac-coupled, the following registers must be written to in the order listed below.

	ADDRESS (hex)	DATA (hex)
Initialization Register 1	01	0010
Initialization Register 5	E2	00C0

To disable the PLL configuration switching (especially useful in systems where a system-level timing calibration is done once after power-up), the following registers must be written to in the order listed below. Also, see section [PLL Operation Across Sampling Frequency](#).

	ADDRESS (hex)	DATA (hex)
For 10 ≤ F _s ≤ 25 ⁽¹⁾	E3	0060
For 15 ≤ F _s ≤ 45 ⁽¹⁾	E3	00A0

(1) where F_s = sampling clock frequency

DIGITAL CHARACTERISTICS

DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. At $C_{LOAD} = 5\text{pF}^{(1)}$, $I_{OUT} = 3.5\text{mA}^{(2)}$, $R_{LOAD} = 100\Omega^{(2)}$, and no internal termination, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS528x			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS					
High-level input voltage		1.4			V
Low-level input voltage				0.3	V
High-level input current			33		μA
Low-level input current			−33		μA
Input capacitance			3		pF
LVDS OUTPUTS					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, V _{OD}			350		mV
V _{OS} output offset voltage	Common-mode voltage of OUT _P and OUT _N		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.

(2) I_{OUT} refers to the LVDS buffer current setting; R_{LOAD} is the differential load resistance between the LVDS output pair.

ELECTRICAL CHARACTERISTICS⁽¹⁾

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = +85^{\circ}\text{C}$, $AVDD = 3.3\text{V}$, $LVDD = 1.8\text{V}$, clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, I_{SET} resistor = 56.2k Ω , and LVDS buffer current setting = 3.5mA, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS528x			UNIT
			MIN	TYP	MAX	
INTERNAL REFERENCE VOLTAGES						
V _{REFB}	Reference bottom			0.5	V	
V _{REFT}	Reference top			2.5	V	
	V _{REFT} – V _{REFB}	1.95	2.0	2.05	V	
V _{CM}	Common-mode voltage (internal)	1.425	1.5	1.575	V	
	V _{CM} output current		±2		mA	
EXTERNAL REFERENCE VOLTAGES						
V _{REFB}	Reference bottom	0.4	0.5	0.6	V	
V _{REFT}	Reference top	2.4	2.5	2.6	V	
	V _{REFT} – V _{REFB}	1.9	2.0	2.1	V	
ANALOG INPUT						
	Differential input voltage range		2.0		V _{PP}	
	Differential input capacitance		3		pF	
	Analog input bandwidth		520		MHz	
	Analog input common-mode range	DC-coupled input		V _{CM} ± 0.05	V	
	Analog input common-mode current	Per input pin per MSPS of sampling speed	2.5		µA/MHz per pin	
	Voltage overload recovery time	Recovery from 6dB overload to within 1% accuracy	1		Clock cycle	
	Voltage overload recovery repeatability	Standard deviation seen on a periodic first data within full-scale range in a 6dB overloaded sine wave	1		LSB	
DC ACCURACY						
	Offset error		–1.25	±0.2	+1.25	%FS
	Offset error temperature coefficient ⁽²⁾			±5		ppm/°C
	Channel gain error	Excludes error in internal reference		–0.8		%FS
	Channel gain error temperature coefficient	Excludes temperature coefficient of internal reference		±10		ppm/°C
	Internal reference error temperature coefficient ⁽³⁾			±15		ppm/°C
DC PSRR	DC power-supply rejection ratio ⁽⁴⁾			1.5		mV/V
POWER-DOWN MODES						
	Power in complete power-down mode			45		mW
	Power in partial power-down mode	Clock at 65MSPS		135		mW
	Power with no clock			88		mW
DYNAMIC PERFORMANCE						
	Crosstalk	5MHz full-scale signal applied to seven channels, measurement taken on channel with no input signal		–90		dBc
	Two-tone, third-order intermodulation distortion	f ₁ = 9.5MHz at –7dBFs f ₂ = 10.2MHz at –7dBFs		–92		dBFS

(1) All characteristics are common for the ADS528x family.

(2) The offset temperature coefficient in ppm/ $^{\circ}\text{C}$ is defined as $(O_1 - O_2) \times 10^6 / (T_1 - T_2) / 4096$, where O_1 and O_2 are the offset codes in LSB at the two extreme temperatures, T_1 and T_2 .

(3) The internal reference temperature coefficient is defined as $(REF_1 - REF_2) \times 10^6 / (T_1 - T_2) / 2$, where REF_1 and REF_2 are the internal reference voltages ($V_{REFT} - V_{REFB}$) at the two extreme temperatures, T_1 and T_2 .

(4) DC PSRR is defined as the ratio of the change in the ADC output (expressed in mV) to the change in supply voltage (in volts).

ELECTRICAL CHARACTERISTICS (BY DEVICE)⁽¹⁾

Typical values at +25°C. Minimum and maximum values are measured across the specified temperature range of $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = +85^{\circ}\text{C}$, AVDD = 3.3V, LVDD = 1.8V, clock frequency = 10MSPS to 65MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, I_{SET} resistor = 56.2k Ω , and LVDS buffer current setting = 3.5mA, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5281 HTQFP-80 50MSPS			ADS5281 QFN-64 50MSPS			ADS5282 QFN-64 65MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY												
No missing codes			Assured			Assured			Assured			
DNL	Differential nonlinearity		−0.75	±0.25	+0.75	−0.75	±0.25	+0.75	−0.9	±0.3	+0.9	LSB
INL	Integral nonlinearity		−1.5	±0.7	+1.5	−1.5	±0.7	+1.5	−1.7	±0.7	+1.7	LSB
POWER SUPPLY—INTERNAL REFERENCE MODE												
IAVDD	Analog supply current			119	145		119	145		145	170	mA
ILVDD	Digital current	Zero input to all channels		76	95		76	95		89	102	mA
Total power				530	649.5		530	649.5		639	744.6	mW
Incremental power saving		Obtained on powering down one channel at a time		51			51			63		mW
POWER SUPPLY—EXTERNAL REFERENCE MODE												
IAVDD	Analog supply current			113			113			138		mA
ILVDD	Digital current	Zero input to all channels		76			76			89		mA
Total power				510			510			616		mW
Incremental power saving		Obtained on powering down one channel at a time		50			50			61		mW
EXTERNAL REFERENCE LOADING												
Switching current		Current drawn by the eight ADCs from the external reference voltages; sourcing for REF _T , sinking for REF _B .		2.5			2.5			3.5		mA
DYNAMIC CHARACTERISTICS												
SFDR	Spurious-free dynamic range	f _{IN} = 5MHz, single-ended clock	74	85		74	85		72	85		dBc
		f _{IN} = 30MHz, differential clock		80			80			80		dBc
HD2	Magnitude of second harmonic	f _{IN} = 5MHz, single-ended clock	74	85		74	85		72	85		dBc
		f _{IN} = 30MHz, differential clock		82			82			82		dBc
HD3	Magnitude of third harmonic	f _{IN} = 5MHz, single-ended clock	74	85		74	85		72	85		dBc
		f _{IN} = 30MHz, differential clock		80			80			80		dBc
THD	Total harmonic distortion	f _{IN} = 5MHz, single-ended clock	71	80		71	80		70	80		
		f _{IN} = 30MHz, differential clock		78			78			78		
SNR	Signal-to-noise ratio	f _{IN} = 5MHz, single-ended clock	68.3	70		68.3	70		68.3	70		dBFS
		f _{IN} = 30MHz, differential clock		69.8			69.8			69.8		dBFS
SINAD	Signal-to-noise and distortion	f _{IN} = 5MHz, single-ended clock	67.7	69.7		67.7	69.7		67.3	69.7		dBFS
		f _{IN} = 30MHz, differential clock		69.5			69.5			69.5		dBFS

(1) All characteristics are specific to each grade.

PIN CONFIGURATIONS

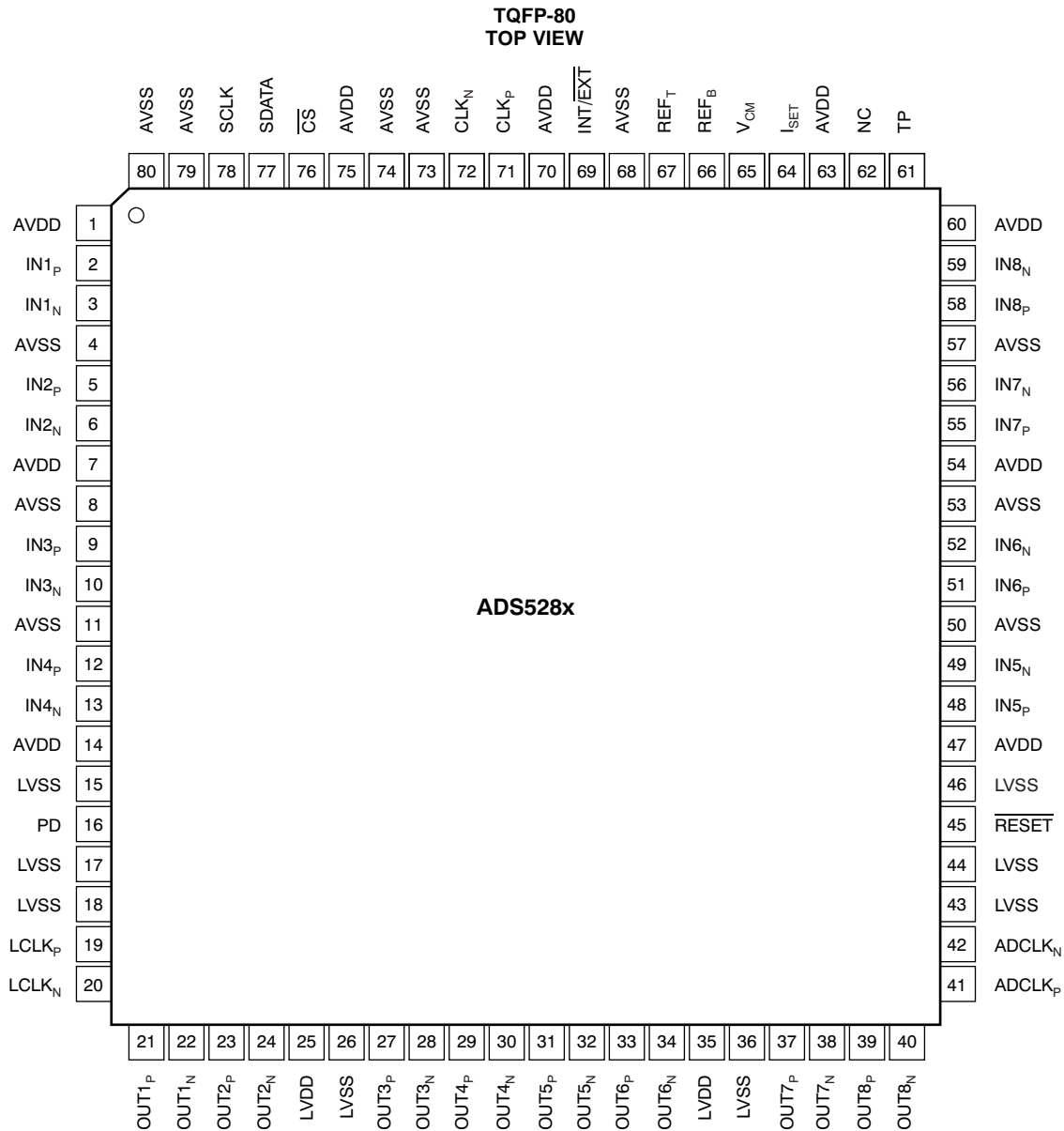


Table 2. PIN DESCRIPTIONS: TQFP-80

PIN NAME	DESCRIPTION	PIN NUMBER	# OF PINS
ADCLK _N	LVDS frame clock (1X)—negative output	42	1
ADCLK _P	LVDS frame clock (1X)—positive output	41	1
AVDD	Analog power supply, 3.3V	1, 7, 14, 47, 54, 60, 63, 70, 75	9
AVSS	Analog ground	4, 8, 11, 50, 53, 57, 68, 73, 74, 79, 80	11
CLK _N	Negative differential clock Tie CLK _N to 0V for a single-ended clock	72	1
CLK _P	Positive differential clock	71	1
CS	Serial enable chip select—active low digital input	76	1
IN1 _N	Negative differential input signal, channel 1	3	1
IN1 _P	Positive differential input signal, channel 1	2	1
IN2 _N	Negative differential input signal, channel 2	6	1

Table 2. PIN DESCRIPTIONS: TQFP-80 (continued)

PIN NAME	DESCRIPTION	PIN NUMBER	# OF PINS
IN2 _P	Positive differential input signal, channel 2	5	1
IN3 _N	Negative differential input signal, channel 3	10	1
IN3 _P	Positive differential input signal, channel 3	9	1
IN4 _N	Negative differential input signal, channel 4	13	1
IN4 _P	Positive differential input signal, channel 4	12	1
IN5 _N	Negative differential input signal, channel 5	49	1
IN5 _P	Positive differential input signal, channel 5	48	1
IN6 _N	Negative differential input signal, channel 6	52	1
IN6 _P	Positive differential input signal, channel 6	51	1
IN7 _N	Negative differential input signal, channel 7	56	1
IN7 _P	Positive differential input signal, channel 7	55	1
IN8 _N	Negative differential input signal, channel 8	59	1
IN8 _P	Positive differential input signal, channel 8	58	1
INT/EXT	Internal/external reference mode select input	69	1
I _{SET}	Bias pin—56.2kΩ to ground	64	1
LCLK _N	LVDS bit clock (6X)—negative output	20	1
LCLK _P	LVDS bit clock (6X)—positive output	19	1
LVDD	Digital and I/O power supply, 1.8V	25, 35	2
LVSS	Digital ground	15, 17, 18, 26, 36, 43, 44, 46	8
NC	No connection (or connect to ground)	62	1
OUT1 _N	LVDS channel 1—negative output	22	1
OUT1 _P	LVDS channel 1—positive output	21	1
OUT2 _N	LVDS channel 2—negative output	24	1
OUT2 _P	LVDS channel 2—positive output	23	1
OUT3 _N	LVDS channel 3—negative output	28	1
OUT3 _P	LVDS channel 3—positive output	27	1
OUT4 _N	LVDS channel 4—negative output	30	1
OUT4 _P	LVDS channel 4—positive output	29	1
OUT5 _N	LVDS channel 5—negative output	32	1
OUT5 _P	LVDS channel 5—positive output	31	1
OUT6 _N	LVDS channel 6—negative output	34	1
OUT6 _P	LVDS channel 6—positive output	33	1
OUT7 _N	LVDS channel 7—negative output	38	1
OUT7 _P	LVDS channel 7—positive output	37	1
OUT8 _N	LVDS channel 8—negative output	40	1
OUT8 _P	LVDS channel 8—positive output	39	1
PD	Power-down input	16	1
REF _B	Negative reference input/output	66	1
REF _T	Positive reference input/output	67	1
RESET	Active low RESET input	45	1
SCLK	Serial clock input	78	1
SDATA	Serial data input	77	1
TP	Test pin, do not use	61	1
V _{CM}	Common-mode output pin, 1.5V output	65	1

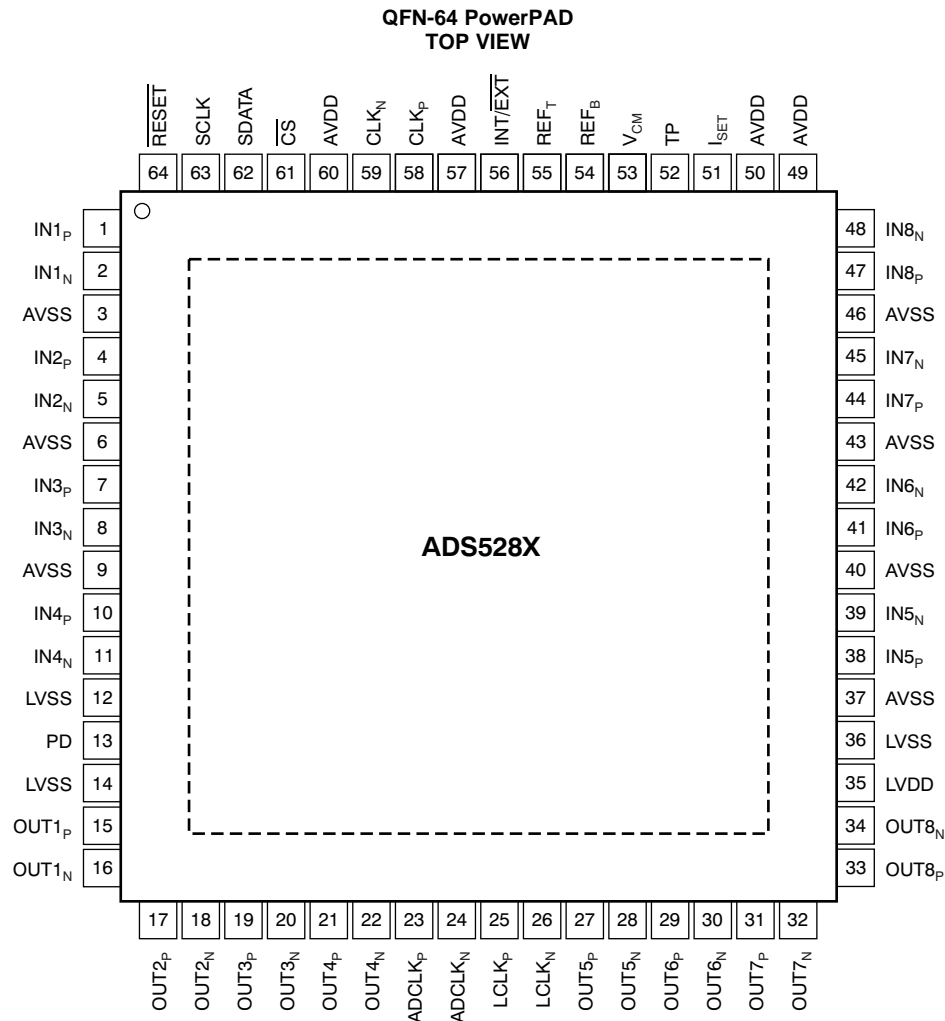
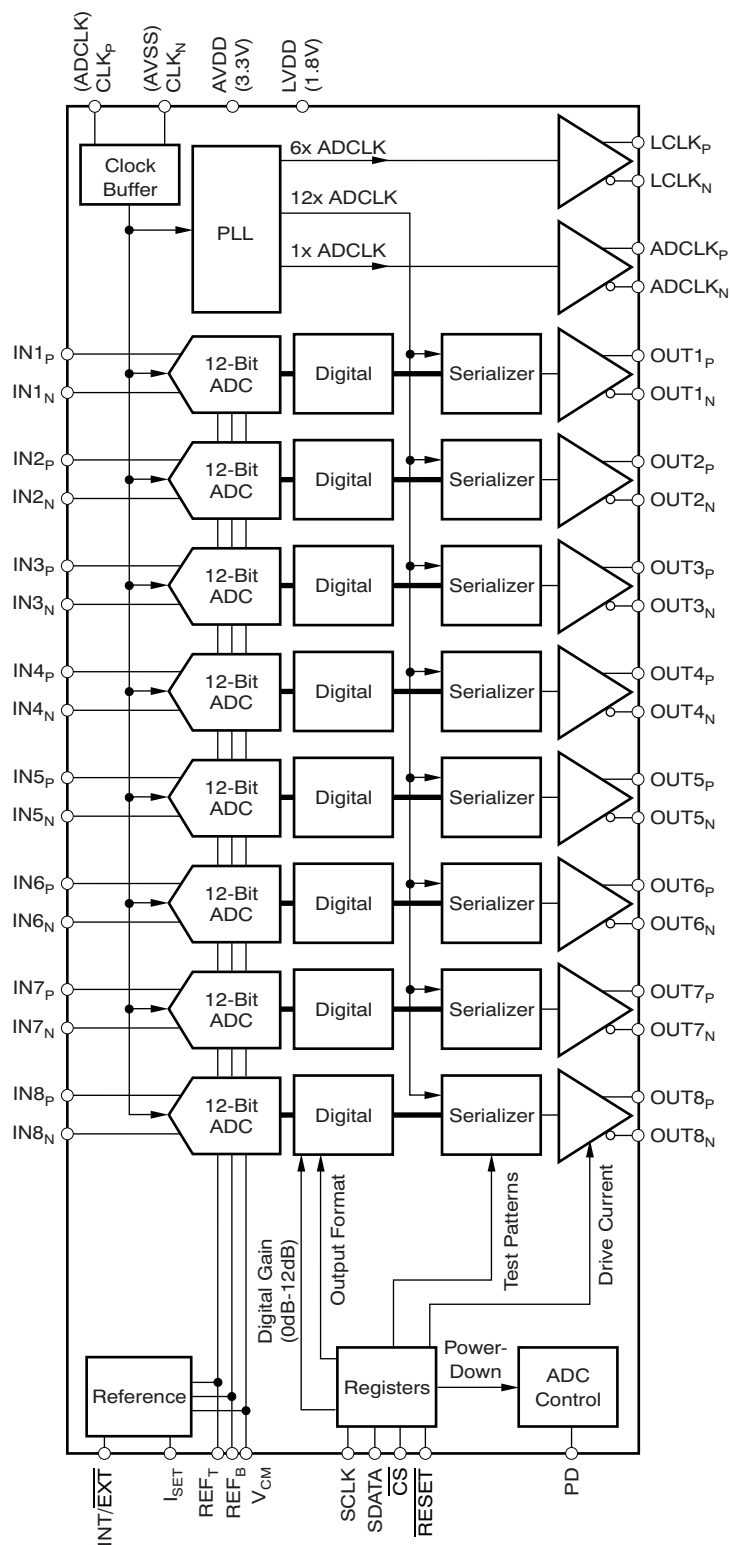


Table 3. PIN DESCRIPTIONS: QFN-64

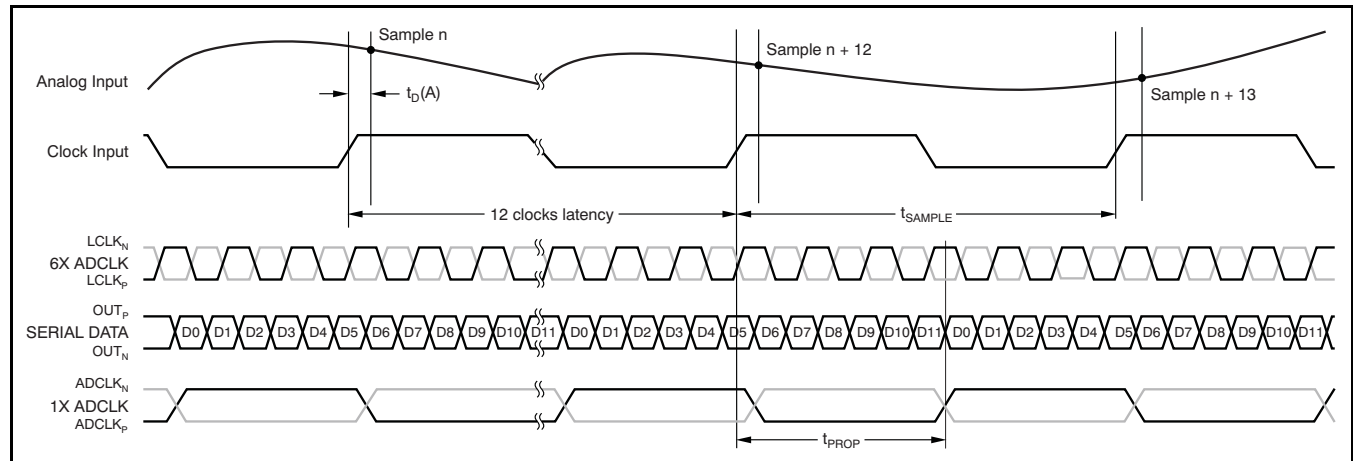
PIN NAME	DESCRIPTION	PIN NUMBER	# OF PINS
ADCLK _N	LVDS frame clock (1X)—negative output	24	1
ADCLK _P	LVDS frame clock (1X)—positive output	23	1
AVDD	Analog power supply, 3.3V	49, 50, 57, 60	4
AVSS	Analog ground	3, 6, 9, 37, 40, 43, 46	7
CLK _N	Negative differential clock input Tie CLK _N to 0V for a single-ended clock	59	1
CLK _P	Positive differential clock input	58	1
$\overline{\text{CS}}$	Serial enable chip select—active low digital input	61	1
IN1 _N	Negative differential input signal, channel 1	2	1
IN1 _P	Positive differential input signal, channel 1	1	1
IN2 _N	Negative differential input signal, channel 2	5	1
IN2 _P	Positive differential input signal, channel 2	4	1
IN3 _N	Negative differential input signal, channel 3	8	1
IN3 _P	Positive differential input signal, channel 3	7	1
IN4 _N	Negative differential input signal, channel 4	11	1
IN4 _P	Positive differential input signal, channel 4	10	1
IN5 _N	Negative differential input signal, channel 5	39	1

Table 3. PIN DESCRIPTIONS: QFN-64 (continued)

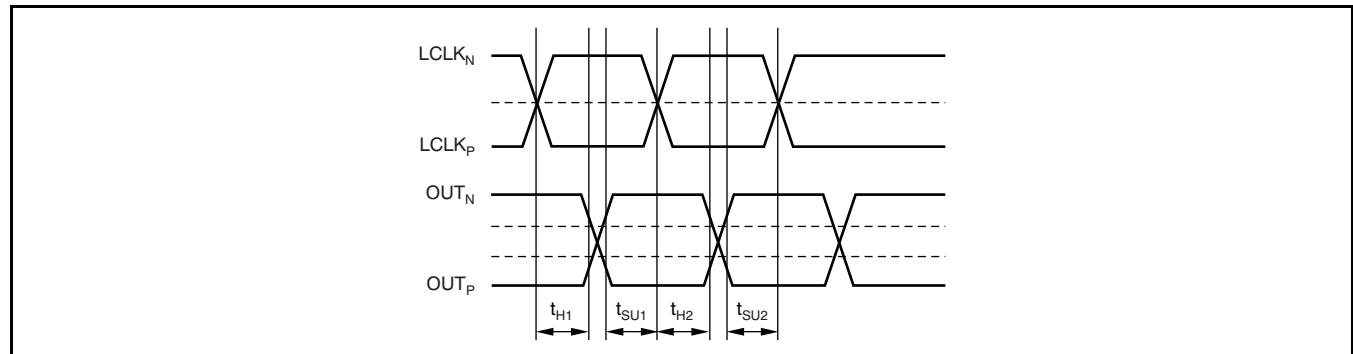
PIN NAME	DESCRIPTION	PIN NUMBER	# OF PINS
IN5 _P	Positive differential input signal, channel 5	38	1
IN6 _N	Negative differential input signal, channel 6	42	1
IN6 _P	Positive differential input signal, channel 6	41	1
IN7 _N	Negative differential input signal, channel 7	45	1
IN7 _P	Positive differential input signal, channel 7	44	1
IN8 _N	Negative differential input signal, channel 8	48	1
IN8 _P	Positive differential input signal, channel 8	47	1
INT/EXT	Internal/external reference mode select input	56	1
I _{SET}	Bias pin—56.2kΩ to ground	51	1
LCLK _N	LVDS bit clock (6X)—negative output	26	1
LCLK _P	LVDS bit clock (6X)—positive output	25	1
LVDD	Digital and I/O power supply, 1.8V	35	1
LVSS	Digital ground	12, 14, 36	3
OUT1 _N	LVDS channel 1—negative output	16	1
OUT1 _P	LVDS channel 1—positive output	15	1
OUT2 _N	LVDS channel 2—negative output	18	1
OUT2 _P	LVDS channel 2—positive output	17	1
OUT3 _N	LVDS channel 3—negative output	20	1
OUT3 _P	LVDS channel 3—positive output	19	1
OUT4 _N	LVDS channel 4—negative output	22	1
OUT4 _P	LVDS channel 4—positive output	21	1
OUT5 _N	LVDS channel 5—negative output	28	1
OUT5 _P	LVDS channel 5—positive output	27	1
OUT6 _N	LVDS channel 6—negative output	30	1
OUT6 _P	LVDS channel 6—positive output	29	1
OUT7 _N	LVDS channel 7—negative output	32	1
OUT7 _P	LVDS channel 7—positive output	31	1
OUT8 _N	LVDS channel 8—negative output	34	1
OUT8 _P	LVDS channel 8—positive output	33	1
PD	Power-down input	13	1
REF _B	Negative reference input/output	54	1
REF _T	Positive reference input/output	55	1
RESET	Active low RESET input	64	1
SCLK	Serial clock input	63	1
SDATA	Serial data input	62	1
TP	Test pin, do not use	52	1
V _{CM}	Common-mode output pin, 1.5V output	53	1



LVDS TIMING DIAGRAM



DEFINITION OF SETUP AND HOLD TIMES



$$t_{SU} = \min(t_{SU1}, t_{SU2})$$

$$t_H = \min(t_{H1}, t_{H2})$$

TIMING CHARACTERISTICS^{(1) (2)}

PARAMETER	TEST CONDITIONS	ADS528x			UNIT
		MIN	TYP	MAX	
t_A Aperture delay		1.5		4.5	ns
Aperture delay variation	Channel-to-channel within the same device (3σ)		± 20		ps
t_J Aperture jitter			400		fs
t_{WAKE} Wake-up time	Time to valid data after coming out of COMPLETE POWER-DOWN mode		50		μ s
	Time to valid data after coming out of PARTIAL POWER-DOWN mode (with clock continuing to run during power-down)		2		μ s
	Time to valid data after stopping and restarting the input clock		40		μ s
Data latency			12		Clock cycles

(1) Timing characteristics are common to the ADS528x family.

(2) Timing parameters are ensured by design and characterization; not production tested.

LVDS OUTPUT TIMING CHARACTERISTICS^{(1) (2)}

Typical values are at +25°C, minimum and maximum values are measured across the specified temperature range of $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = +85^{\circ}\text{C}$, sampling frequency = as specified, $C_{LOAD} = 5\text{pF}^{(3)}$, $I_{OUT} = 3.5\text{mA}$, $R_{LOAD} = 100\Omega^{(4)}$, and no internal termination, unless otherwise noted.

PARAMETER		TEST CONDITIONS ⁽⁵⁾	ADS528x									UNIT
			40MSPS			50MSPS			65MSPS			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{SU}	Data setup time ⁽⁶⁾	Data valid ⁽⁷⁾ to zero-crossing of LCLK _P	0.67			0.47			0.27			ns
t _H	Data hold time ⁽⁶⁾	Zero-crossing of LCLK _P to data becoming invalid ⁽⁷⁾	0.85			0.65			0.4			ns
t _{PROP}	Clock propagation delay	Input clock (ADCLK) rising edge cross-over to output clock (ADCLK _P) rising edge cross-over	10	14	16.6	10	12.5	14.1	9.7	11.5	14	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (LCLK _P – LCLK _N)	45.5	50	53	45	50	53.5	41	50	57	
	Bit clock cycle-to-cycle jitter			250			250			250		ps, pp
	Frame clock cycle-to-cycle jitter			150			150			150		ps, pp
t _{RISE} , t _{FALL}	Data rise time, data fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns
t _{CLKRISE} , t _{CLKFALL}	Output clock rise time, output clock fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns

- (1) All characteristics are at the maximum rated speed for each speed grade.
- (2) Timing parameters are ensured by design and characterization; not production tested.
- (3) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
- (4) I_{OUT} refers to the LVDS buffer current setting; R_{LOAD} is the differential load resistance between the LVDS output pair.
- (5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load.
- (6) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
- (7) Data valid refers to a logic high of +100mV and a logic low of –100mV.

LVDS OUTPUT TIMING CHARACTERISTICS^{(1) (2)}

Typical values are at +25°C, minimum and maximum values are measured across the specified temperature range of $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = +85^{\circ}\text{C}$, sampling frequency = as specified, $C_{LOAD} = 5\text{pF}^{(3)}$, $I_{OUT} = 3.5\text{mA}$, $R_{LOAD} = 100\Omega^{(4)}$, and no internal termination, unless otherwise noted.

PARAMETER		TEST CONDITIONS ⁽⁵⁾	ADS528x									UNIT
			30MSPS			20MSPS			10MSPS			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{SU}	Data setup time ⁽⁶⁾	Data valid ⁽⁷⁾ to zero-crossing of LCLK _P	0.8			1.5			3.7			ns
t _H	Data hold time ⁽⁶⁾	Zero-crossing of LCLK _P to data becoming invalid ⁽⁷⁾	1.2			1.9			3.9			ns
t _{PROP}	Clock propagation delay	Input clock (ADCLK) rising edge cross-over to output clock (ADCLK _P) rising edge cross-over	9.5	13.5	17.3	9.5	14.5	17.3	10	14.7	17.1	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (LCLK _P – LCLK _N)	46.5	50	52	48	50	51	49	50	51	
	Bit clock cycle-to-cycle jitter			250			250			750		ps, pp
	Frame clock cycle-to-cycle jitter			150			150			500		ps, pp
t _{RISE} , t _{FALL}	Data rise time, data fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns
t _{CLKRISE} , t _{CLKFALL}	Output clock rise time, output clock fall time	Rise time is from –100mV to +100mV Fall time is from +100mV to –100mV	0.09	0.2	0.4	0.09	0.2	0.4	0.09	0.2	0.4	ns

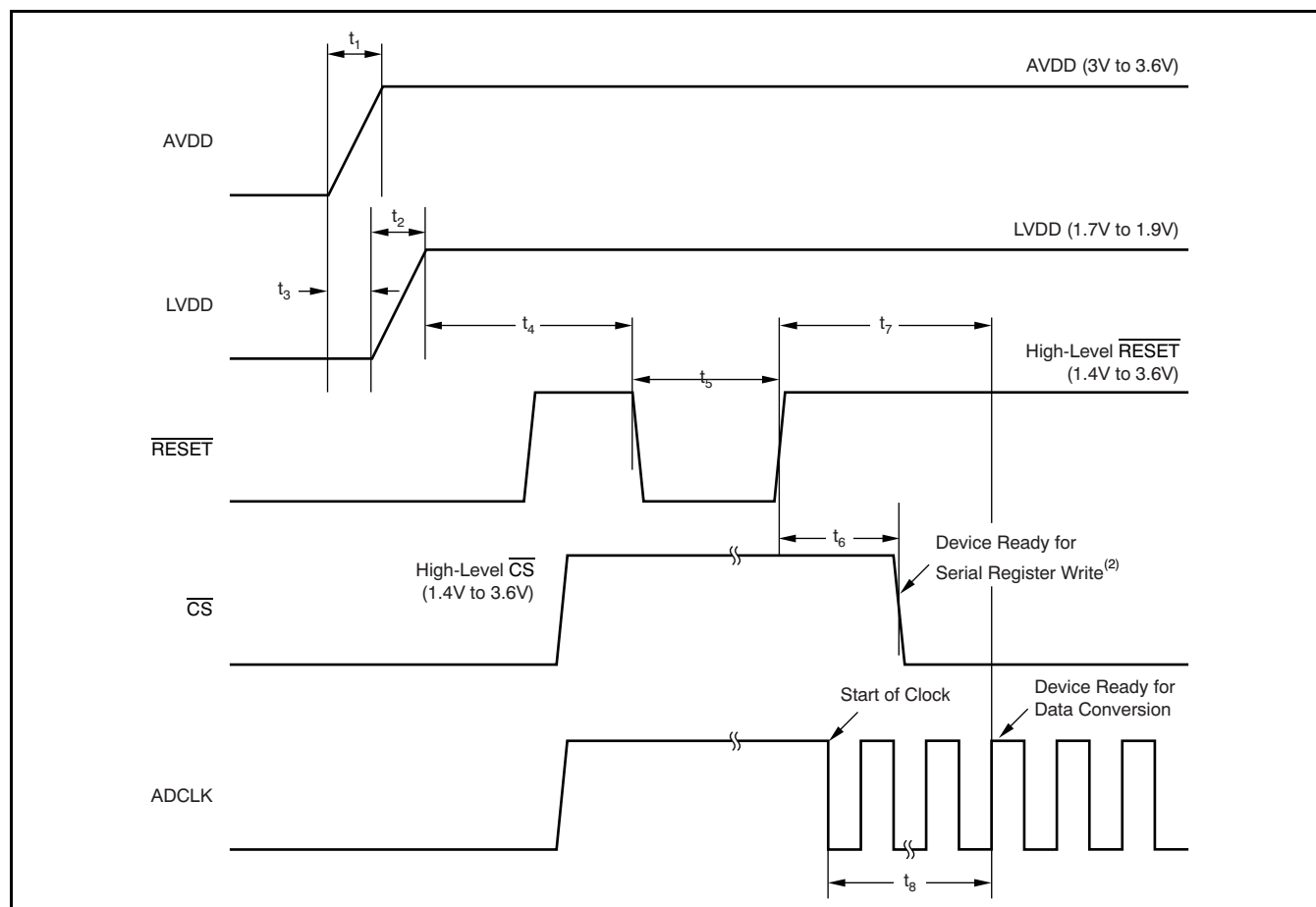
- (1) All characteristics are at the speeds other than the maximum rated speed for each speed grade.
- (2) Timing parameters are ensured by design and characterization; not production tested.
- (3) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
- (4) I_{OUT} refers to the LVDS buffer current setting; R_{LOAD} is the differential load resistance between the LVDS output pair.
- (5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load.
- (6) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
- (7) Data valid refers to a logic high of +100mV and a logic low of –100mV.

LVDS OUTPUT TIMING CHARACTERISTICS

PARAMETER ⁽¹⁾	TEST CONDITIONS	TIMINGS WHEN USING REGISTER 0xE3 ⁽²⁾ At 40 MSPS		
		MIN	TYP	MAX
Data setup time	Data valid ⁽³⁾ to zero-crossing of LCLKp	0.60		
Data hold time	Zero-crossing of LCLKp to data becoming invalid ⁽³⁾	0.92		
Clock propagation delay	Input clock (ADCLK) rising edge cross-over to output clock (ADCLK) rising edge crossover	8	12	14.6

- (1) Only the setup time, hold time and clock propagation delay parameters are affected. Rest of the parameters are same as given in previous two tables.
- (2) Only timing specifications for 40MSPS are affected when using register 0xE3 (as specified in the recommended operating table section). The timing specifications for other clock frequencies are same as given in previous two tables.
- (3) Data valid refers to logic high of +100mV and logic low of –100mV.

RECOMMENDED POWER-UP SEQUENCING AND RESET TIMING

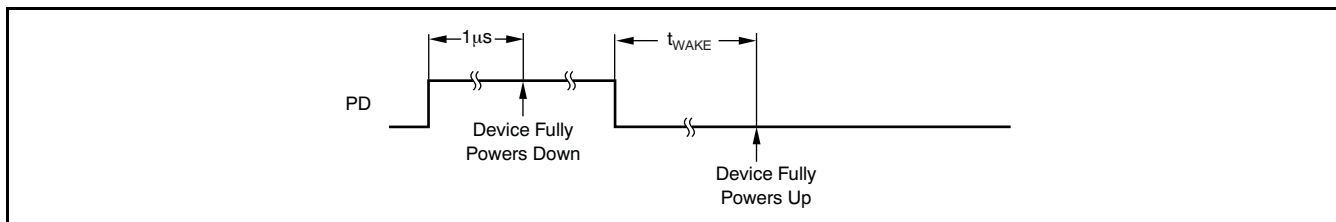


$10\mu\text{s} < t_1 < 50\text{ms}$, $10\mu\text{s} < t_2 < 50\text{ms}$, $-10\text{ms} < t_3 < 10\text{ms}$, $t_4 > 10\text{ms}$, $t_5 > 100\text{ns}$, $t_6 > 100\text{ns}$, $t_7 > 10\text{ms}$, and $t_8 > 100\mu\text{s}$.

(1) The AVDD and LVDD power on sequence does not matter as long as $-10\text{ms} < t_3 < 10\text{ms}$. Similar considerations apply while shutting down the device.

(2) Write initialization registers listed in the [Initialization Registers](#) table.

POWER-DOWN TIMING



Power-up time shown is based on $1\mu\text{F}$ bypass capacitors on the reference pins. t_{WAKE} is the time it takes for the device to wake up completely from power-down mode. The ADS528x has two power-down modes: complete power-down mode and partial power-down mode. The device can be configured in partial power-down mode through a register setting.

$t_{\text{WAKE}} < 50\mu\text{s}$ for complete power-down mode.

$t_{\text{WAKE}} < 2\mu\text{s}$ for partial power-down mode (provided the clock is not shut off during power-down).

SERIAL INTERFACE

The ADS528x has a set of internal registers that can be accessed through the serial interface formed by pins $\overline{\text{CS}}$ (chip select, active low), SCLK (serial interface clock), and SDATA (serial interface data). When $\overline{\text{CS}}$ is low, the following actions occur:

- Serial shift of bits into the device is enabled
- SDATA (serial data) is latched at every rising edge of SCLK
- SDATA is loaded into the register at every 24th SCLK rising edge

If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active $\overline{\text{CS}}$ pulse. The first eight bits form the register address and the remaining 16 bits form the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (a few hertz) and also with a non-50% SCLK duty cycle.

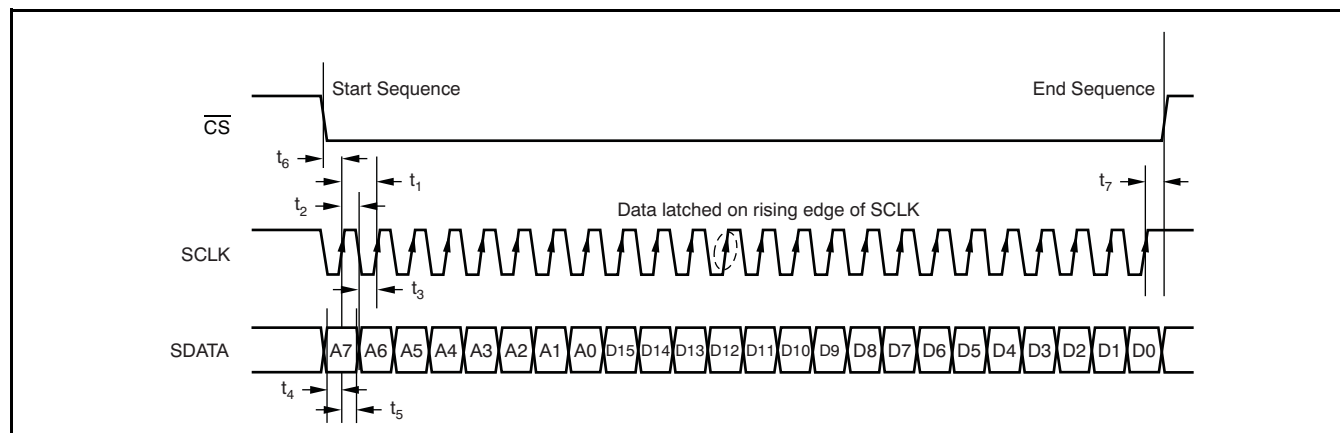
Register Initialization

After power-up, the internal registers **must** be initialized to the respective default values. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a low-going pulse on the $\overline{\text{RESET}}$ pin; or
2. Through a software reset; using the serial interface, set the RST bit high. Setting this bit initializes the internal registers to the respective default values and then self-resets the RST bit low. In this case, the $\overline{\text{RESET}}$ pin stays high (inactive).

After all registers have been initialized to their default values through a RESET operation, the registers detailed in the [Initialization Registers](#) table must be written into. This process must be done after every hardware or software RESET operation in order to reconfigure the device for the best mode of operation.

SERIAL INTERFACE TIMING



PARAMETER	DESCRIPTION	ADS528x			UNIT
		MIN	TYP	MAX	
t ₁	SCLK period	50			ns
t ₂	SCLK high time	20			ns
t ₃	SCLK low time	20			ns
t ₄	Data setup time	5			ns
t ₅	Data hold time	5			ns
t ₆	$\overline{\text{CS}}$ fall to SCLK rise	8			ns
t ₇	Time between last SCLK rising edge to $\overline{\text{CS}}$ rising edge	8			ns

SERIAL REGISTER MAP

Table 4. SUMMARY OF FUNCTIONS SUPPORTED BY SERIAL INTERFACE^{(1) (2) (3) (4)}

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION	DEFAULT
00																X	RST	Self-clearing software RESET.	Inactive
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>	Channel-specific ADC power-down mode.	Inactive
								X									PDN_PARTIAL	Partial power-down mode (fast recovery from power-down).	Inactive
							X										PDN_COMPLETE	Register mode for complete power-down (slower recovery).	Inactive
						X											PDN_PIN_CFG	Configures the PD pin for partial power-down mode.	Complete power-down
11														X	X	X	ILVDS_LCLK<2:0>	LVDS current drive programmability for LCLK _N and LCLK _P pins.	3.5mA drive
										X	X	X					ILVDS_FRAME<2:0>	LVDS current drive programmability for ADCLK _N and ADCLK _P pins.	3.5mA drive
						X	X	X									ILVDS_DAT<2:0>	LVDS current drive programmability for OUT _N and OUT _P pins.	3.5mA drive
12		X															EN_LVDS_TERM	Enables internal termination for LVDS buffers.	Termination disabled
		1												X	X	X	TERM_LCLK<2:0>	Programmable termination for LCLK _N and LCLK _P buffers.	Termination disabled
		1								X	X	X					TERM_FRAME<2:0>	Programmable termination for ADCLK _N and ADCLK _P buffers.	Termination disabled
		1				X	X	X									TERM_DAT<2:0>	Programmable termination for OUT _N and OUT _P buffers.	Termination disabled
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>	Channel-specific, low-frequency noise suppression mode enable.	Inactive
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>	Swaps the polarity of the analog input pins electrically.	IN _P is positive input
25										X	0	0					EN_RAMP	Enables a repeating full-scale ramp pattern on the outputs.	Inactive
										0	X	0					DUALCUSTOM_PAT	Enables the mode wherein the output toggles between two defined codes.	Inactive
										0	0	X					SINGLE_CUSTOM_PAT	Enables the mode wherein the output is a constant specified code.	Inactive
															X	X	BITS_CUSTOM1<11:10>	2MSBs for a single custom pattern (and for the first code of the dual custom pattern). <11> is the MSB.	Inactive
													X	X			BITS_CUSTOM2<11:10>	2MSBs for the second code of the dual custom pattern.	Inactive
26	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM1<9:0>	10 lower bits for the single custom pattern (and for the first code of the dual custom pattern). <0> is the LSB.	Inactive
27	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM2<9:0>	10 lower bits for the second code of the dual custom pattern.	Inactive
2A													X	X	X	X	GAIN_CH1<3:0>	Programmable gain channel 1.	0dB gain
									X	X	X	X					GAIN_CH2<3:0>	Programmable gain channel 2.	0dB gain
					X	X	X	X									GAIN_CH3<3:0>	Programmable gain channel 3.	0dB gain
	X	X	X	X													GAIN_CH4<3:0>	Programmable gain channel 4.	0dB gain
2B	X	X	X	X													GAIN_CH5<3:0>	Programmable gain channel 5.	0dB gain
					X	X	X	X									GAIN_CH6<3:0>	Programmable gain channel 6.	0dB gain
									X	X	X	X					GAIN_CH7<3:0>	Programmable gain channel 7.	0dB gain
													X	X	X	X	GAIN_CH8<3:0>	Programmable gain channel 8.	0dB gain

(1) The unused bits in each register (identified as blank table cells) must be programmed as '0'.

(2) X = Register bit referenced by the corresponding name and description (default is 0).

(3) Bits marked as '0' should be forced to 0, and bits marked as '1' should be forced to 1 when the particular register is programmed.

(4) Multiple functions in a register should be programmed in a single write operation.

Table 4. SUMMARY OF FUNCTIONS SUPPORTED BY SERIAL INTERFACE^{(1) (2) (3) (4)} (continued)

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION	DEFAULT
42	1															X	DIFF_CLK	Differential clock mode.	Single-ended clock
	1													X			EN_DCC	Enables the duty-cycle correction circuit.	Disabled
	1												X				EXT_REF_VCM	Drives the external reference mode through the V _{CM} pin.	External reference drives REF _T and REF _B
	1									X	X						PHASE_DDR<1:0>	Controls the phase of LCLK output relative to data.	90 degrees
45															0	X	PAT_DESKEW	Enables deskew pattern mode.	Inactive
															X	0	PAT_SYNC	Enables sync pattern mode.	Inactive
46	1						1							X			BTC_MODE	Binary two's complement format for ADC output.	Straight offset binary
	1						1						X				MSB_FIRST	Serialized ADC output comes out MSB-first.	LSB-first output
	1						1					X					EN_SDR	Enables SDR output mode (LCLK becomes a 12x input clock).	DDR output mode
	1		X				1					1					FALL_SDR	Controls whether the LCLK rising or falling edge comes in the middle of the data window when operating in SDR output mode.	Rising edge of LCLK in middle of data window

SUMMARY OF FEATURES

FEATURES	DEFAULT	SELECTION	POWER IMPACT (relative to default) AT f _S = 65MSPS
ANALOG FEATURES			
Internal or external reference (driven on the REF _T and REF _B pins)	N/A	Pin	Internal reference mode uses approximately 23mW more power on AVDD
External reference driven on the V _{CM} pin	Off	Register 42	Approximately 9mW less power on AVDD
Duty cycle correction circuit	Off	Register 42	Approximately 7mW more power on AVDD
Low-frequency noise suppression	Off	Register 14	With zero input to the ADC, low-frequency noise suppression causes digital switching at f _S /2, thereby increasing LVDD power by approximately 7mW/channel
Single-ended or differential clock	Single-ended	Register 42	Differential clock mode uses approximately 7mW more power on AVDD
Power-down mode	Off	Pin and register 0F	Refer to the <i>Power-Down Modes</i> section in the Electrical Characteristics table
DIGITAL FEATURES			
Programmable digital gain (0dB to 12dB)	0dB	Registers 2A and 2B	No difference
Straight offset or BTC output	Straight offset	Register 46	No difference
Swap polarity of analog input pins	Off	Register 24	No difference
LVDS OUTPUT PHYSICAL LAYER			
LVDS internal termination	Off	Register 12	Approximately 7mW more power on AVDD
LVDS current programmability	3.5mA	Register 11	As per LVDS clock and data buffer current setting
LVDS OUTPUT TIMING			
LSB- or MSB-first output	LSB-first	Register 46	No difference
DDR or SDR output	DDR	Register 46	SDR mode uses approximately 2mW more power on LVDD (at f _S = 30MSPS)
LCLK phase relative to data output	Refer to Figure 1	Register 42	No difference

DESCRIPTION OF SERIAL REGISTERS

SOFTWARE RESET

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
00																X	RST

Software reset is applied when the RST bit is set to '1'; setting this bit resets all internal registers and self-clears to '0'.

POWER-DOWN MODES

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>
								X									PDN_PARTIAL
						0	X										PDN_COMPLETE
						X	0										PDN_PIN_CFG

Each of the eight channels can be individually powered down. PDN_CH<N> controls the power-down mode for the ADC channel <N>.

In addition to channel-specific power-down, the ADS528x also has two global power-down modes—partial power-down mode and complete power-down mode. Partial power-down mode partially powers down the chip; recovery from this mode is much quicker, provided that the clock has been running for at least 50μs before exiting this mode. Complete power-down mode, on the other hand, completely powers down the chip, and involves a much longer recovery time.

In addition to programming the device for either of these two power-down modes (through either the PDN_PARTIAL or PDN_COMPLETE bits, respectively), the PD pin itself can be configured as either a partial power-down pin or a complete power-down pin control. For example, if PDN_PIN_CFG = 0 (default), when the PD pin is high, the device enters complete power-down mode. However, if PDN_PIN_CFG = 1, when the PD pin is high, the device enters partial power-down mode.

LVDS DRIVE PROGRAMMABILITY

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
11														X	X	X	ILVDS_LCLK<2:0>
										X	X	X					ILVDS_FRAME<2:0>
						X	X	X									ILVDS_DAT<2:0>

The LVDS drive strength of the bit clock (LCLK_P or LCLK_N) and the frame clock (ADCLK_P or ADCLK_N) can be individually programmed. The LVDS drive strengths of all the data outputs OUT_P and OUT_N can also be programmed to the same value.

All three drive strengths (bit clock, frame clock, and data) are programmed using sets of three bits. [Table 5](#) shows an example of how the drive strength of the bit clock is programmed (the method is similar for the frame clock and data drive strengths).

Table 5. Bit Clock Drive Strength⁽¹⁾

ILVDS_LCLK<2>	ILVDS_LCLK<1>	ILVDS_LCLK<0>	LVDS DRIVE STRENGTH FOR LCLK _P AND LCLK _N
0	0	0	3.5mA (default)
0	0	1	2.5mA
0	1	0	1.5mA
0	1	1	0.5mA
1	0	0	7.5mA
1	0	1	6.5mA
1	1	0	5.5mA
1	1	1	4.5mA

(1) Current settings lower than 1.5mA are not recommended.

LVDS INTERNAL TERMINATION PROGRAMMABILITY

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
12		X															EN_LVDS_TERM
		1												X	X	X	TERM_LCLK<2:0>
		1								X	X	X					TERM_FRAME<2:0>
		1				X	X	X									TERM_DAT<2:0>

The LVDS buffers have high-impedance current sources driving the outputs. When driving traces whose characteristic impedance is not perfectly matched with the termination impedance on the receiver side, there may be reflections back to the LVDS output pins of the ADS528x that cause degraded signal integrity. By enabling an internal termination (between the positive and negative outputs) for the LVDS buffers, the signal integrity can be significantly improved in such scenarios. To set the internal termination mode, the EN_LVDS_TERM bit should be set to '1'. Once this bit is set, the internal termination values for the bit clock, frame clock, and data buffers can be independently programmed using sets of three bits. [Table 6](#) shows an example of how the internal termination of the LVDS buffer driving the bit clock is programmed (the method is similar for the frame clock and data buffers). These termination values are only typical values and can vary by up to $\pm 20\%$ across temperature and from device to device.

Table 6. Bit Clock Internal Termination

TERM_LCLK<2>	TERM_LCLK<1>	TERM_LCLK<0>	INTERNAL TERMINATION BETWEEN LCLK _P AND LCLK _N IN Ω
0	0	0	None
0	0	1	260
0	1	0	150
0	1	1	94
1	0	0	125
1	0	1	80
1	1	0	66
1	1	1	55

LOW-FREQUENCY NOISE SUPPRESSION MODE

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>

The low-frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around dc). Setting this mode shifts the low-frequency noise of the ADS528x to approximately $f_s/2$, thereby moving the noise floor around dc to a much lower value. LFNS_CH<8:1> enables this mode individually for each channel.

ANALOG INPUT INVERT

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>

Normally, the IN_P pin represents the positive analog input pin, and IN_N represents the complementary negative input. Setting the bits marked INVERT_CH<8:1> (individual control for each channel) causes the inputs to be swapped. IN_N now represents the positive input, and IN_P the negative input.

LVDS TEST PATTERNS

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
25										X	0	0					EN_RAMP
										0	X	0					DUALCUSTOM_PAT
										0	0	X					SINGLE_CUSTOM_PAT
															X	X	BITS_CUSTOM1<11:0>
													X	X			BITS_CUSTOM2<11:0>
26	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM1<9:0>
27	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM2<9:0>
45															0	X	PAT_DESKEW
															X	0	PAT_SYNC

The ADS528x can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. Setting EN_RAMP to '1' causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.

The device can also be programmed to output a constant code by setting SINGLE_CUSTOM_PAT to '1', and programming the desired code in BITS_CUSTOM1<11:0>. In this mode, BITS_CUSTOM1<11:0> take the place of the 12-bit ADC data at the output, and are controlled by LSB-first and MSB-first modes in the same way as normal ADC data are.

The device may also be made to toggle between two consecutive codes by programming DUAL_CUSTOM_PAT to '1'. The two codes are represented by the contents of BITS_CUSTOM1<11:0> and BITS_CUSTOM2<11:0>.

In addition to custom patterns, the device may also be made to output two preset patterns:

1. **Deskew patten:** Set using PAT_DESKEW, this mode replaces the 12-bit ADC output D<11:0> with the 010101010101 word.
2. **Sync pattern:** Set using PAT_SYNC, the normal ADC word is replaced by a fixed 111111000000 word.

Note that only one of the above patterns should be active at any given instant.

PROGRAMMABLE GAIN

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2A													X	X	X	X	GAIN_CH1<3:0>
									X	X	X	X					GAIN_CH2<3:0>
					X	X	X	X									GAIN_CH3<3:0>
	X	X	X	X													GAIN_CH4<3:0>
2B	X	X	X	X													GAIN_CH5<3:0>
					X	X	X	X									GAIN_CH6<3:0>
									X	X	X	X					GAIN_CH7<3:0>
													X	X	X	X	GAIN_CH8<3:0>

In applications where the full-scale swing of the analog input signal is much less than the $2V_{PP}$ range supported by the ADS528x, a programmable gain can be set to achieve the full-scale output code even with a lower analog input swing. The programmable gain not only fills the output code range of the ADC, but also enhances the SNR of the device by utilizing quantization information from some extra internal bits. The programmable gain for each channel can be individually set using a set of four bits, indicated as GAIN_CHN<3:0> for Channel N. The gain setting is coded in binary from 0dB to 12dB, as shown in [Table 7](#).

Table 7. Gain Setting for Channel 1

GAIN_CH1<3>	GAIN_CH1<2>	GAIN_CH1<1>	GAIN_CH1<0>	CHANNEL 1 GAIN SETTING
0	0	0	0	0dB
0	0	0	1	1dB
0	0	1	0	2dB
0	0	1	1	3dB
0	1	0	0	4dB
0	1	0	1	5dB
0	1	1	0	6dB
0	1	1	1	7dB
1	0	0	0	8dB
1	0	0	1	9dB
1	0	1	0	10dB
1	0	1	1	11dB
1	1	0	0	12dB
1	1	0	1	Do not use
1	1	1	0	Do not use
1	1	1	1	Do not use

CLOCK, REFERENCE, AND DATA OUTPUT MODES

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
42	1															X	DIFF_CLK
	1													X			EN_DCC
	1												X				EXT_REF_VCM
	1									X	X						PHASE_DDR<1:0>
46	1						1							X			BTC_MODE
	1						1						X				MSB_FIRST
	1						1					X					EN_SDR
	1		X				1					1					FALL_SDR

INPUT CLOCK

The ADS528x is configured by default to operate with a single-ended input clock—CLK_P is driven by a CMOS clock and CLK_N is tied to '0'. However, by programming DIFF_CLK to '1', the device can be made to work with a differential input clock on CLK_P and CLK_N. Operating with a low-jitter differential clock usually gives better SNR performance, especially at input frequencies greater than 30MHz.

In cases where the duty cycle of the input clock falls outside the 45% to 55% range, it is recommended to enable an internal duty cycle correction circuit. This enabling is done by setting the EN_DCC bit to '1'.

EXTERNAL REFERENCE

The ADS528x can be made to operate in external reference mode by pulling the INT/ $\overline{\text{EXT}}$ pin to '0'. In this mode, the REF_T and REF_B pins should be driven with voltage levels of 2.5V and 0.5V, respectively, and must have enough drive strength to drive the switched capacitance loading of the reference voltages by each ADC. The advantage of using the external reference mode is that multiple ADS528x units can be made to operate with the same external reference, thereby improving parameters such as gain matching across devices. However, in applications that do not have an available high drive, differential external reference, the ADS528x can still be driven with a single external reference voltage on the V_{CM} pin. When EXT_REF_VCM is set as '1' (and the INT/ $\overline{\text{EXT}}$ pin is set to '0'), the V_{CM} pin is configured as an input pin, and the voltages on REF_T and REF_B are generated as shown in [Equation 1](#) and [Equation 2](#).

$$\text{VREF}_T = 1.5\text{V} + \frac{\text{V}_{\text{CM}}}{1.5\text{V}} \quad (1)$$

$$\text{VREF}_B = 1.5\text{V} - \frac{\text{V}_{\text{CM}}}{1.5\text{V}} \quad (2)$$

BIT CLOCK PROGRAMMABILITY

The output interface of the ADS528x is normally a DDR interface, with the LCLK rising edge and falling edge transitions in the middle of alternate data windows. This default phase is shown in [Figure 1](#).

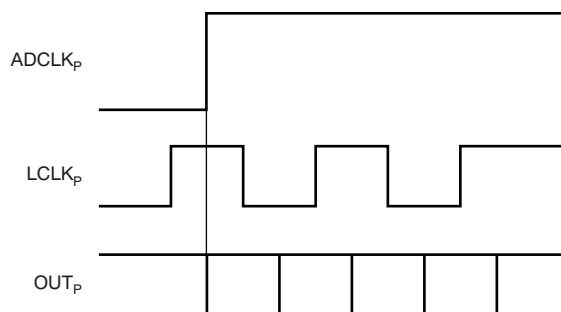


Figure 1. Default Phase of LCLK

The phase of LCLK can be programmed relative to the output frame clock and data using bits PHASE_DDR<1:0>. The LCLK phase modes are shown in [Figure 2](#).

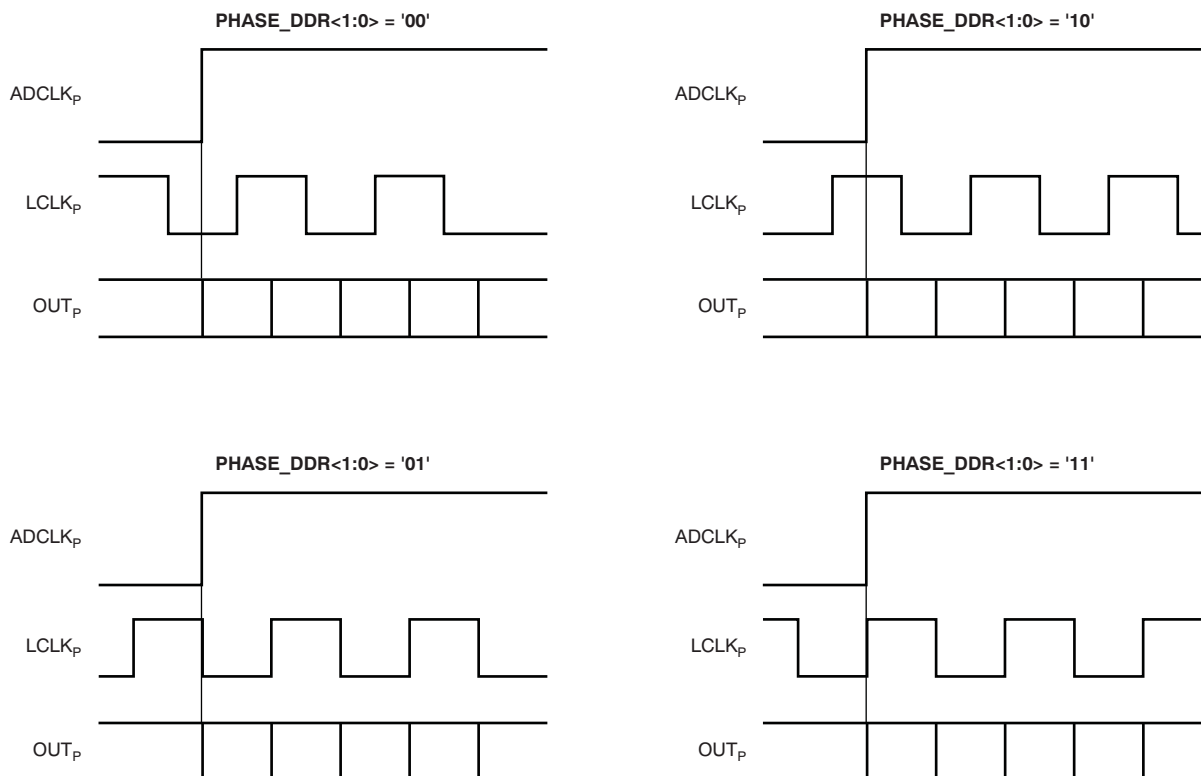


Figure 2. Phase Programmability Modes for LCLK

In addition to programming the phase of LCLK in the DDR mode, the device can also be made to operate in SDR mode by setting the EN_SDR bit to '1'. In this mode, the bit clock (LCLK) is output at 12x times the input clock, or twice the rate as in DDR mode. Depending on the state of FALL_SDR, LCLK may be output in either of the two manners shown in Figure 3. As can be seen in Figure 3, only the LCLK rising (or falling) edge is used to capture the output data in SDR mode.

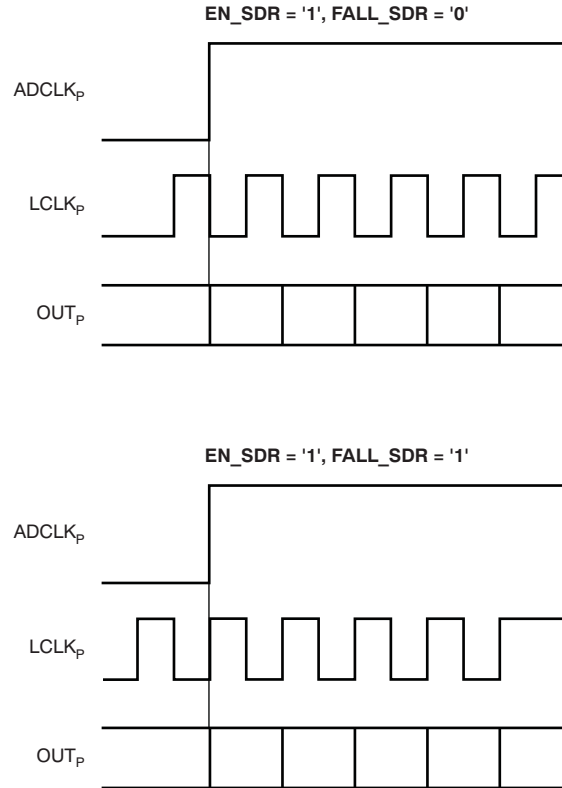


Figure 3. SDR Interface Modes

The SDR mode does not work well beyond 40MSPS because the LCLK frequency becomes very high.

DATA OUTPUT FORMAT MODES

The ADC output, by default, is in straight offset binary mode. Programming the BTC_MODE bit to '1' inverts the MSB, and the output becomes binary two's complement mode.

Also by default, the first bit of the frame (following the rising edge of **ADCLK_p**) is the LSB of the ADC output. Programming the MSB_FIRST mode inverts the bit order in the word, and the MSB is output as the first bit following the **ADCLK_p** rising edge.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $A_{VDD} = +3.3\text{V}$, $LVDD = 1.8\text{V}$, clock frequency = 65MSPS, differential clock mode, $1V_{PP}$ clock amplitude, 50% clock duty cycle, input frequency = 10MHz, -1dBFS differential analog input, 0dB digital gain setting, 1.5V analog input common-mode, low-frequency noise suppression = off, internal reference mode, I_{SET} resistor = $56.2\text{k}\Omega$, and LVDS buffer current setting = 3.5mA , unless otherwise noted.

SPECTRAL PERFORMANCE
($f_S = 40\text{MHz}$, $f_{IN} = 10\text{MHz}$)

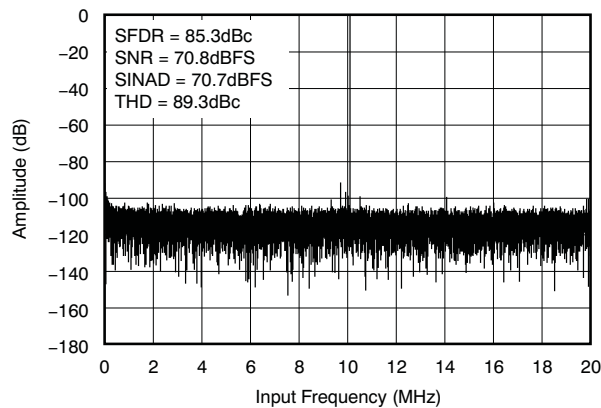


Figure 4.

SPECTRAL PERFORMANCE
($f_S = 40\text{MHz}$, $f_{IN} = 25\text{MHz}$)

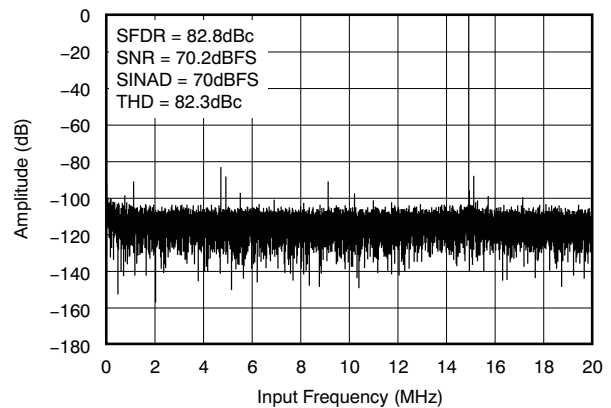


Figure 5.

SPECTRAL PERFORMANCE
($f_S = 50\text{MHz}$, $f_{IN} = 10\text{MHz}$)

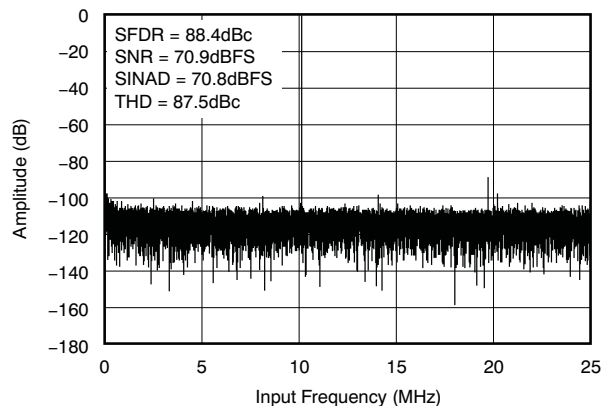


Figure 6.

SPECTRAL PERFORMANCE
($f_S = 50\text{MHz}$, $f_{IN} = 25\text{MHz}$)

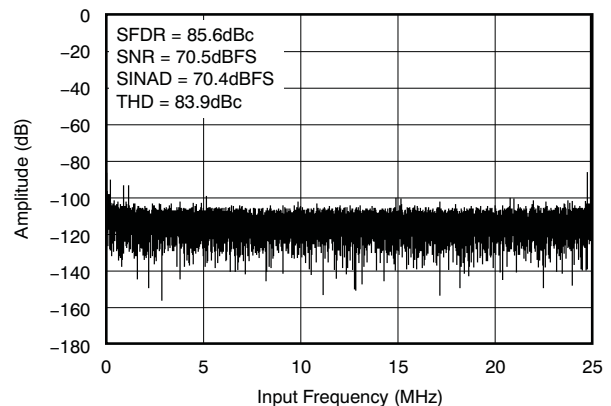


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AVDD = +3.3\text{V}$, $LVDD = 1.8\text{V}$, clock frequency = 65MSPS, differential clock mode, $1V_{PP}$ clock amplitude, 50% clock duty cycle, input frequency = 10MHz, -1dBFS differential analog input, 0dB digital gain setting, 1.5V analog input common-mode, low-frequency noise suppression = off, internal reference mode, I_{SET} resistor = $56.2\text{k}\Omega$, and LVDS buffer current setting = 3.5mA , unless otherwise noted.

SPECTRAL PERFORMANCE
($f_S = 65\text{MHz}$, $f_{IN} = 10\text{MHz}$)

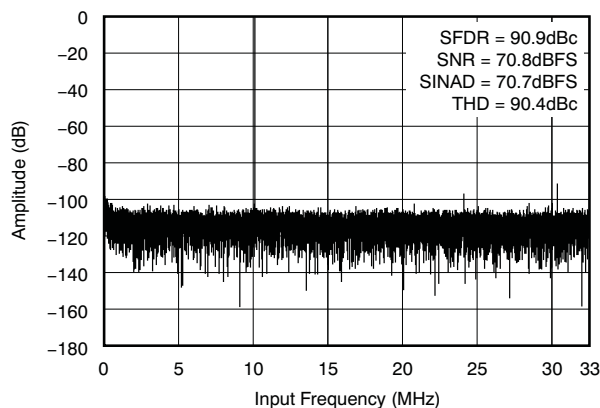


Figure 8.

SPECTRAL PERFORMANCE
($f_S = 65\text{MHz}$, $f_{IN} = 25\text{MHz}$)

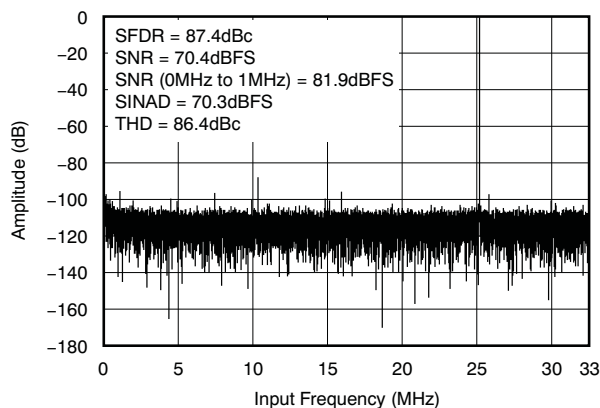


Figure 9.

**SPECTRAL PERFORMANCE, LOW-FREQUENCY NOISE
SUPPRESSION MODE ENABLED**
($f_S = 65\text{MHz}$, $f_{IN} = 25\text{MHz}$)

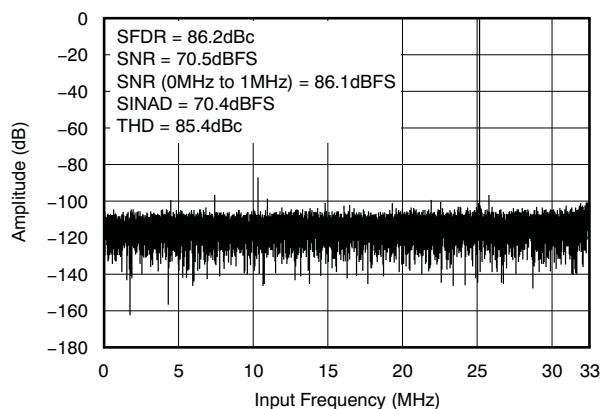


Figure 10.

DYNAMIC PERFORMANCE vs INPUT FREQUENCY

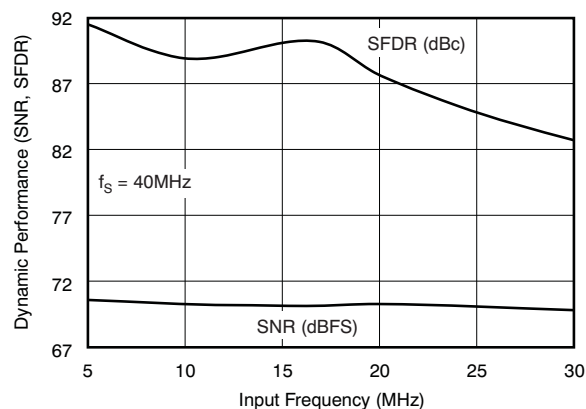
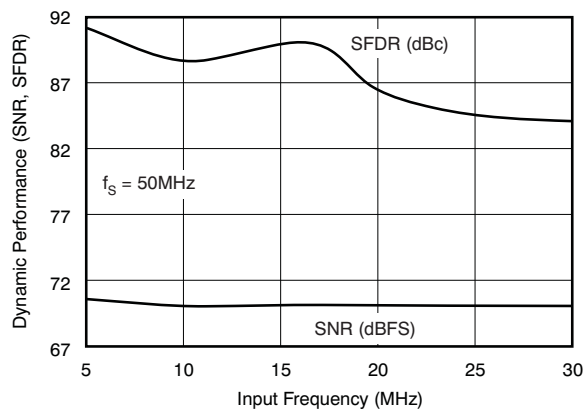
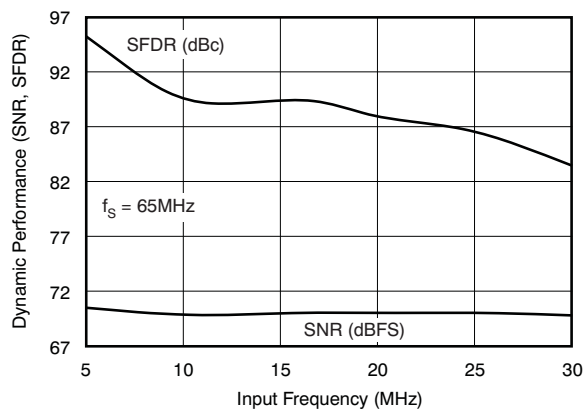
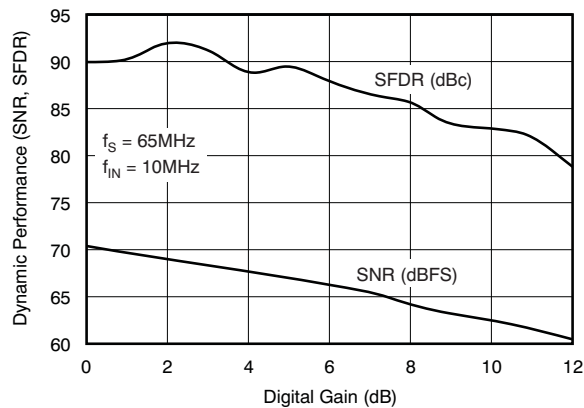
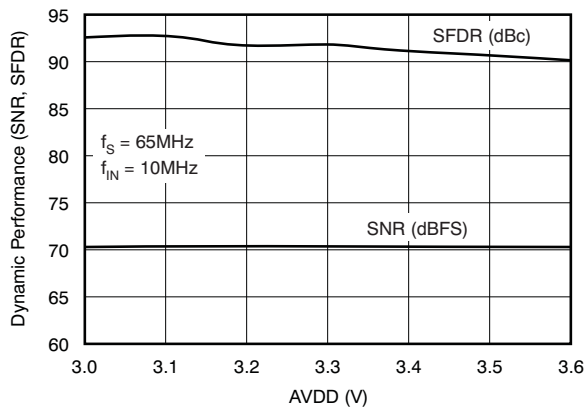
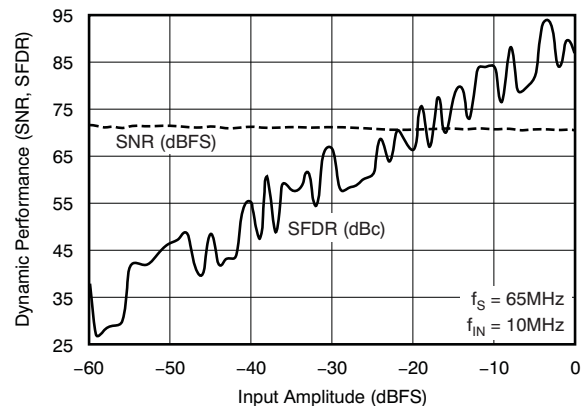
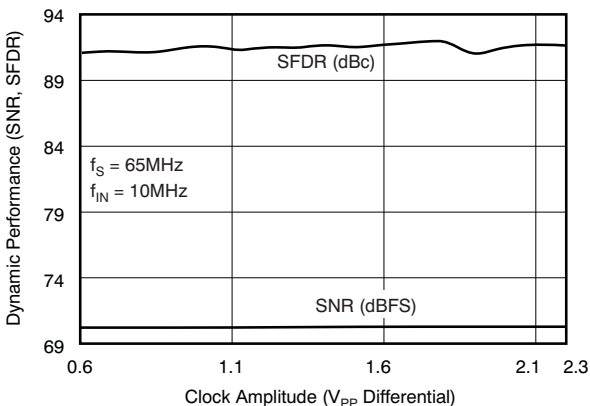


Figure 11.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = +3.3\text{V}$, $LV_{DD} = 1.8\text{V}$, clock frequency = 65MSPS, differential clock mode, $1V_{PP}$ clock amplitude, 50% clock duty cycle, input frequency = 10MHz, -1dBFS differential analog input, 0dB digital gain setting, 1.5V analog input common-mode, low-frequency noise suppression = off, internal reference mode, I_{SET} resistor = $56.2\text{k}\Omega$, and LVDS buffer current setting = 3.5mA , unless otherwise noted.

DYNAMIC PERFORMANCE vs INPUT FREQUENCY**Figure 12.****DYNAMIC PERFORMANCE vs INPUT FREQUENCY****Figure 13.****DYNAMIC PERFORMANCE vs DIGITAL GAIN****Figure 14.****DYNAMIC PERFORMANCE vs AVDD****Figure 15.****DYNAMIC PERFORMANCE vs INPUT AMPLITUDE****Figure 16.****DYNAMIC PERFORMANCE vs CLOCK AMPLITUDE****Figure 17.**

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = +3.3\text{V}$, $LV_{DD} = 1.8\text{V}$, clock frequency = 65MSPS, differential clock mode, $1V_{PP}$ clock amplitude, 50% clock duty cycle, input frequency = 10MHz, -1dBFS differential analog input, 0dB digital gain setting, 1.5V analog input common-mode, low-frequency noise suppression = off, internal reference mode, I_{SET} resistor = 56.2k Ω , and LVDS buffer current setting = 3.5mA, unless otherwise noted.

DYNAMIC PERFORMANCE vs ANALOG INPUT COMMON-MODE VOLTAGE

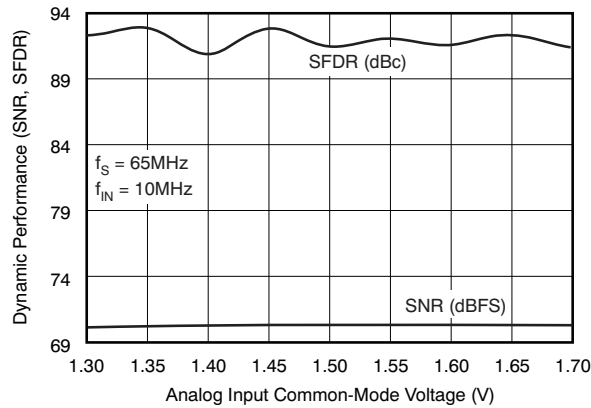


Figure 18.

DYNAMIC PERFORMANCE vs EXTERNAL REFERENCE DIFFERENTIAL VOLTAGE

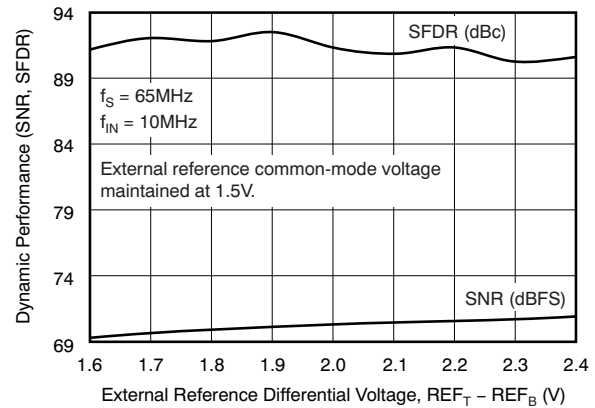


Figure 19.

DYNAMIC PERFORMANCE vs EXTERNAL REFERENCE COMMON-MODE VOLTAGE

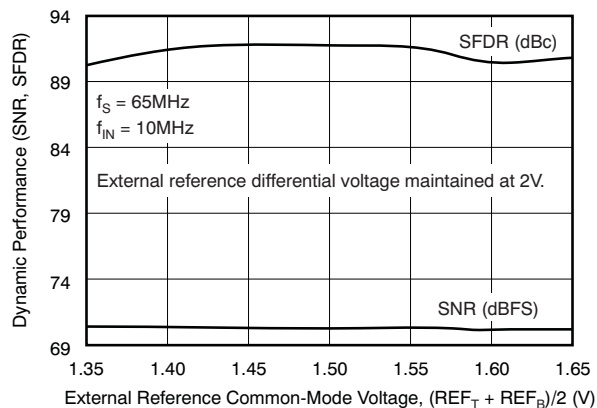


Figure 20.

DYNAMIC PERFORMANCE vs EXTERNAL REFERENCE FORCED THROUGH V_{CM}

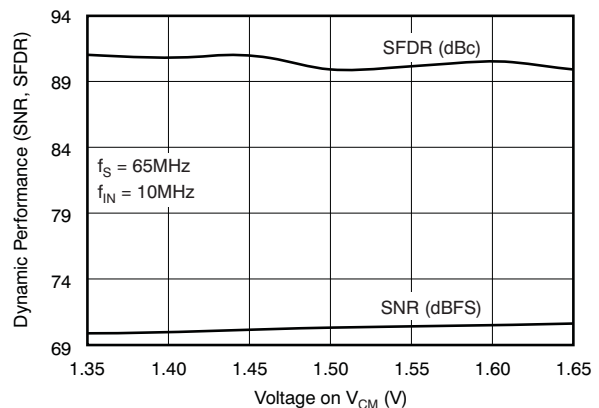


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AVDD = +3.3\text{V}$, $LVDD = 1.8\text{V}$, clock frequency = 65MSPS, differential clock mode, $1V_{PP}$ clock amplitude, 50% clock duty cycle, input frequency = 10MHz, -1dBFS differential analog input, 0dB digital gain setting, 1.5V analog input common-mode, low-frequency noise suppression = off, internal reference mode, I_{SET} resistor = $56.2\text{k}\Omega$, and LVDS buffer current setting = 3.5mA , unless otherwise noted.

DYNAMIC PERFORMANCE vs CLOCK DUTY CYCLE, DCC DISABLED

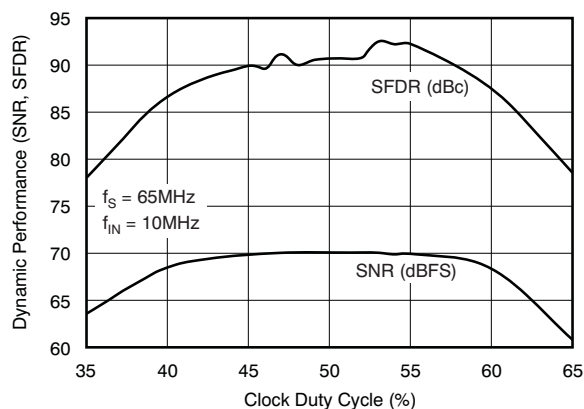


Figure 22.

DYNAMIC PERFORMANCE vs CLOCK DUTY CYCLE, DCC ENABLED

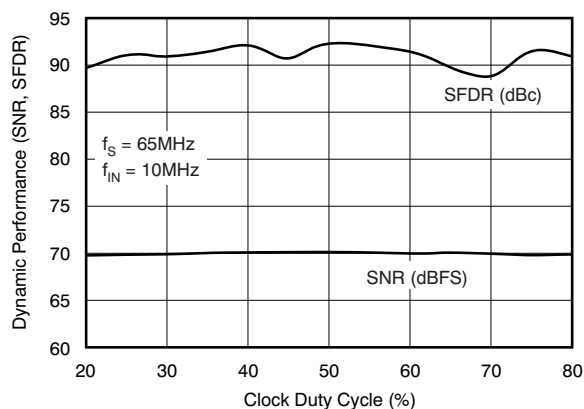


Figure 23.

HISTOGRAM OF OUTPUT CODE FOR ZERO INPUT

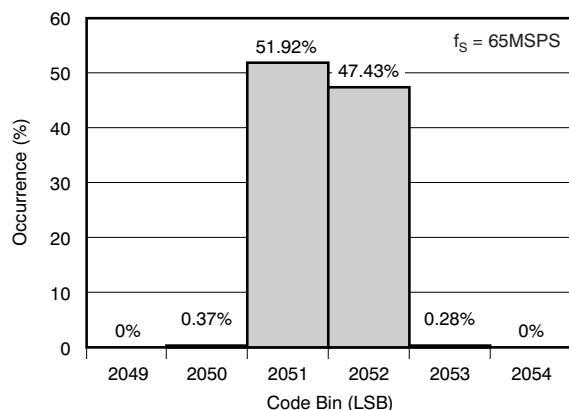


Figure 24.

INTERMODULATION DISTORTION

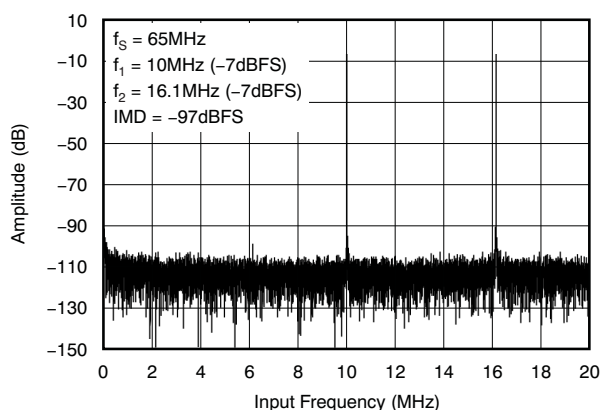


Figure 25.

INTEGRAL NONLINEARITY

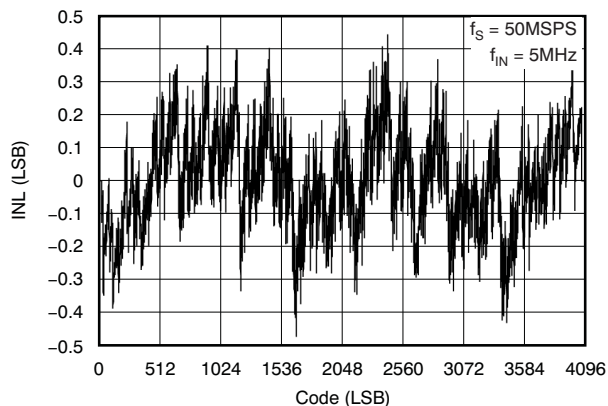


Figure 26.

DIFFERENTIAL NONLINEARITY

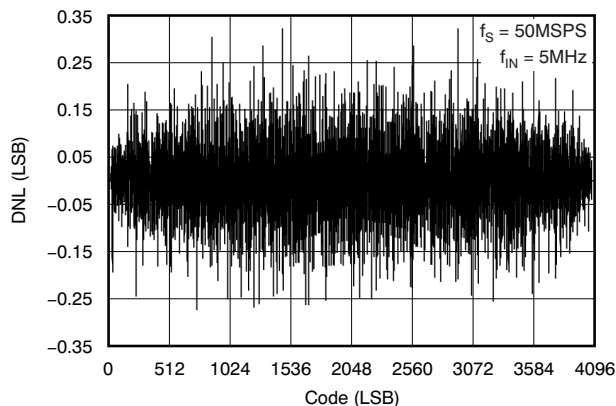


Figure 27.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AVDD = +3.3\text{V}$, $LVDD = 1.8\text{V}$, clock frequency = 65MSPS, differential clock mode, $1V_{PP}$ clock amplitude, 50% clock duty cycle, input frequency = 10MHz, -1dBFS differential analog input, 0dB digital gain setting, 1.5V analog input common-mode, low-frequency noise suppression = off, internal reference mode, I_{SET} resistor = $56.2\text{k}\Omega$, and LVDS buffer current setting = 3.5mA , unless otherwise noted.

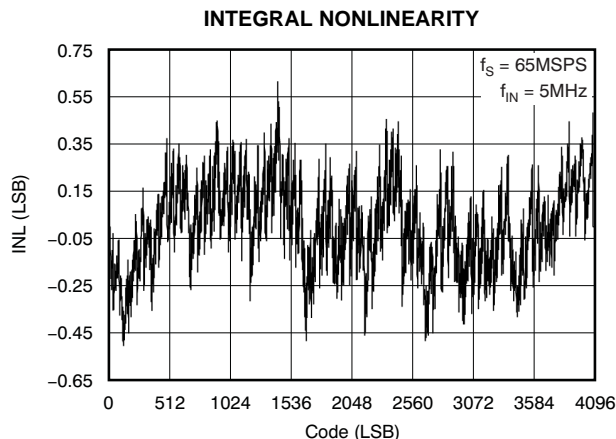


Figure 28.

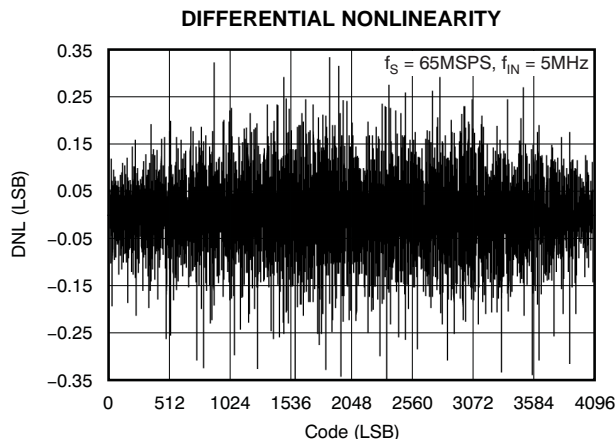


Figure 29.

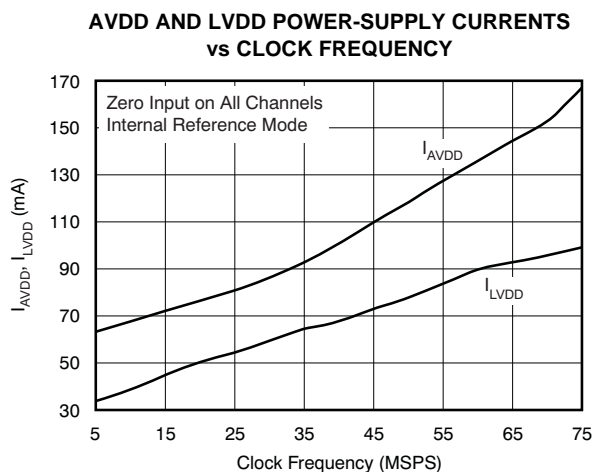


Figure 30.

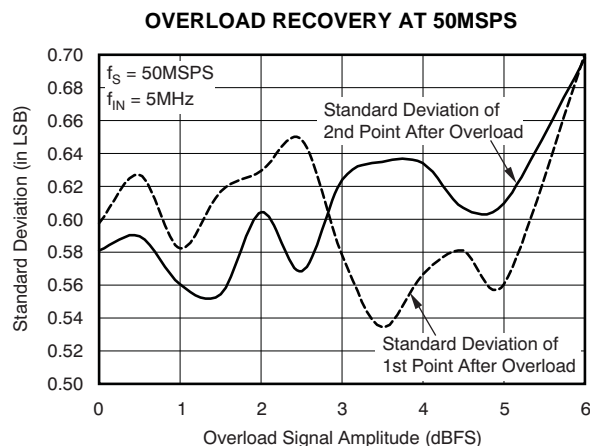


Figure 31.

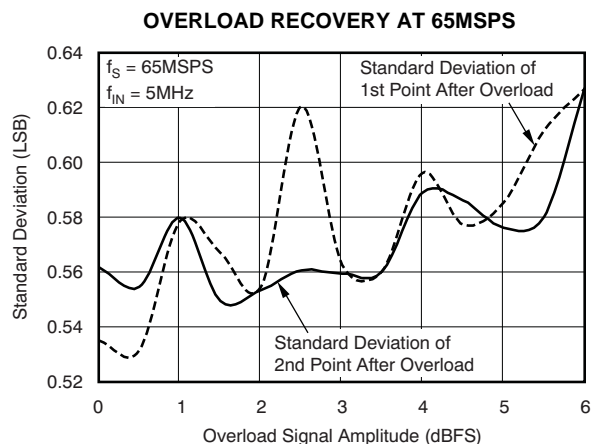


Figure 32.

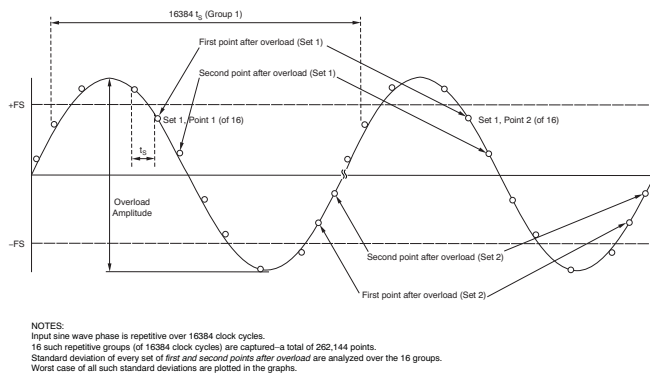


Figure 33. Overload Recovery

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS528x devices are a family of 8-channel, high-speed, CMOS ADCs. The 12 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the ADS528x operate from a single clock (ADCLK). The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 12x clock required for the serializer is generated internally from ADCLK using a phase-locked loop (PLL). A 6x and a 1x clock are also output in LVDS format, along with the data, to enable easy data capture. The ADS528x operates from internally-generated reference voltages that are trimmed to improve to a high level of accuracy. Trimmed references improve the gain matching across devices, and provide the option to operate the devices without having to externally drive and route reference lines. The nominal values of REF_T and REF_B are 2.5V and 0.5V, respectively. The references are internally scaled down differentially by a factor of 2. This scaling results in a differential input of $-1V$ to correspond to the zero code of the ADC, and a differential input of $+1V$ to correspond to the full-scale code (4095 LSB). V_{CM} (the common-mode voltage of REF_T and REF_B) is also made available externally through a pin, and is nominally 1.5V.

The ADC employs a pipelined converter architecture that consists of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 12-bit level.

The ADC output goes to a serializer that operates from a 12x clock generated by the PLL. The 12 data bits from each channel are serialized and sent LSB first. In addition to serializing the data, the serializer also generates a 1x clock and a 6x clock. These clocks are generated in the same way the serialized data are generated, so these clocks maintain perfect synchronization with the data. The data and clock outputs of the serializer are buffered externally using LVDS buffers. Using LVDS buffers to transmit data externally has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the ADS528x.

The ADS528x operates from two sets of supplies and grounds. The analog supply and ground set is identified as AVDD and AVSS, while the digital set is identified by LVDD and LVSS.

ANALOG INPUT

The analog input consists of a switched-capacitor based, differential sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The IN_N and IN_P pins must be externally biased around a common-mode voltage of 1.5V, available on V_{CM} . For a full-scale differential input, each input pin (IN_N and IN_P) must swing symmetrically between $V_{CM} + 0.5V$ and $V_{CM} - 0.5V$, resulting in a $2V_{PP}$ differential input swing. The maximum input peak-to-peak differential swing is determined to be the difference between the internal reference voltages REF_T (2.5V nominal) and REF_B (0.5V nominal). [Figure 34](#) illustrates the model of the input driving circuit.

Driving Circuit

For optimum performance, the analog inputs must be driven differentially. This approach improves the common-mode noise immunity and even-order harmonic rejection. Input configurations using RF transformers suitable for low and high input frequencies are shown in [Figure 36](#) and [Figure 37](#), respectively. The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated by 50Ω resistor on the secondary side. Placing the termination on the secondary side helps to shield the kicks caused by the input sampling capacitors from the RF transformer leakage inductances. The termination is accomplished by two 25Ω resistors, connected in series, with the center point connected to the 1.5V common-mode. The 4.7Ω resistor in series with each input pin is required to damp the ringing caused by the device package parasitics.

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps to minimize this mismatch, and good performance is obtained for high-frequency input signals. An additional termination resistor pair is required between the two transformers, as shown in [Figure 37](#). The center point of this termination is connected to ground to improve the balance between the positive and negative sides. The values of the terminations between the transformers and on the secondary side must be chosen to achieve an overall 50Ω (in the case of 50Ω source impedance).

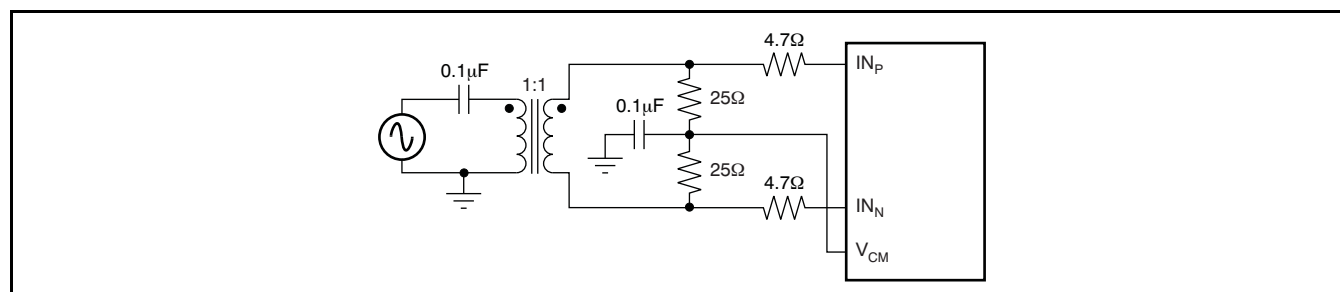


Figure 36. Drive Circuit at Low Input Frequencies

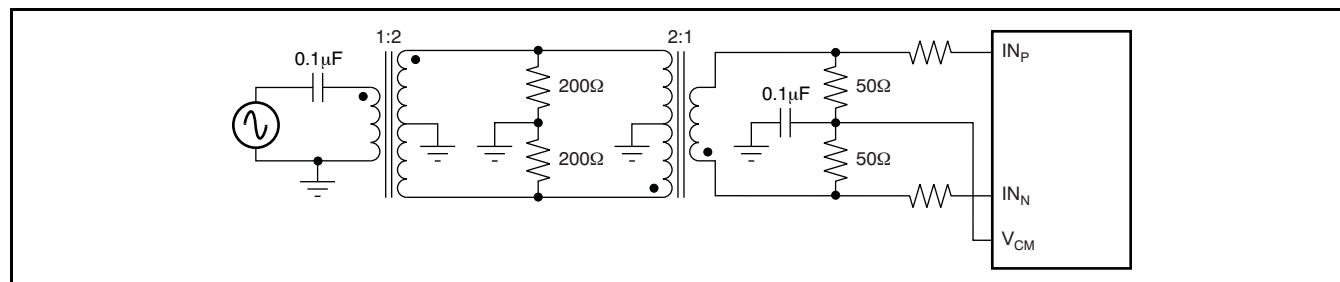


Figure 37. Drive Circuit at High Input Frequencies

CLOCK INPUT

The eight channels on the device operate from a single ADCLK input. To ensure that the aperture delay and jitter are the same for all channels, a clock tree network is used to generate individual sampling clocks to each channel. The clock paths for all the channels are matched from the source point to the sampling circuit. This architecture ensures that the performance and timing for all channels are identical. The use of the clock tree for matching introduces an aperture delay that is defined as the delay between the rising edge of ADCLK and the actual instant of sampling. The aperture delays for all the channels are matched to the best possible extent. A mismatch of $\pm 20\text{ps}$ ($\pm 3\sigma$) could exist between the aperture instants of the eight ADCs within the same chip. However, the aperture delays of ADCs across two different chips can be several hundred picoseconds apart.

The ADS528x can be made to operate either in CMOS single-ended clock mode (default is DIFF_CLK = 0) or differential clock mode (SINE, LVPECL, or LVDS). When operating in the single-ended clock mode, CLK_N must be forced to 0V_{DC}, and the single-ended CMOS applied on the CLK_P pin. This operation is shown in Figure 38.

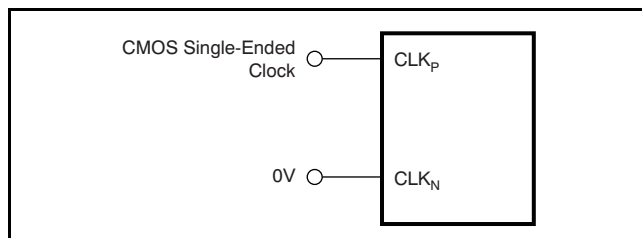


Figure 38. Single-Ended Clock Driving Circuit (DIFF_CLK = 0)

When configured to operate in the differential clock mode (register bit DIFF_CLK = 1) the ADS528x clock inputs can be driven differentially (SINE, LVPECL, or LVDS) with little or no difference in performance between them, or with a single-ended (LVCMOS). The common-mode voltage of the clock inputs is set to V_{CM} using internal 5kΩ resistors, as shown in Figure 39. This method allows using transformer-coupled drive circuits for a sine wave clock or ac-coupling for LVPECL and LVDS clock sources, as shown in Figure 40. When operating in the differential clock mode, the single-ended CMOS clock can be ac-coupled to the CLK_P input, with CLK_N (pin 11) connected to ground with a 0.1μF capacitor, as shown in Figure 41.

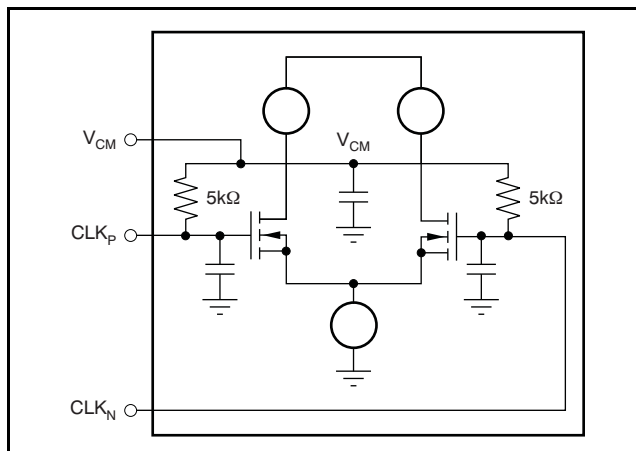


Figure 39. Internal Clock Buffer

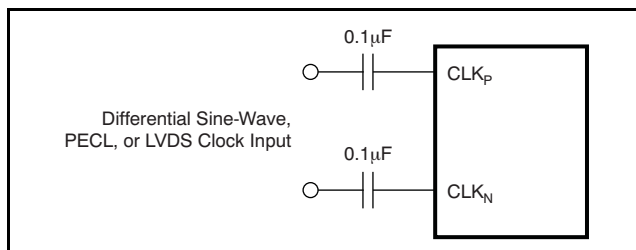


Figure 40. Differential Clock Driving Circuit (DIFF_CLK = 1)

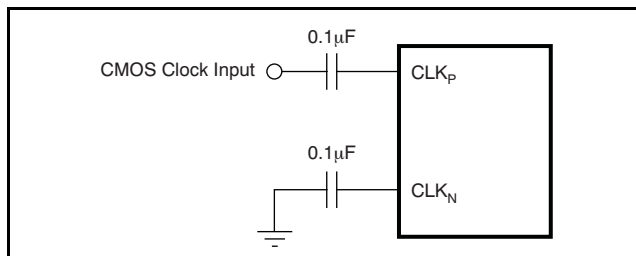


Figure 41. Single-Ended Clock Driving Circuit When DIFF_CLK = 1

For best performance, the clock inputs must be driven differentially in order to reduce susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. If the duty cycle deviates from 50% by more than 2% or 3%, it is recommended to enable the DCC through register bit EN_DCC.

PLL OPERATION ACROSS SAMPLING FREQUENCY

The ADS528X uses a PLL for generating the high speed bit clock (LCLK), the frame clock (ADCLK) & internal clocks for the serializer operation.

To enable operation across the entire frequency range, the PLL is automatically configured to one of four states, depending on the sampling clock frequency range. The frequency range detection is automatic and each time the sampling frequency crosses a threshold, the PLL changes its configuration to a new state. To prevent unwanted toggling of PLL state around a threshold, the circuit has an inbuilt hysteresis. The ADS528x has three thresholds – taking into account the hysteresis range of each threshold, variation across devices and temperature, the thresholds can span the sampling clock frequency range from 10MHz to 45MHz.

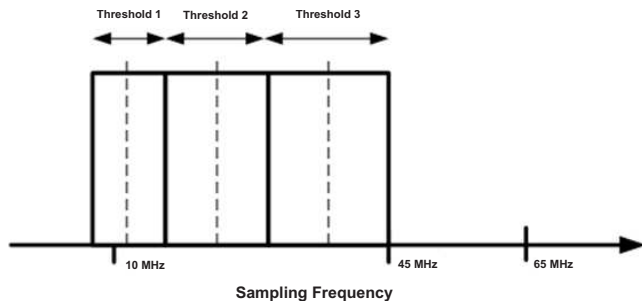


Figure 42. Variation of Thresholds Across Sampling Frequency

Based on actual system clock frequency, there are two scenarios:

1. For sampling clock frequency < 45MSPS

After system power up, depending on the frequency of operation and the frequency threshold for the given device, the frequency range detection circuit may change state once. In some applications where a timing calibration might be done at the system level once after power up, this subsequent change of the PLL state might be undesirable as it can cause a loss of alignment in the received data. A software fix for eliminating this one-time change of PLL state exists using the serial register interface:

- Disable the automatic switch of the PLL configuration based on frequency detected.
- In addition to disabling the switching, it is also required to set the PLL to the correct configuration, depending on the sample clock frequency used in the system.

The following sequence of register writes must be followed:

Step 1: Write Address = 0x01, Data = 0x0010

Step 2: Disable the PLL automatic switch and set the PLL configuration depending on the clock frequency

SAMPLE CLOCK FREQUENCY RANGE (MSPS)		REGISTER SETTING (Hex)	
Min	Max	Address	Data
10	25	E3	0060
15	45	E3	00A0

With the above settings applied for the respective frequency ranges, the part will continue to operate as per the stated datasheet specifications for all timing parameters at all specified frequencies, EXCEPT for the timing specifications at 40MSPS. At 40MSPS, the affected parameters are – Data setup time, Data hold time and Clock propagation delay (refer to LVDS Timing).

2. For sampling clock frequency ≥ 45MSPS

As there are no PLL thresholds beyond 45MHz, no change in PLL configuration can occur as the temperature in the system stabilizes. The ADS528x can be used in the system without using the above software fix.

INPUT OVER-VOLTAGE RECOVERY

The differential peak-to-peak full-scale range supported by the ADS528x is nominally 2.0V. The ADS528x is specially designed to handle an over-voltage condition where the differential peak-to-peak voltage can be up to twice the ADC full-scale range. If the input common-mode is not considerably off from V_{CM} during overload (less than 300mV around the nominal value of 1.5V), recovery from an over-voltage pulse input of twice the amplitude of a full-scale pulse is expected to be within one clock cycle when the input switches from overload to zero signal.

REFERENCE CIRCUIT

The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system would have about 12 octal ADCs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the ADCs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips.

All bias currents required for the internal operation of the device are set using an external resistor to ground at the I_{SET} pin. Using a 56.2kΩ resistor on I_{SET} generates an internal reference current of 20μA. This current is mirrored internally to generate the bias current for the internal blocks. Using a larger external

resistor at I_{SET} reduces the reference bias current and thereby scales down the device operating power. However, it is recommended that the external resistor be within 10% of the specified value of 56.2k Ω so that the internal bias margins for the various blocks are proper.

Buffering the internal bandgap voltage also generates the common-mode voltage V_{CM} , which is set to the midlevel of REF_T and REF_B , and is accessible on a pin (pin 65 in TQFP-80 package, pin 53 in QFN-64 package). It is meant as a reference voltage to derive the input common-mode if the input is directly coupled. It can also be used to derive the reference common-mode voltage in the external reference mode. The suggested decoupling for the reference pins is shown in [Figure 43](#).

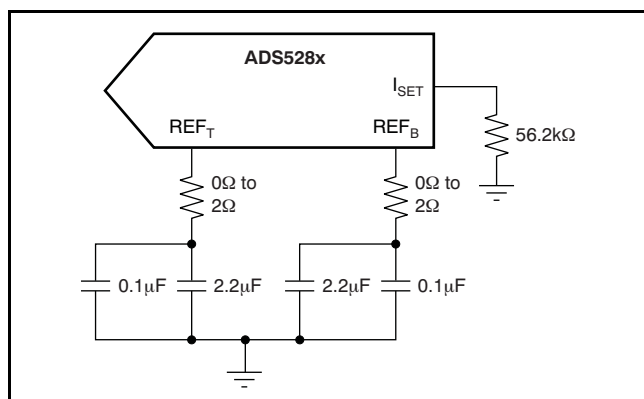


Figure 43. Suggested Decoupling on the Reference Pins

The device also supports the use of external reference voltages. There are two methods to force the references externally. The first method involves pulling INT/EXT low and forcing externally REF_T and REF_B to 2.5V and 0.5V nominally, respectively. In this mode, the internal reference buffer goes to a 3-state output. The external reference driving circuit should be designed to provide the required switching current for the eight ADCs inside the chip. It should be noted that in this mode, V_{CM} and I_{SET} continue to be generated from the internal bandgap voltage, as in the internal reference mode. It is therefore important to ensure that the common-mode voltage of the externally-forced reference voltages matches to within 50mV of V_{CM} .

The second method of forcing the reference voltages externally can be accessed by pulling INT/EXT low, and programming the serial interface to drive the external reference mode through the V_{CM} pin (register bit called EXT_REF_VCM). In this mode, V_{CM} becomes configured as an input pin that can be driven from external circuitry. The internal reference buffers driving REF_T and REF_B are active in this mode. Forcing 1.5V on the V_{CM} pin in the mode results in REF_T and REF_B coming to 2.5V and 0.5V, respectively. In general, the voltages on REF_T and REF_B in this mode are given by [Equation 4](#) and [Equation 5](#), respectively:

$$V_{REF_T} = 1.5V + \frac{V_{CM}}{1.5V} \quad (4)$$

$$V_{REF_B} = 1.5V - \frac{V_{CM}}{1.5V} \quad (5)$$

The state of the reference voltage internal buffers during various combinations of the PD, INT/EXT, and EXT_REF_VCM register bits is described in [Table 8](#).

Table 8. State of Reference Voltages for Various Combinations of PD, INT/EXT, and EXT_REF_VCM

REGISTER BIT	INTERNAL BUFFER STATE							
PD	0	0	1	1	0	0	1	1
INT/EXT	0	1	0	1	0	1	0	1
EXT_REF_VCM	0	0	0	0	1	1	1	1
REF_T buffer	3-state	2.5V	3-state	2.5V ⁽¹⁾	$1.5V + V_{CM}/1.5V$	Do not use	2.5V ⁽¹⁾	Do not use
REF_B buffer	3-state	0.5V	3-state	0.5V ⁽¹⁾	$1.5V - V_{CM}/1.5V$	Do not use	0.5V ⁽¹⁾	Do not use
V_{CM} pin	1.5V	1.5V	1.5V	1.5V	Force	Do not use	Force	Do not use

(1) Weakly forced with reduced strength.

NOISE COUPLING ISSUES

High-speed mixed signals are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffers. Maximum care is taken to isolate these noise sources from the sensitive analog blocks. As a starting point, the analog and digital domains of the device are clearly demarcated. AVDD and AVSS are used to denote the supplies for the analog

sections, while LVDD and LVSS are used to denote the digital supplies. Care is taken to ensure that there is minimal interaction between the supply sets within the device. The extent of noise coupled and transmitted from the digital to the analog sections depends on:

1. The effective inductances of each of the supply and ground sets.
2. The isolation between the digital and analog supply and ground sets.

Smaller effective inductance of the supply and ground pins leads to better noise suppression. For this reason, multiple pins are used to drive each supply and ground. It is also critical to ensure that the impedances of the supply and ground lines on the board are kept to the minimum possible values. Use of ground planes in the printed circuit board (PCB) as well as large decoupling capacitors between the supply and ground lines are necessary to obtain the best possible SNR performance from the device.

It is recommended that the isolation be maintained on the board by using separate supplies to drive AVDD and LVDD, as well as separate ground planes for AVSS and LVSS. The use of LVDS buffers reduces the injected noise considerably, compared to CMOS buffers. The current in the LVDS buffer is independent of the direction of switching. Also, the low output swing as well as the differential nature of the LVDS buffer results in low-noise coupling.

REVISION HISTORY

Changes from Revision G (March 2008) to Revision H	Page
<ul style="list-style-type: none"> Changed second table and conditions in the Initialization Registers section 3 Changed In Input Common-Mode Current section, changed <i>initialization register 5</i> to <i>initialization registers 1 and 5</i> to reflect change in Initialization Registers table 33 	
Changes from Revision F (March 2008) to Revision G	Page
<ul style="list-style-type: none"> Deleted note (3) of Ordering Information table to indicate device status is now Production Data for all parts 2 Added new note (3) of Ordering Information table to indicate the quantity of transport media is available in the Package Option Addendum 2 Added note (1) to Initialization Registers section to indicate it is no longer necessary to program initialization registers 1 to 4 3 Changed maximum specifications for ADS5282 column in the <i>Power Supply—Internal Reference Mode</i> section of Electrical Characteristics (By Device) table 6 Changed minimum specification for ADS5282 column in the <i>f</i> = 10 MHz row of the <i>SNR</i> section of Electrical Characteristics (By Device) table 6 	
Changes from Revision H (March 2008) to Revision I	Page
<ul style="list-style-type: none"> Added table in the INITIALIZATION REGISTERS section 3 Added table in the LVDS OUTPUT TIMING CHARACTERISTICS section 14 Added PLL OPERATION ACROSS SAMPLING FREQUENCY section 36 	

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5281IPFP	Active	Production	HTQFP (PFP) 80	96 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5281I
ADS5281IPFP.A	Active	Production	HTQFP (PFP) 80	96 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5281I
ADS5281IPFPR	Active	Production	HTQFP (PFP) 80	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5281I
ADS5281IPFPR.A	Active	Production	HTQFP (PFP) 80	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5281I
ADS5281IRGCR	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5281
ADS5281IRGCR.A	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5281
ADS5281IRGCT	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5281
ADS5281IRGCT.A	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5281
ADS5282IRGCR	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5282
ADS5282IRGCR.A	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5282
ADS5282IRGCRG4	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5282
ADS5282IRGCRG4.A	Active	Production	VQFN (RGC) 64	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5282
ADS5282IRGCT	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5282
ADS5282IRGCT.A	Active	Production	VQFN (RGC) 64	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5282

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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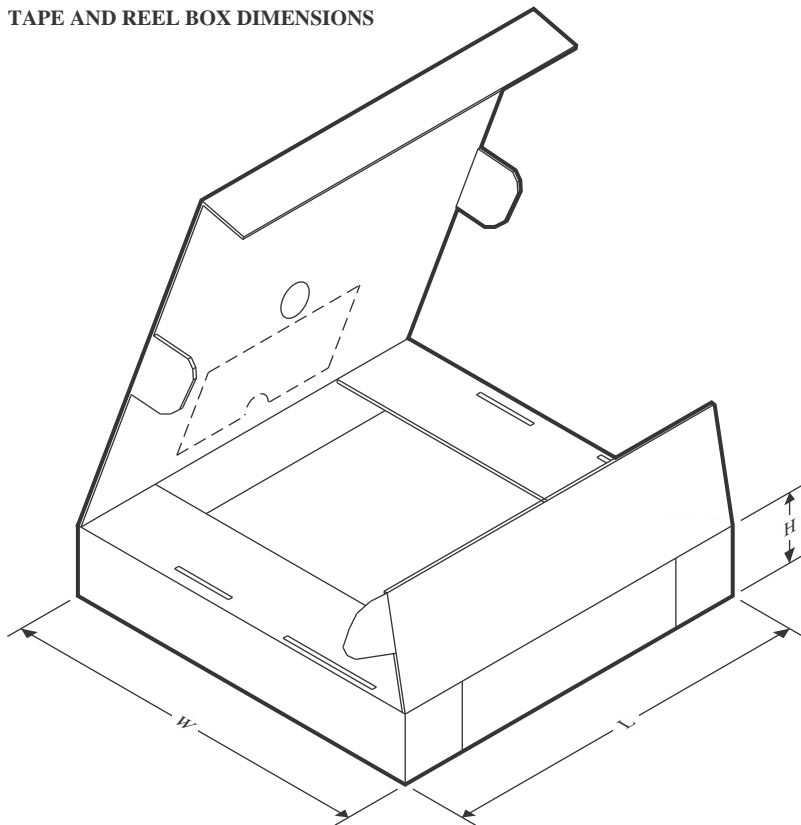
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5281IPFPR	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
ADS5281IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS5282IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS5282IRGCRG4	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

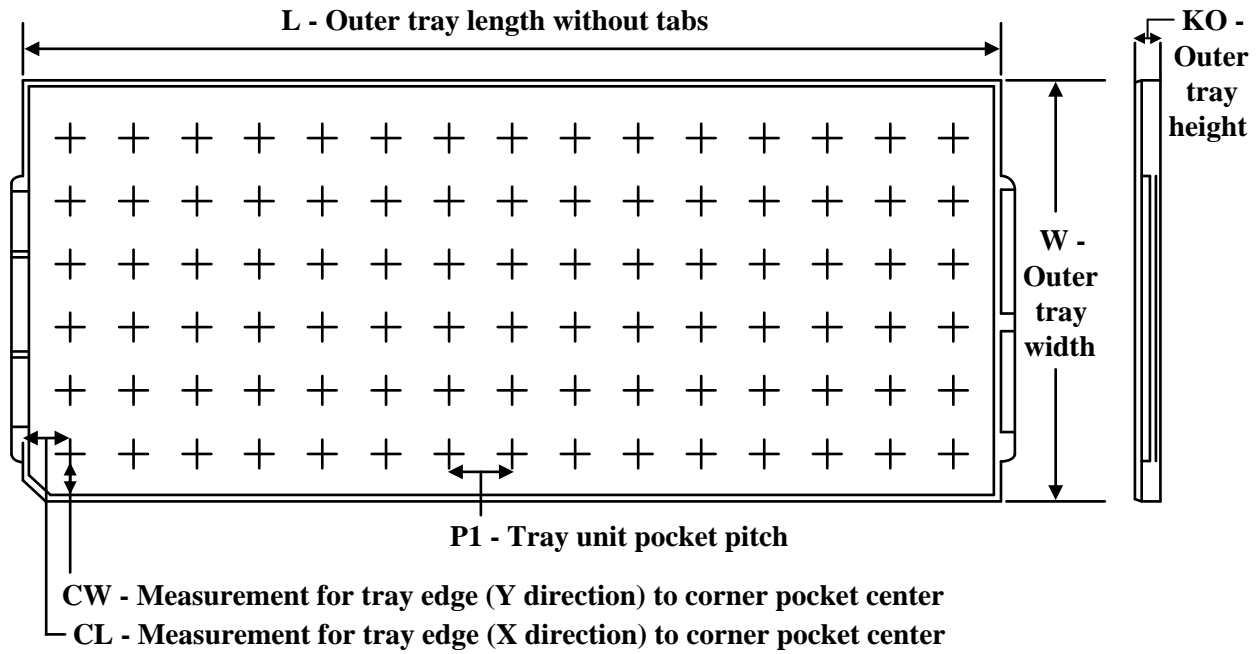
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5281IPFPR	HTQFP	PFP	80	1000	350.0	350.0	43.0
ADS5281IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS5282IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS5282IRGCRG4	VQFN	RGC	64	2000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
ADS5281IPFP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
ADS5281IPFP.A	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3

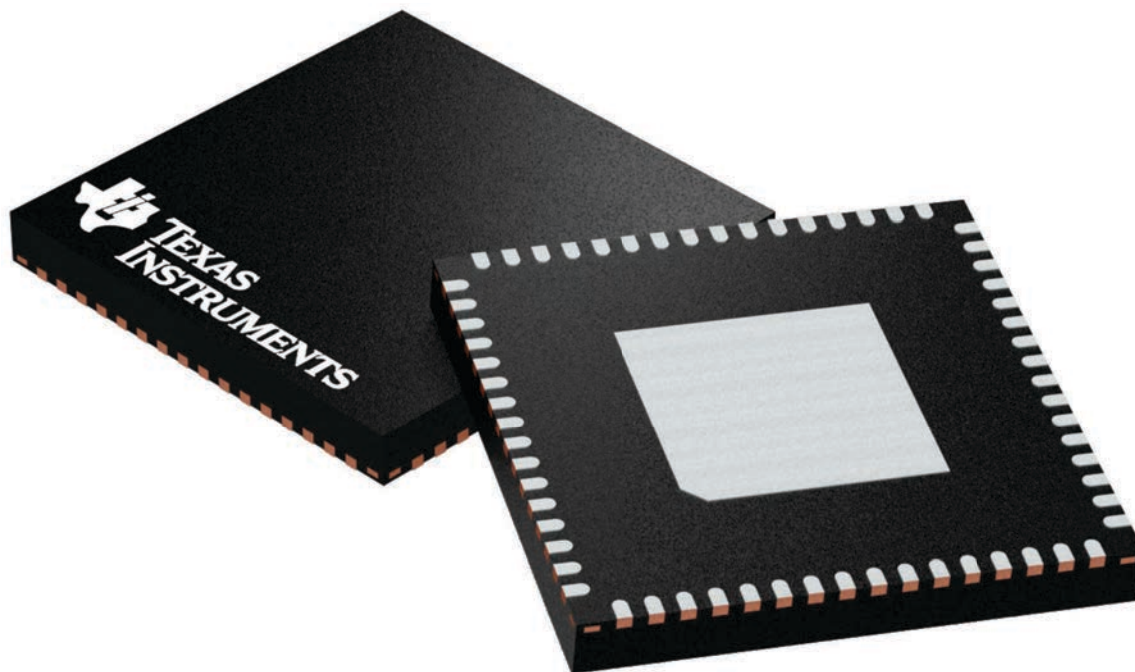
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

VQFN - 1 mm max height

[illegible]

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

VQFN - 1 mm max height

[illegible]

The diagram illustrates two types of solder mask openings on a PCB:

- Non Solder Mask Defined (Preferred):** This type shows a solder mask opening (blue outline) with a metal pad (green outline) inside it. The metal pad is defined by the metal layer, and the solder mask opening is defined by the solder mask. The dimensions are specified as 0.07 MAX ALL AROUND.
- Solder Mask Defined:** This type shows a solder mask opening (blue outline) with a metal pad (green outline) inside it. The metal pad is defined by the metal layer, and the solder mask opening is defined by the solder mask. The dimensions are specified as 0.07 MIN ALL AROUND.

4219009/A 10/2018

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

VQFN - 1 mm max height

SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

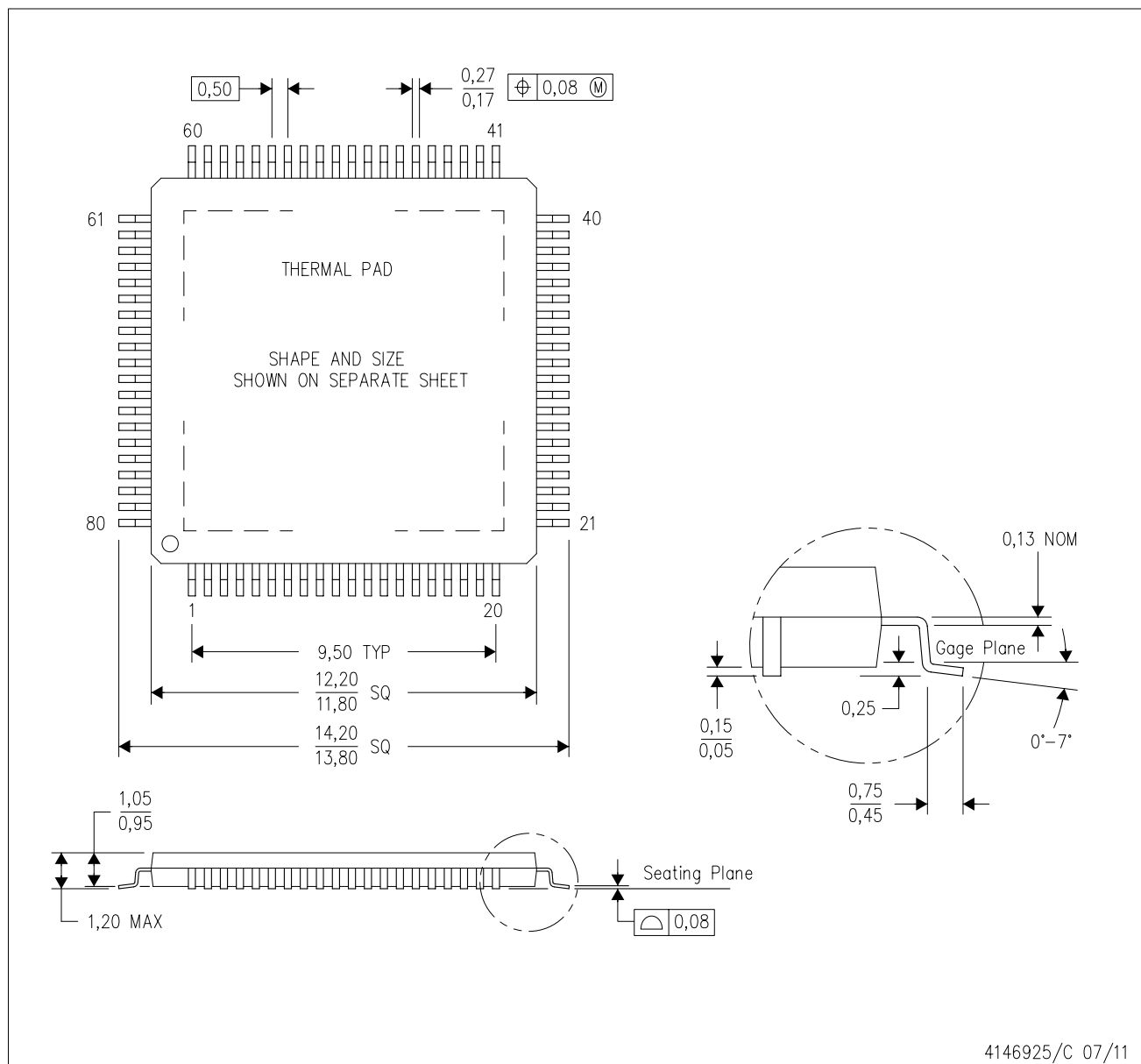
EXPOSED PAD
 60% PRINTED COVERAGE BY AREA
 SCALE: 12X

4219009/A 10/2018

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



4146925/C 07/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PFP (S-PQFP-G80)

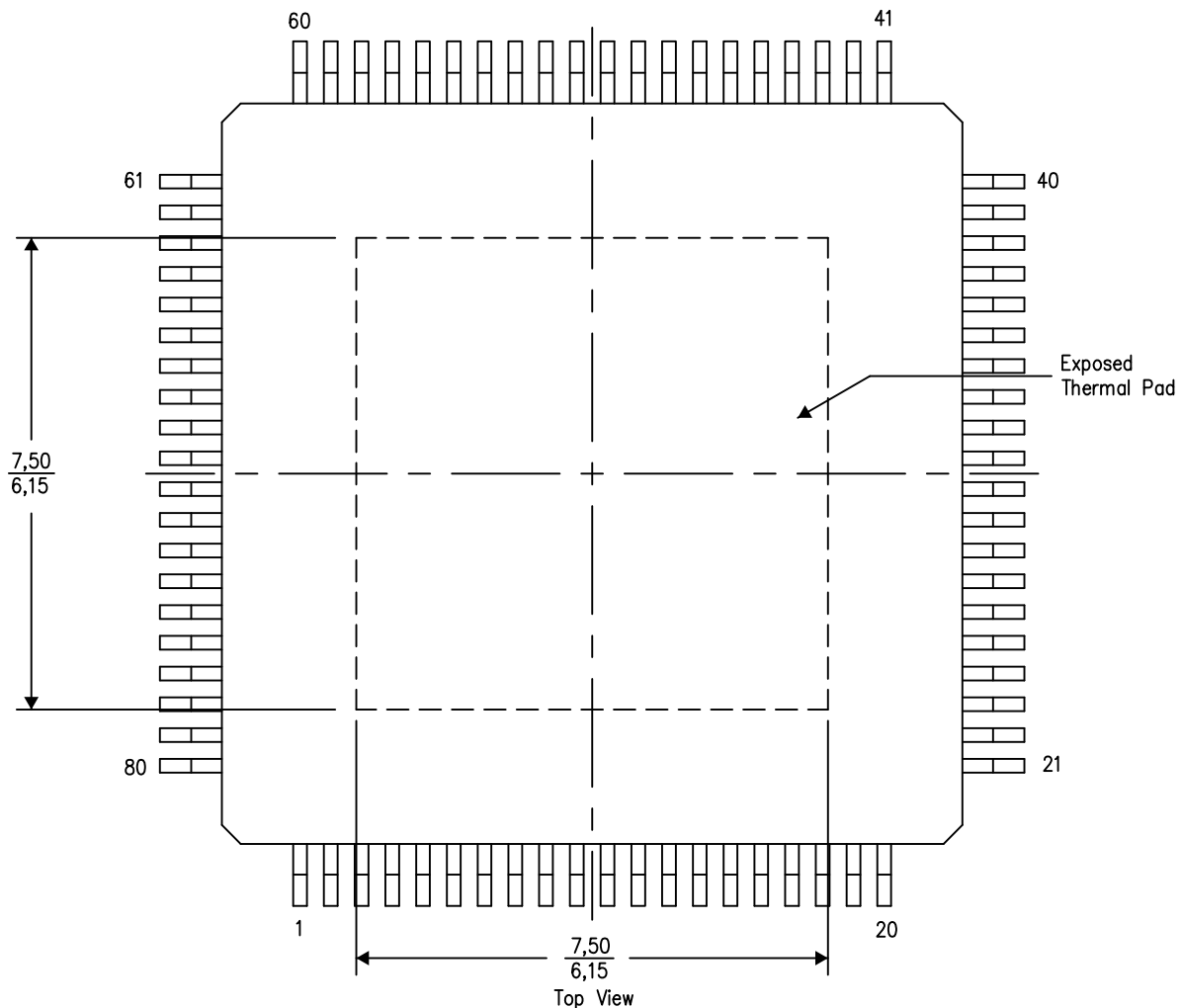
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206327-2/P 05/14

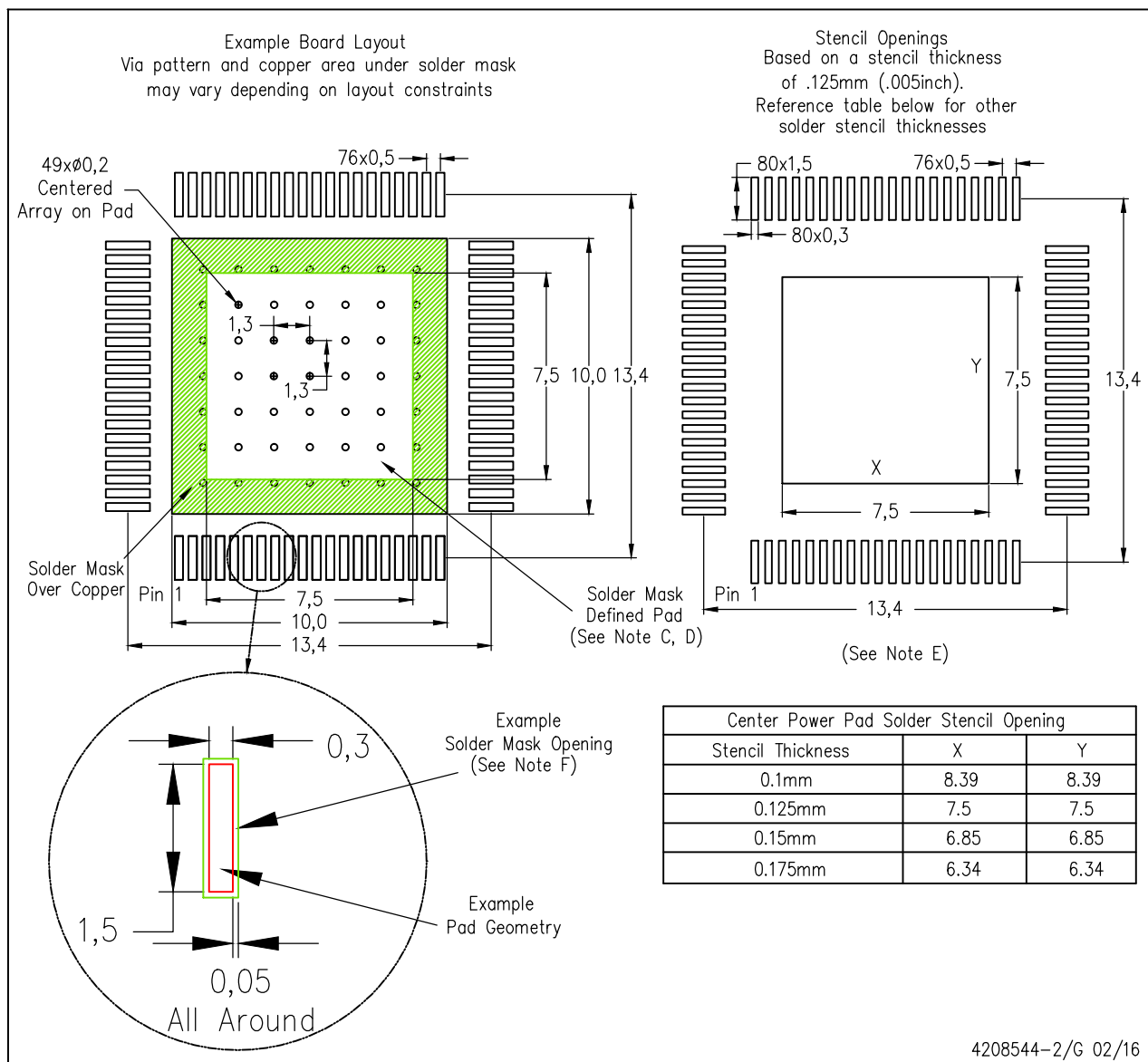
NOTE: A. All linear dimensions are in millimeters

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LAND PATTERN DATA

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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