Data Sheet, V0.1, Feb. 2000

TC1775

32-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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TC1775
Advance Information
Revision History: **2000-02** V0.1

Previous Version: -

Page	Subjects (major changes since last revision)

Controller Area Network (CAN): License of Robert Bosch GmbH

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Advance Information

- High Performance 32-bit TriCore CPU with 4-Stage Pipeline
  - 50 ns Instruction Cycle Time at 40 MHz CPU Clock
- Dual Issue super-scalar implementation
  - MAC instruction triple issue
- Circular Buffer and bit-reverse addressing modes for DSP algorithms
- Flexible multi-master interrupt system
- Very fast interrupt response time
- Hardware controlled context switch for task switch and interrupts
- 72 kByte of on-chip SRAM for data and time critical code
- Independent Peripheral Control Processor (PCP) for low level driver support with 20 kByte code/parameter memory
- Built-in calibration support
- On-chip Flexible Peripheral Interface Bus (FPI-Bus) for interconnections of functional units
- Flexible External Bus Interface Unit (EBU) used for
  - communication with external data memories and peripheral units
  - instruction fetches from external Burst Flash program memories
- On-Chip Peripheral Units
  - General Purpose Timer Array (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex I/O management
  - Multifunctional General Purpose Timer Unit (GPTU) with three 32-bit timer/counters
  - Two Asynchronous/Synchronous Serial Channels (ASC0, ASC1) with baudrate generator, parity, framing and overrun error detection
  - Two High Speed Synchronous Serial Channels (SSC0, SSC1) with programmable data length and shift direction
  - TwinCAN Module with two interconnected CAN nodes for high efficiency data handling via FIFO buffering and gateway data transfer
  - Serial Data Link Module (SDLM) compliant to SAE Class B J1850 specification
  - Two Analog-to-Digital Converter Units (ADC0, ADC1) with 8-bit, 10-bit, or 12-bit resolution and 16 analog inputs each
  - Watchdog Timer and System Timer
  - Real Time Clock
- Eleven 16-bit digital I/O ports and two 16-bit analog ports
- On-chip Debug Support
- Power Management System
- Clock Generation Unit with PLL
- Ambient temperature under bias: -40° to +125°C
- P-BGA-329 package

Advance Information

Logic Symbol

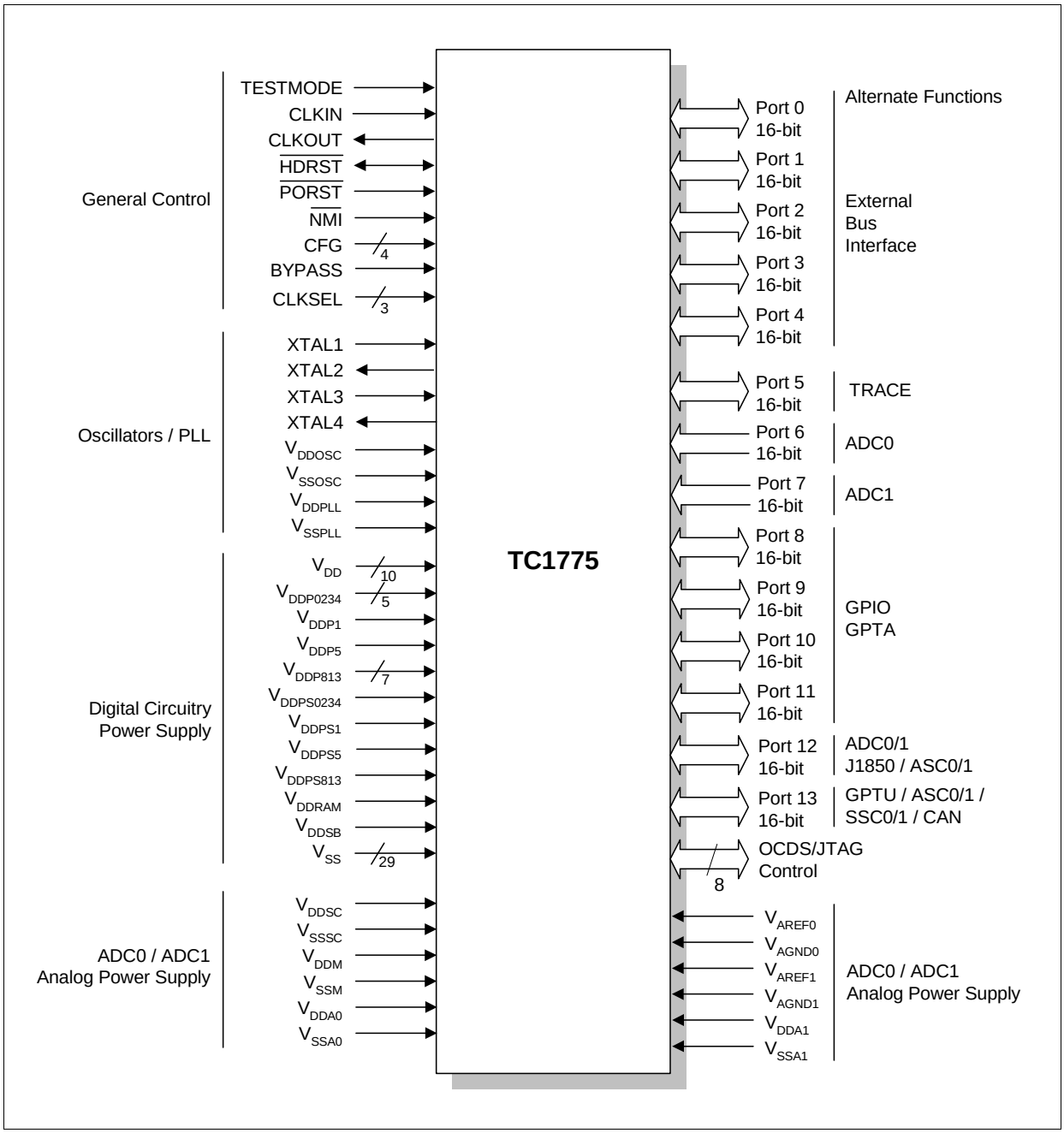
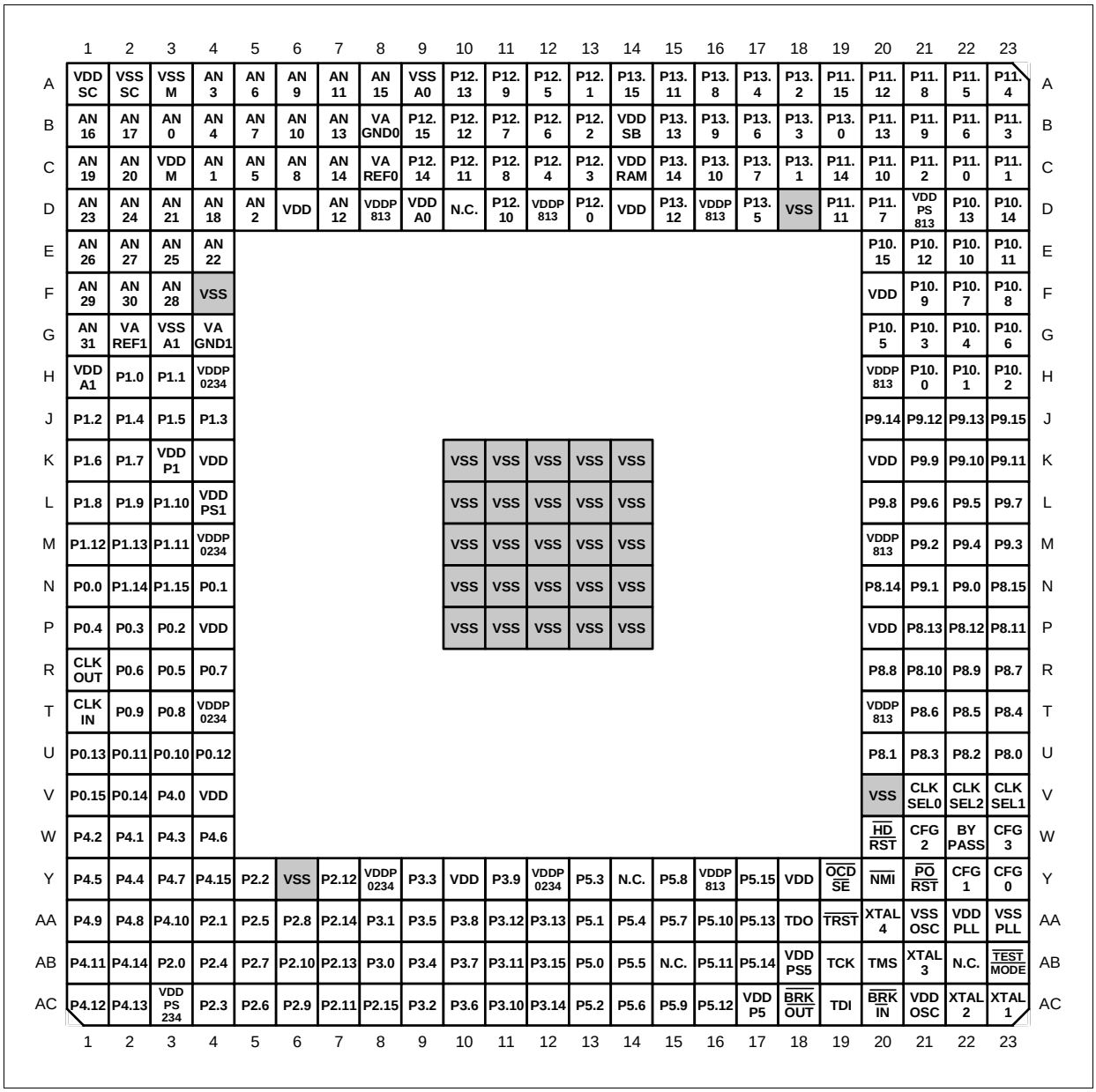


Figure 1 TC1775 Logic Symbol

Advance Information

Pin Configuration



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	VDD SC	VSS SC	VSS M	AN 3	AN 6	AN 9	AN 11	AN 15	VSS A0	P12. 13	P12. 9	P12. 5	P12. 1	P13. 15	P13. 11	P13. 8	P13. 4	P13. 2	P11. 15	P11. 12	P11. 8	P11. 5	P11. 4	A
B	AN 16	AN 17	AN 0	AN 4	AN 7	AN 10	AN 13	VA GND0	P12. 15	P12. 12	P12. 7	P12. 6	P12. 2	VDD SB	P13. 13	P13. 9	P13. 6	P13. 3	P13. 0	P11. 13	P11. 9	P11. 6	P11. 3	B
C	AN 19	AN 20	VDD M	AN 1	AN 5	AN 8	AN 14	VA REF0	P12. 14	P12. 11	P12. 8	P12. 4	P12. 3	VDD RAM	P13. 14	P13. 10	P13. 7	P13. 1	P11. 14	P11. 10	P11. 2	P11. 0	P11. 1	C
D	AN 23	AN 24	AN 21	AN 18	AN 2	VDD	AN 12	VDDP 813	VDD A0	N.C.	P12. 10	VDDP 813	P12. 0	VDD	P13. 12	VDDP 813	P13. 5	VSS	P11. 11	P11. 7	VDD PS 813	P10. 13	P10. 14	D
E	AN 26	AN 27	AN 25	AN 22																P10. 15	P10. 12	P10. 10	P10. 11	E
F	AN 29	AN 30	AN 28	VSS																VDD	P10. 9	P10. 7	P10. 8	F
G	AN 31	VA REF1	VSS A1	VA GND1																P10. 5	P10. 3	P10. 4	P10. 6	G
H	VDD A1	P1.0	P1.1	VDDP 0234																VDDP 813	P10. 0	P10. 1	P10. 2	H
J	P1.2	P1.4	P1.5	P1.3																P9.14	P9.12	P9.13	P9.15	J
K	P1.6	P1.7	VDD P1	VDD						VSS	VSS	VSS	VSS	VSS						VDD	P9.9	P9.10	P9.11	K
L	P1.8	P1.9	P1.10	VDD PS1						VSS	VSS	VSS	VSS	VSS						P9.8	P9.6	P9.5	P9.7	L
M	P1.12	P1.13	P1.11	VDDP 0234						VSS	VSS	VSS	VSS	VSS						VDDP 813	P9.2	P9.4	P9.3	M
N	P0.0	P1.14	P1.15	P0.1						VSS	VSS	VSS	VSS	VSS						P8.14	P9.1	P9.0	P8.15	N
P	P0.4	P0.3	P0.2	VDD						VSS	VSS	VSS	VSS	VSS						VDD	P8.13	P8.12	P8.11	P
R	CLK OUT	P0.6	P0.5	P0.7																P8.8	P8.10	P8.9	P8.7	R
T	CLK IN	P0.9	P0.8	VDDP 0234																VDDP 813	P8.6	P8.5	P8.4	T
U	P0.13	P0.11	P0.10	P0.12																P8.1	P8.3	P8.2	P8.0	U
V	P0.15	P0.14	P4.0	VDD																VSS	CLK SEL0	CLK SEL2	CLK SEL1	V
W	P4.2	P4.1	P4.3	P4.6																HD RST	CFG 2	BY PASS	CFG 3	W
Y	P4.5	P4.4	P4.7	P4.15	P2.2	VSS	P2.12	VDDP 0234	P3.3	VDD	P3.9	VDDP 0234	P5.3	N.C.	P5.8	VDDP 813	P5.15	VDD	OCD SE	NMI	PO RST	CFG 1	CFG 0	Y
AA	P4.9	P4.8	P4.10	P2.1	P2.5	P2.8	P2.14	P3.1	P3.5	P3.8	P3.12	P3.13	P5.1	P5.4	P5.7	P5.10	P5.13	TDO	TRST	XTAL 4	VSS OSC	VDD PLL	VSS PLL	AA
AB	P4.11	P4.14	P2.0	P2.4	P2.7	P2.10	P2.13	P3.0	P3.4	P3.7	P3.11	P3.15	P5.0	P5.5	N.C.	P5.11	P5.14	VDD PS5	TCK	TMS	XTAL 3	N.C.	TEST MODE	AB
AC	P4.12	P4.13	VDD PS 234	P2.3	P2.6	P2.9	P2.11	P2.15	P3.2	P3.6	P3.10	P3.14	P5.2	P5.6	P5.9	P5.12	VDD P5	BRK OUT	TDI	BRK IN	VDD OSC	XTAL 2	XTAL 1	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Figure 2 TC1775 Pin Configuration P-BGA-329 Package (Top view)

Table 1 Pin Definitions and Functions

Symbol	Pin	In Out	Functions
P0		I/O	**Port 0** Port 0 serves as 16-bit general purpose I/O port or as lower external address/data bus AD[15:0] (multiplexed bus mode) or data bus D[15:0] (demultiplexed bus mode) for the EBU. Port 0 is used as data input by an external bus master when accessing modules on the internal FPI-Bus.
P0.0	N1	I/O	AD0 / D0 Address/data bus line 0 / Data bus line 0
P0.1	N4	I/O	AD1 / D1 Address/data bus line 1/ Data bus line 1
P0.2	P3	I/O	AD2 / D2 Address/data bus line 2 / Data bus line 2
P0.3	P2	I/O	AD3 / D3 Address/data bus line 3 / Data bus line 3
P0.4	P1	I/O	AD4 / D4 Address/data bus line 4 / Data bus line 4
P0.5	R3	I/O	AD5 / D5 Address/data bus line 5 / Data bus line 5
P0.6	R2	I/O	AD6 / D6 Address/data bus line 6 / Data bus line 6
P0.7	R4	I/O	AD7 / D7 Address/data bus line 7 / Data bus line 7
P0.8	T3	I/O	AD8 / D8 Address/data bus line 8 / Data bus line 8
P0.9	T2	I/O	AD9 / D9 Address/data bus line 9 / Data bus line 9
P0.10	U3	I/O	AD10 / D10 Address/data bus line 10 / Data bus line 10
P0.11	U2	I/O	AD11 / D11 Address/data bus line 11 / Data bus line 11
P0.12	U4	I/O	AD12 / D12 Address/data bus line 12 / Data bus line 12
P0.13	U1	I/O	AD13 / D13 Address/data bus line 13 / Data bus line 13
P0.14	V2	I/O	AD14 / D14 Address/data bus line 14 / Data bus line 14
P0.15	V1	I/O	AD15 / D15 Address/data bus line 15 / Data bus line 15

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P1		I/O	**Port 1** Port 1 serves as 16-bit general purpose I/O port or as upper external address/data bus AD[31:16] (multiplexed bus mode) or data bus D[31:16] (demultiplexed bus mode) for the EBU. Port 1 is used as data input by an external bus master when accessing modules on the internal FPI-Bus.
P1.0	H2	I/O	AD16 / D16 Address/data bus line 16 / Data bus line 16
P1.1	H3	I/O	AD17 / D17 Address/data bus line 17/ Data bus line 17
P1.2	J1	I/O	AD18 / D18 Address/data bus line 18 / Data bus line 18
P1.3	J4	I/O	AD19 / D19 Address/data bus line 19 / Data bus line 19
P1.4	J2	I/O	AD20 / D20 Address/data bus line 20 / Data bus line 20
P1.5	J3	I/O	AD21 / D21 Address/data bus line 21 / Data bus line 21
P1.6	K1	I/O	AD22 / D22 Address/data bus line 22 / Data bus line 22
P1.7	K2	I/O	AD23 / D23 Address/data bus line 23 / Data bus line 23
P1.8	L1	I/O	AD24 / D24 Address/data bus line 24 / Data bus line 24
P1.9	L2	I/O	AD25 / D25 Address/data bus line 25 / Data bus line 25
P1.10	L3	I/O	AD26 / D26 Address/data bus line 26 / Data bus line 26
P1.11	M3	I/O	AD27 / D27 Address/data bus line 27 / Data bus line 27
P1.12	M1	I/O	AD28 / D28 Address/data bus line 28 / Data bus line 28
P1.13	M2	I/O	AD29 / D29 Address/data bus line 29 / Data bus line 29
P1.14	N2	I/O	AD30 / D30 Address/data bus line 30 / Data bus line 30
P1.15	N3	I/O	AD31 / D31 Address/data bus line 31 / Data bus line 31

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P2		I/O	**Port 2** Port 2 serves as 16-bit general purpose I/O port or as lower external address bus for the EBU. When used as address bus, it outputs the addresses A[15:0] of an external access in both, multiplexed and demultiplexed bus mode. Port 2 is used as address input by an external bus master when accessing modules on the internal FPI-Bus.
P2.0	AB3	I/O	A0 Address bus line 0
P2.1	AA4	I/O	A1 Address bus line 1
P2.2	Y5	I/O	A2 Address bus line 2
P2.3	AC4	I/O	A3 Address bus line 3
P2.4	AB4	I/O	A4 Address bus line 4
P2.5	AA5	I/O	A5 Address bus line 5
P2.6	AC5	I/O	A6 Address bus line 6
P2.7	AB5	I/O	A7 Address bus line 7
P2.8	AA6	I/O	A8 Address bus line 8
P2.9	AC6	I/O	A9 Address bus line 9
P2.10	AB6	I/O	A10 Address bus line 10
P2.11	AC7	I/O	A11 Address bus line 11
P2.12	Y7	I/O	A12 Address bus line 12
P2.13	AB7	I/O	A13 Address bus line 13
P2.14	AA7	I/O	A14 Address bus line 14
P2.15	AC8	I/O	A15 Address bus line 15

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P3		I/O	**Port 3** P3[9:0] serves as 16-bit general purpose I/O port or as upper external address bus for the EBU. When used as address bus, it outputs the addresses A[25:16] of an external access in both, multiplexed and demultiplexed bus mode. P3[9:0] is used as address input by an external bus master when accessing modules on the internal FPI-Bus. Port 3 also provides chip select output lines $\overline{CS0}$-$\overline{CS3}$, $\overline{CSEMU}$, and $\overline{CSOVL}$.
P3.0	AB8	I/O	A16 Address bus line 16
P3.1	AA8	I/O	A17 Address bus line 17
P3.2	AC9	I/O	A18 Address bus line 18
P3.3	Y9	I/O	A19 Address bus line 19
P3.4	AB9	I/O	A20 Address bus line 20
P3.5	AA9	I/O	A21 Address bus line 21
P3.6	AC10	I/O	A22 Address bus line 22
P3.7	AB10	I/O	A23 Address bus line 23
P3.8	AA10	I/O	A24 Address bus line 24
P3.9	Y11	I/O	$\overline{A25}$ Address bus line 25
P3.10	AC11	O	$\overline{CS3}$ Chip select output line 3
P3.11	AB11	O	$\overline{CS2}$ Chip select output line 2
P3.12	AA11	O	$\overline{CS1}$ Chip select output line 1
P3.13	AA12	O	$\overline{CS0}$ Chip select output line 0
P3.14	AC12	O	$\overline{CSEMU}$ Chip select output for emulator region
P3.15	AB12	O	$\overline{CSOVL}$ Chip select output for emulator overlay memory

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P4		I/O	**Port 4** Port 4 is used as general purpose I/O port but also serves as control bus for the EBU control lines.
P4.0	V3	I/O	$\overline{RD}$ Read control line
P4.1	W2	I/O	RD/$\overline{WR}$ Write control line
P4.2	W1	O	$\overline{ALE}$ Address latch enable output
P4.3	W3	O	$\overline{ADV}$ Address valid output
P4.4	Y2	I/O	$\overline{BC0}$ Byte control line 0
P4.5	Y1	I/O	$\overline{BC1}$ Byte control line 1
P4.6	W4	I/O	$\overline{BC2}$ Byte control line 2
P4.7	Y3	I/O	$\overline{BC3}$ Byte control line 3
P4.8	AA2	I	$\overline{WAIT}$/$\overline{IND}$ Wait input / End of burst input
P4.9	AA1	O	$\overline{BAA}$ Burst address advance output
P4.10	AA3	I	$\overline{CSFPI}$ Chip select FPI input
P4.11	AB1	I	$\overline{HOLD}$ Hold request input
P4.12	AC1	I/O	$\overline{HLDA}$ Hold acknowledge input/output
P4.13	AC2	O	$\overline{BREQ}$ Bus request output
P4.14	AB2	O	$\overline{CODE}$ Code fetch status output
P4.15	Y4	O	SVM Supervisor mode output The $\overline{CODE}$ signal has the same timing as the $\overline{CSx}$ signals which are located at port 3.

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P5		I/O	**Port 5** Port 5 serves as 16-bit general purpose I/O port or as CPU or PCP trace output port for the OCDS logic.	
P5.0	AB13	O	TRACE0	CPU or PCP trace outputs 0
P5.1	AA13	O	TRACE1	CPU or PCP trace outputs 1
P5.2	AC13	O	TRACE2	CPU or PCP trace outputs 2
P5.3	Y13	O	TRACE3	CPU or PCP trace outputs 3
P5.4	AA14	O	TRACE4	CPU or PCP trace outputs 4
P5.5	AB14	O	TRACE5	CPU or PCP trace outputs 5
P5.6	AC14	O	TRACE6	CPU or PCP trace outputs 6
P5.7	AA15	O	TRACE7	CPU or PCP trace outputs 7
P5.8	Y15	O	TRACE8	CPU or PCP trace outputs 8
P5.9	AC15	O	TRACE9	CPU or PCP trace outputs 9
P5.10	AA16	O	TRACE10	CPU or PCP trace outputs 10
P5.11	AB16	O	TRACE11	CPU or PCP trace outputs 11
P5.12	AC16	O	TRACE12	CPU or PCP trace outputs 12
P5.13	AA17	O	TRACE13	CPU or PCP trace outputs 13
P5.14	AB17	O	TRACE14	CPU or PCP trace outputs 14
P5.15	Y17	O	TRACE15	CPU or PCP trace outputs 15

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P6		I	**Port 6** Port 6 provides the analog input lines for the AD Converter 0 (ADC0).	
P6.0	B3	I	AN0	Analog inputs 0
P6.1	C4	I	AN1	Analog inputs 1
P6.2	D5	I	AN2	Analog inputs 2
P6.3	A4	I	AN3	Analog inputs 3
P6.4	B4	I	AN4	Analog inputs 4
P6.5	C5	I	AN5	Analog inputs 5
P6.6	A5	I	AN6	Analog inputs 6
P6.7	B5	I	AN7	Analog inputs 7
P6.8	C6	I	AN8	Analog inputs 8
P6.9	A6	I	AN9	Analog inputs 9
P6.10	B6	I	AN10	Analog inputs 10
P6.11	A7	I	AN11	Analog inputs 11
P6.12	D7	I	AN12	Analog inputs 12
P6.13	B7	I	AN13	Analog inputs 13
P6.14	C7	I	AN14	Analog inputs 14
P6.15	A8	I	AN15	Analog inputs 15
P7		I	**Port 7** Port 7 provides the analog input lines for the AD Converter 1 (ADC1).	
P7.0	B1	I	AN16	Analog inputs 16
P7.1	B2	I	AN17	Analog inputs 17
P7.2	D4	I	AN18	Analog inputs 18
P7.3	C1	I	AN19	Analog inputs 19
P7.4	C2	I	AN20	Analog inputs 20
P7.5	D3	I	AN21	Analog inputs 21
P7.6	E4	I	AN22	Analog inputs 22
P7.7	D1	I	AN23	Analog inputs 23
P7.8	D2	I	AN24	Analog inputs 24
P7.9	E3	I	AN25	Analog inputs 25
P7.10	E1	I	AN26	Analog inputs 26
P7.11	E2	I	AN27	Analog inputs 27
P7.12	F3	I	AN28	Analog inputs 28
P7.13	F1	I	AN29	Analog inputs 29
P7.14	F2	I	AN30	Analog inputs 30
P7.15	G1	I	AN31	Analog inputs 31

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P8		I/O	**Port 8** Port 8 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P8.0	U23	I/O	IN0 / OUT0 line of GPTA
P8.1	U20	I/O	IN1 / OUT1 line of GPTA
P8.2	U22	I/O	IN2 / OUT2 line of GPTA
P8.3	U21	I/O	IN3 / OUT3 line of GPTA
P8.4	T23	I/O	IN4 / OUT4 line of GPTA
P8.5	T22	I/O	IN5 / OUT5 line of GPTA
P8.6	T21	I/O	IN6 / OUT6 line of GPTA
P8.7	R23	I/O	IN7 / OUT7 line of GPTA
P8.8	R20	I/O	IN8 / OUT8 line of GPTA
P8.9	R22	I/O	IN9 / OUT9 line of GPTA
P8.10	R21	I/O	IN10 / OUT10 line of GPTA
P8.11	P23	I/O	IN11 / OUT11 line of GPTA
P8.12	P22	I/O	IN12 / OUT12 line of GPTA
P8.13	P21	I/O	IN13 / OUT13 line of GPTA
P8.14	N20	I/O	IN14 / OUT14 line of GPTA
P8.15	N23	I/O	IN15 / OUT15 line of GPTA
P9		I/O	**Port 9** Port 9 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P9.0	N22	I/O	IN16 / OUT16 line of GPTA
P9.1	N21	I/O	IN17 / OUT17 line of GPTA
P9.2	M21	I/O	IN18 / OUT18 line of GPTA
P9.3	M23	I/O	IN19 / OUT19 line of GPTA
P9.4	M22	I/O	IN20 / OUT20 line of GPTA
P9.5	L22	I/O	IN21 / OUT21 line of GPTA
P9.6	L21	I/O	IN22 / OUT22 line of GPTA
P9.7	L23	I/O	IN23 / OUT23 line of GPTA
P9.8	L20	I/O	IN24 / OUT24 line of GPTA
P9.9	K21	I/O	IN25 / OUT25 line of GPTA
P9.10	K22	I/O	IN26 / OUT26 line of GPTA
P9.11	K23	I/O	IN27 / OUT27 line of GPTA
P9.12	J21	I/O	IN28 / OUT28 line of GPTA
P9.13	J22	I/O	IN29 / OUT29 line of GPTA
P9.14	J20	I/O	IN30 / OUT30 line of GPTA
P9.15	J23	I/O	IN31 / OUT31 line of GPTA

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P10		I/O	**Port 10** Port 10 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P10.0	H21	I/O	IN32 / OUT32 line of GPTA
P10.1	H22	I/O	IN33 / OUT33 line of GPTA
P10.2	H23	I/O	IN34 / OUT34 line of GPTA
P10.3	G21	I/O	IN35 / OUT35 line of GPTA
P10.4	G22	I/O	IN36 / OUT36 line of GPTA
P10.5	G20	I/O	IN37 / OUT37 line of GPTA
P10.6	G23	I/O	IN38 / OUT38 line of GPTA
P10.7	F22	I/O	IN39 / OUT39 line of GPTA
P10.8	F23	I/O	IN40 / OUT40 line of GPTA
P10.9	F21	I/O	IN41 / OUT41 line of GPTA
P10.10	E22	I/O	IN42 / OUT42 line of GPTA
P10.11	E23	I/O	IN43 / OUT43 line of GPTA
P10.12	E21	I/O	IN44 / OUT44 line of GPTA
P10.13	D22	I/O	IN45 / OUT45 line of GPTA
P10.14	D23	I/O	IN46 / OUT46 line of GPTA
P10.15	E20	I/O	IN47 / OUT47 line of GPTA
P11		I/O	**Port 11** Port 11 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P11.0	C22	I/O	IN48 / OUT48 line of GPTA
P11.1	C23	I/O	IN49 / OUT49 line of GPTA
P11.2	C21	I/O	IN50 / OUT50 line of GPTA
P11.3	B23	I/O	IN51 / OUT51 line of GPTA
P11.4	A23	I/O	IN52 / OUT52 line of GPTA
P11.5	A22	I/O	IN53 / OUT53 line of GPTA
P11.6	B22	I/O	IN54 / OUT54 line of GPTA
P11.7	D20	I/O	IN55 / OUT55 line of GPTA
P11.8	A21	I/O	IN56 / OUT56 line of GPTA
P11.9	B21	I/O	IN57 / OUT57 line of GPTA
P11.10	C20	I/O	IN58 / OUT58 line of GPTA
P11.11	D19	I/O	IN59 / OUT59 line of GPTA
P11.12	A20	I/O	IN60 / OUT60 line of GPTA
P11.13	B20	I/O	IN61 / OUT61 line of GPTA
P11.14	C19	I/O	IN62 / OUT62 line of GPTA
P11.15	A19	I/O	IN63 / OUT63 line of GPTA

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P12		I/O	**Port 12** Port 12 is a 16-bit bidirectional general purpose I/O port or serves as ADC control port and SDLM/ASC I/O port.
P12.0	D13	O	AD0EMUX0 ADC0 external multiplexer control 0
P12.1	A13	O	AD0EMUX1 ADC0 external multiplexer control 1
P12.2	B13	O	AD0EMUX2 ADC0 external multiplexer control 2
P12.3	C13	O	AD1EMUX0 ADC1 external multiplexer control 0
P12.4	C12	O	AD1EMUX1 ADC1 external multiplexer control 1
P12.5	A12	O	AD1EMUX2 ADC1 external multiplexer control 2
P12.6	B12	I	AD1EXTIN0 ADC1 external trigger input 0
P12.7	B11	I	AD1EXTIN1 ADC1 external trigger input 1
P12.8	C11	I	AD0EXTIN0 ADC0 external trigger input 0
P12.9	A11	I	AD0EXTIN1 ADC0 external trigger input 1
P12.10	D11	I	RXJ1850 SDLM receiver input
P12.11	C10	O	TXJ1850 SDLM transmitter output
P12.12	B10	I/O	RXD0A ASC0 receiver input/output A
P12.13	A10	O	TXD0A ASC0 transmitter output A
P12.14	C9	I/O	RXD1A ASC1 receiver input/output A
P12.15	B9	O	TXD1A ASC1 transmitter output A

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P13		I/O	**Port 13** Port 13 is a 16-bit bidirectional general purpose I/O port which is also used as input/output for the serial interfaces (ASC, SSC, CAN) and timers (GPTU).	
P13.0	B19	I/O	GPT0	GPTU I/O line 0
P13.1	C18	I/O	GPT1	GPTU I/O line 1
P13.2	A18	I/O	GPT2	GPTU I/O line 2
		I/O	RXD0B	ASC0 receiver input/output B
P13.3	B18	I/O	GPT3	GPTU I/O line 3
		O	TXD0B	ASC0 transmitter output B
P13.4	A17	I/O	GPT4	GPTU I/O line 4
		I/O	RXD1B	ASC1 receiver input/output B
P13.5	D17	I/O	GPT5	GPTU I/O line 5
		O	TXD1B	ASC1 transmitter output B
P13.6	B17	I/O	GPT6	GPTU I/O line 6
		I/O	SCLK0	SSC0 clock input/output
P13.7	C17	I/O	GPT7	GPTU I/O line 7
		I/O	MRST0	SSC0 master receive / slave transmit input/output
P13.8	A16	I/O	MTSR0	SSC0 master transmit / slave receive output/input
P13.9	B16	I/O	SCLK1	SSC1 clock input/output
P13.10	C16	I/O	MRST1	SSC1 master receive / slave transmit input/output
P13.11	A15	I/O	MTSR1	SSC1 master transmit / slave receive output/input
P13.12	D15	I	RXDCAN0	CAN receiver input 0
P13.13	B15	O	TXDCAN0	CAN transmitter output 0
P13.14	C15	I	RXDCAN1	CAN receiver input 1
P13.15	A14	O	TXDCAN1	CAN transmitter output 1
CLKSEL0 **CLKSEL1** **CLKSEL2**	V21 V23 V22	I I I	**PLL Clock Selection Inputs** These pins are sampled during power-on reset ($\overline{\text{PORST}}$ = low) and determine the division rate in the feedback path of the PLL (N-Factor). The latched values of these input pins are available into the PLL Clock Control Register PLL_CLC. Test modes are selected with CLKSEL[2:0] = 000_B and BYPASS=1.	

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
BYPASS	W22	I	**PLL Bypass Control Input** BYPASS is used for direct drive mode operation of the clock circuitry and for test mode selection. This pin is sampled during power-on reset ($\overline{\text{PORST}}$ = low). Its level is latched into the PLL Clock Control Register PLL_CLC.
CFG0 **CFG1** **CFG2** **CFG3**	Y23 Y22 W21 W23	I I I I	**Operation Configuration Inputs** The configuration inputs define the boot options of the TC1775 after a hardware reset operation.
$\overline{\text{TRST}}$	AA19	I	**JTAG Module Reset/Enable Input** A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.
TCK	AB19	I	**JTAG Module Clock Input**
TDI	AC19	I	**JTAG Module Serial Data Input**
TDO	AA18	O	**JTAG Module Serial Data Output**
TMS	AB20	I	**JTAG Module State Machine Control Input**
$\overline{\text{OCDSE}}$	Y19	I	**OCDS Enable Input** A low level on this pin during power-on reset ($\overline{\text{PORST}}$ = low) enables the on-chip debug support (OCDS). In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{BRKIN}}$	AC20	I	**OCDS Break Input** A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{BRKOUT}}$	AC18	O	**OCDS Break Output** A low level on this pin indicates that a programmable OCDS event has occurred.
$\overline{\text{NMI}}$	Y20	I	**Non-Maskable Interrupt Input** A high-to-low transition on this pin causes a NMI-Trap request to the CPU.

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
$\overline{\text{HDRST}}$	W20	I/O	**Hardware Reset Input / Reset Indication Output** Assertion of this open-drain bidirectional pin causes a synchronous reset of the chip through external circuitry. This pin must be driven for minimum duration of (tbd). The internal reset circuitry drives this pin in response to a power-on, hardware, watchdog and power-down wake-up reset. For a software reset, it is programmable whether this pin is activated or not. The pin is driven by the internal reset circuitry for a specific period of time (tbd).
$\overline{\text{PORST}}$	Y21	I	**Power-on Reset Input** A low level on $\overline{\text{PORST}}$ causes an asynchronous reset of the entire chip. During power-up of the TC1775, this pin must be held active (low). Otherwise the life time of the flash memory may be reduced.
CLKIN	T1	I	**EBU Clock Input** CLKIN must be connected externally with CLKOUT. For fine-tuning of the external bus interface timing, this external connection can be an external delay circuit.
CLKOUT	R1	O	**Clock Output**
TEST MODE	AB23	I	**Test Mode Select Input**
XTAL1 **XTAL2**	AC23 AC22	I O	**Oscillator/PLL/Clock Generator Input/Output Pins** XTAL1 is the input to the oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the oscillator amplifier circuit. For clocking the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
XTAL3 **XTAL4**	AB21 AA20	I O	**Real Time Clock Oscillator Input/Output**

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
V_{DDOSC}	AC21	-	**Main Oscillator Power Supply (2.5V)** 1)
V_{SSOSC}	AA21	-	**Main Oscillator ground**
V_{DDPLL}	AA22	-	**PLL Power Supply (2.5V)** 1)
V_{SSPLL}	AA23	-	**PLL Ground**
V_{DDP1}	K3	-	**Port 1 Power Supply (2.5V)** 2)
V_{DDP5}	AC17	-	**Port 5 and OCDS/JTAG Pins Power Supply (2.5V)** 2)
$V_{DDP0234}$	H4 M4 T4 Y8 Y12	-	**Ports 0,2,3,4 and Dedicated Pins Power Supply (2.5V)** 2)
V_{DDP813}	D8 D12 D16 H20 M20 T20 Y16	-	**Port 8-13 Power Supply (3 - 5V)** 2)
		-	**Port Logic/Schmitt Trigger Power Supply** 2) 3)
$V_{DDPS0234}$	AC3		for Port 0,2,3, and 4 (2.5V)
V_{DDPS1}	L4		for Port 1 (2.5V)
V_{DDPS5}	AB18		for Port 5 and OCDS/JTAG control lines (2.5V)
$V_{DDPS813}$	D21		for Port 8-13 and dedicated pins (3 - 5V)
V_{DDRAM}	C14	-	**SRAM (DMU-, PMU-, PCP-SRAM) Power Supply (2.5V)**
V_{DDSB}	B14	-	**Stand-by Power Supply (2.5V)** 1)

1)2) The voltage on power supply pins marked with 2) has to be raised earlier or at least at the same time (= time window of 1µs) than on power supply pins marked with 1).

3) V_{DDPSx} of a port group x must be always at the same voltage level as V_{DDPx}. Therefore, V_{DDPSx} of port group x should be always connected together with V_{DDPx} to one power supply. (x="0234", "1", "5", or "813")

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
V_{DD}	K4,P4 V4,D6 Y10 D14 Y18 F20 K20 P20	-	**Power Supply (2.5V)** 1) for core and internal logic.
V_{SS}	F4, Y6, V20, D18, K10 to K14, L10 to L14, M10 to M14, N10 to N14, P10 to P14	-	**Ground** used for core, internal logic, peripherals, and ports.

1) 2) The voltage on power supply pins marked with 2) has to be raised earlier or at least at the same time (= time window of 1µs) than on power supply pins marked with 1).

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
V_{DDSC}	A1	-	**ADC Short Circuit/Broken Wire Logic Power Supply (5V)**
V_{SSSC}	A2	-	**ADC Short Circuit/Broken Wire Logic Ground**
V_{DDM}	C3	-	**ADC Digital Part Power Supply (5V)**
V_{SSM}	A3	-	**ADC Digital Part Ground**
V_{DDA0}	D9	-	**ADC0 Port and Analog Part Power Supply** (2.5V)
V_{SSA0}	A9	-	**ADC0 Port and Analog Part Ground**
V_{DDA1}	H1	-	**ADC1 Port and Analog Part Power Supply** (2.5V)
V_{SSA1}	G3	-	**ADC1 Port and Analog Part Ground**
V_{AREF0}	C8	-	**ADC0 Reference Voltage** 2)
V_{AGND0}	B8	-	**ADC0 Reference Ground**
V_{AREF1}	G2	-	**ADC1 Reference Voltage** 2)
V_{AGND1}	G4	-	**ADC1 Reference Ground**
N.C.	D10 Y14 AB15 AB22	-	**Not Connected** These pins should be not connected.

1) 2) The voltage on power supply pins marked with 2) has to be raised earlier or at least at the same time (= time window of 1µs) than on power supply pins marked with 1).

Block Diagram

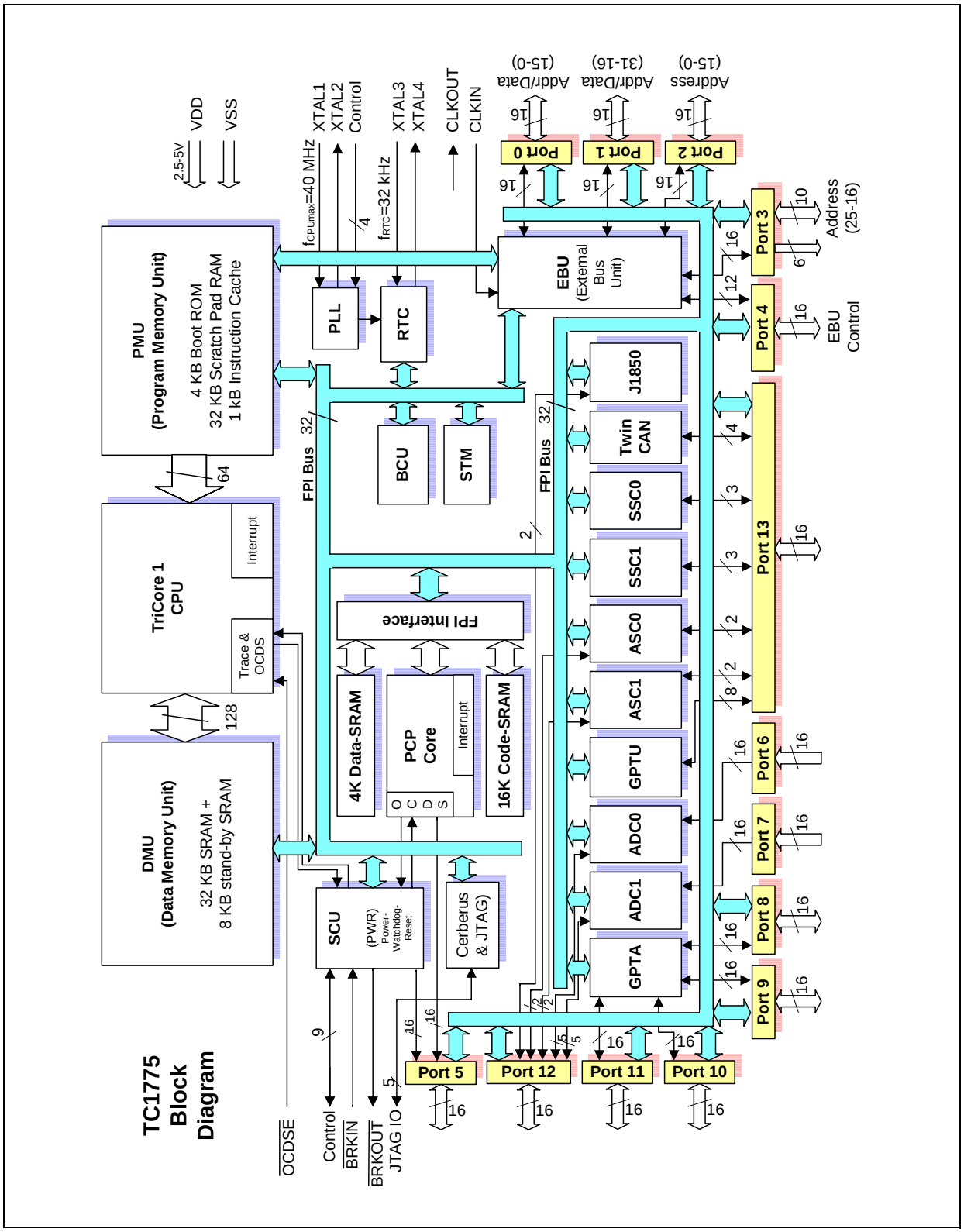


Figure 3 TC1775 Block Diagram

Advance Information

Serial Interfaces

The TC1775 includes six serial peripheral interface units:

- two Asynchronous/Synchronous Serial Interfaces (ASC0 and ASC1)
- two High-Speed Synchronous Serial Interfaces (SSC0 and SSC1)
- one TwinCAN interface
- one J1850 Serial Data Link Interface (SDLM)

Asynchronous/Synchronous Serial Interfaces

Figure 4 shows a global view of the functional blocks of the two ASC interfaces.

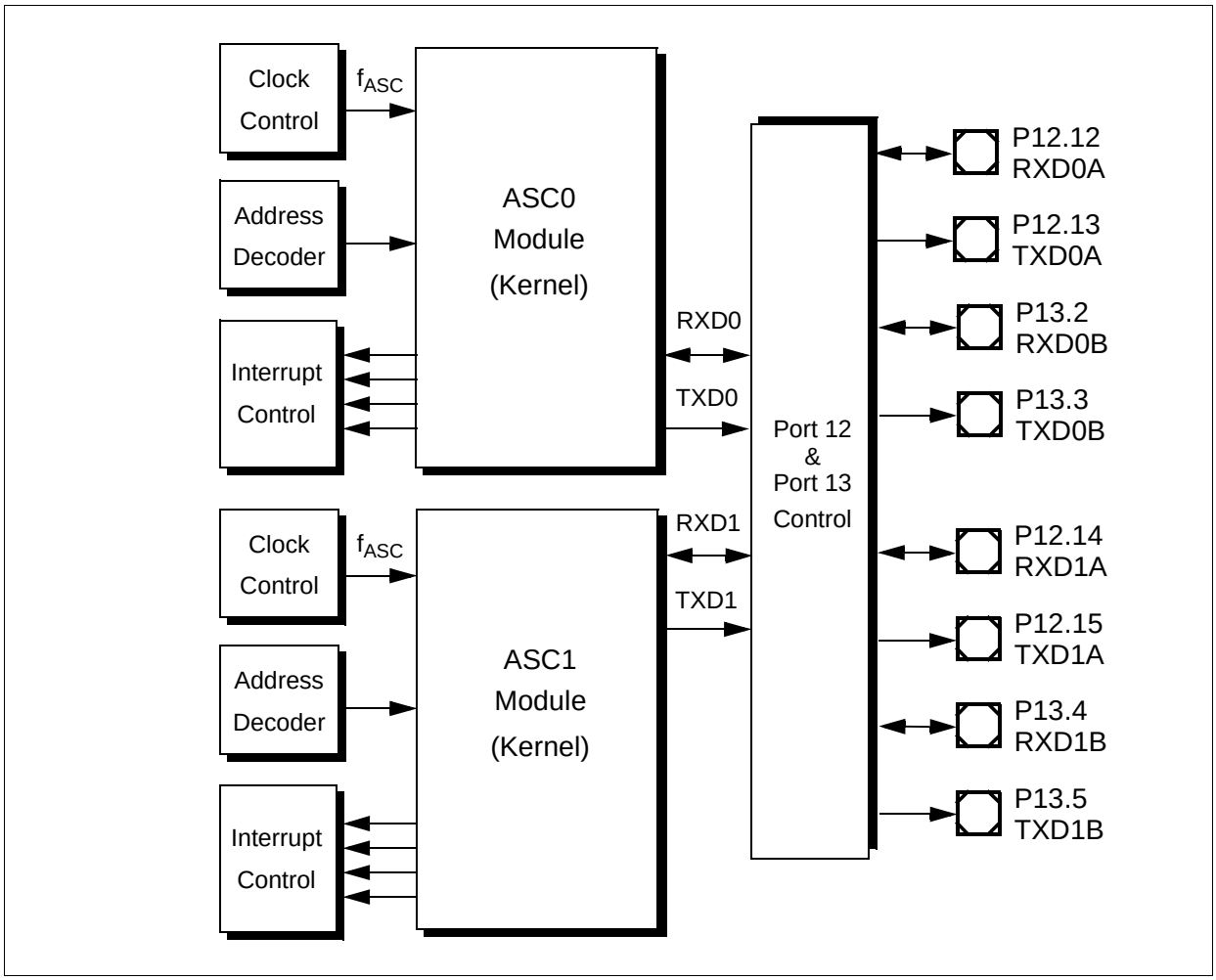


Figure 4 General Block Diagram of the ASC Interfaces

Each ASC module, ASC0 and ASC1, communicate with the external world via two pairs of two I/O lines each. The RXD line is the receive data input signal (in synchronous mode also output), and TXD is the transmit output signal. Clock control, address decoding, interrupt service request control, and port control is managed outside the ASC module kernel.

Advance Information

The Asynchronous/Synchronous Serial Interfaces provide serial communication between the TC1775 and other microcontrollers, microprocessors or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In synchronous mode, data are transmitted or received synchronous to a shift clock which is generated by the ASC internally. In asynchronous mode, 8- or 9-bit data transfer, parity generation and the number of stop bits can be selected. Parity, framing and overrun error detection is provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism to distinguish address from data bytes is included. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be very accurately adjusted by a prescaler implemented as fractional divider.

Features

- Full duplex asynchronous operating modes
  - 8- or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baudrate from 2.5 MBaud to 0.6 Baud (@ 40 MHz clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baudrate from 5 MBaud to 406.9 Baud (@ 40 MHz clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - on a transmitter buffer empty condition
  - on a transmit last bit of a frame condition
  - on a receiver buffer full condition
  - on an error condition (frame, parity, overrun error)
- Two pin pairs RXD/TXD for each ASC available at port 12 or port 13

High-Speed Synchronous Serial Interfaces

Figure 5 shows a global view of the functional blocks of the two SSC interfaces.

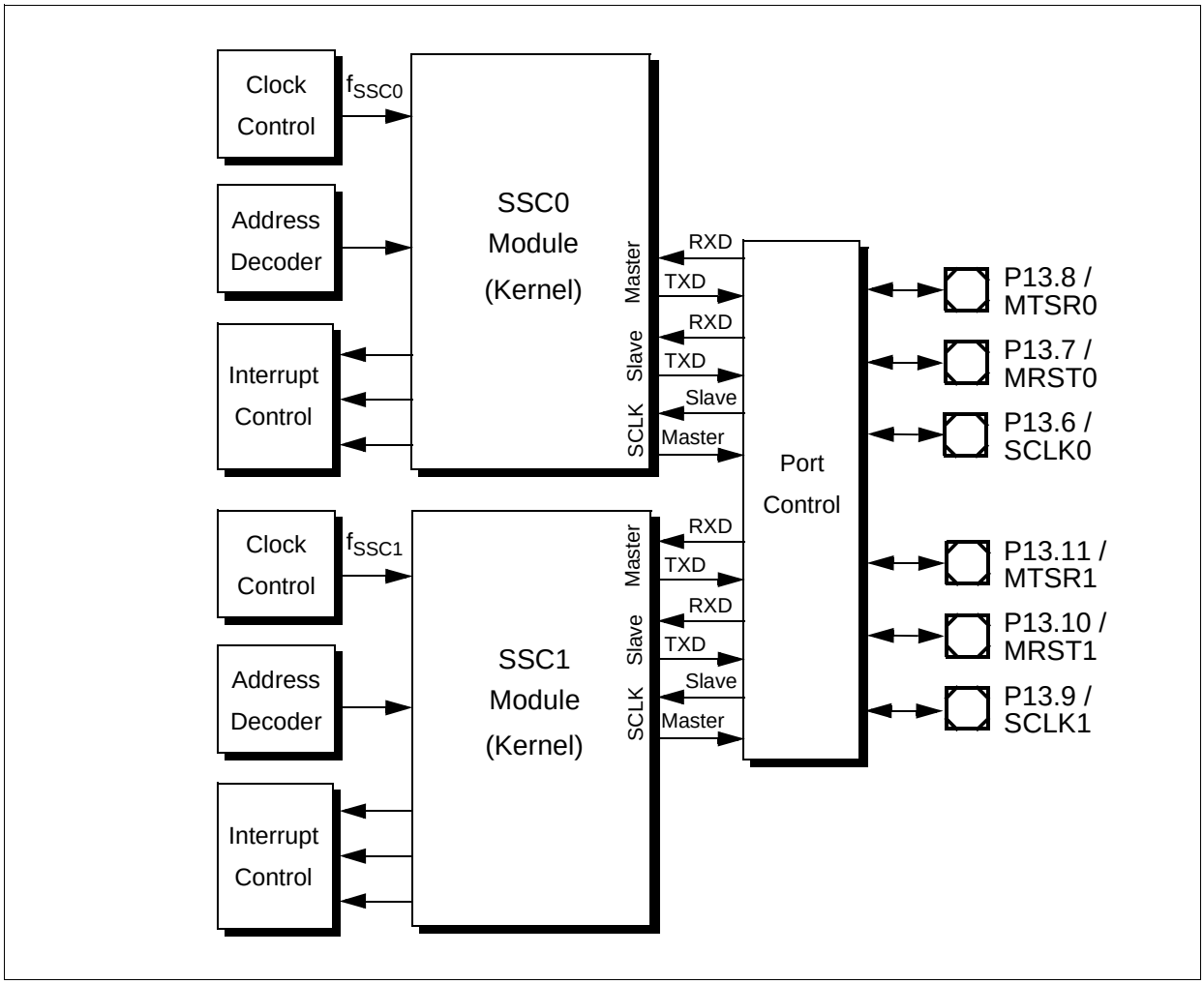


Figure 5 General Block Diagram of the SSC Interfaces

Each of the SSC module has three IO lines which are located at Port 13. Each of the SSC modules is further supplied by a separate clock control, interrupt control, address decoding and port control logic.

The SSC supports full-duplex and half-duplex serial synchronous communication up to 20 MBaud (@ 40 MHz module clock). The serial clock signal can be generated by the SSC itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A 16-bit baud rate generator provides the SSC with a separate serial clock signal.

Advance Information

Features

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Flexible data format
  - Programmable number of data bits: 2 to 16 bit
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baudrate generation from 20 MBaud to 305.18 Baud (@ 40 MHz module clock)
- Interrupt generation
  - on a transmitter empty condition
  - on a receiver full condition
  - on an error condition (receive, phase, baudrate, transmit error)
- Three pin interface
  - Flexible SSC pin configuration

Advance Information

TwinCAN Interface

Figure 6 shows a global view of the functional blocks of the TwinCAN module.

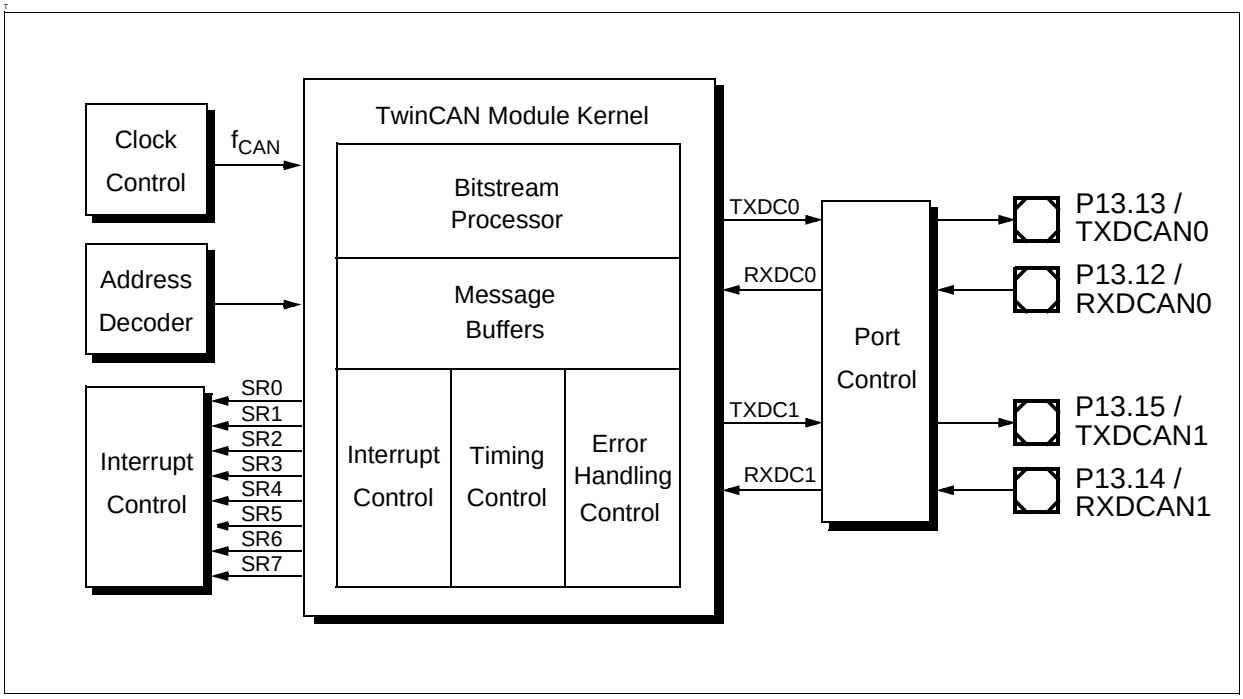


Figure 6 General Block Diagram of the TwinCAN Interfaces

The TwinCAN module has four IO lines which are located at Port 13. The TwinCAN module is further supplied by a clock control, interrupt control, address decoding and port control logic.

The TwinCAN module combines two Full-CAN interfaces in one module, which either operate independently or share the TwinCAN module's resources. Transmission and reception of CAN frames is handled autonomously in accordance to CAN specification V2.0 part B (active). Each of the two Full-CAN interfaces can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share the TwinCAN module's resources in order to optimize the CAN bus traffic handling as well as to minimize the CPU load. The flexible combination of Full-CAN functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the increased number of message objects permit precise and comfortable CAN bus traffic handling.

Depending on the application, each of the 32 message objects can be individually assigned to one of the two CAN nodes. Gateway functionality allows automatic data exchange between two separated CAN bus systems, which decreases CPU load and improves the real time behavior of the entire system.

Advance Information

The bit timing for both CAN interfaces is derived from the peripheral clock and is programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins interface each of the CAN interfaces to a bus transceiver.

Features

- Full CAN functionality which complies with CAN specification V2.0 B active
- Handling of frames with 11-bit and 29-bit identifiers
- Dedicated control register for each channel
- Up to 1MBaud data transfer rate
- Flexible and powerful message transfer control and error handling capability
- Power Saving Mode (idle and auto-idle)
- 32 independent message objects individually assignable to one of the two CAN nodes
- Message objects: double, quad, eight times, 16 times, and 32 times buffered (FIFO structure)
- Receive object and transmit object buffering
- Acceptance filtering by message object specific and individually programmable masks
- Frame Number information for all messages available
- Up to eight individually programmable interrupt outputs
- CAN Analyzer Mode for bus monitoring
- Listen Mode individual programmable for message objects
- ’Gateway“ functionality supported to interconnect two CAN bus systems

Advance Information

Serial Data Link Interface

Figure 7 shows a global view of the functional blocks of the SDLM interface.

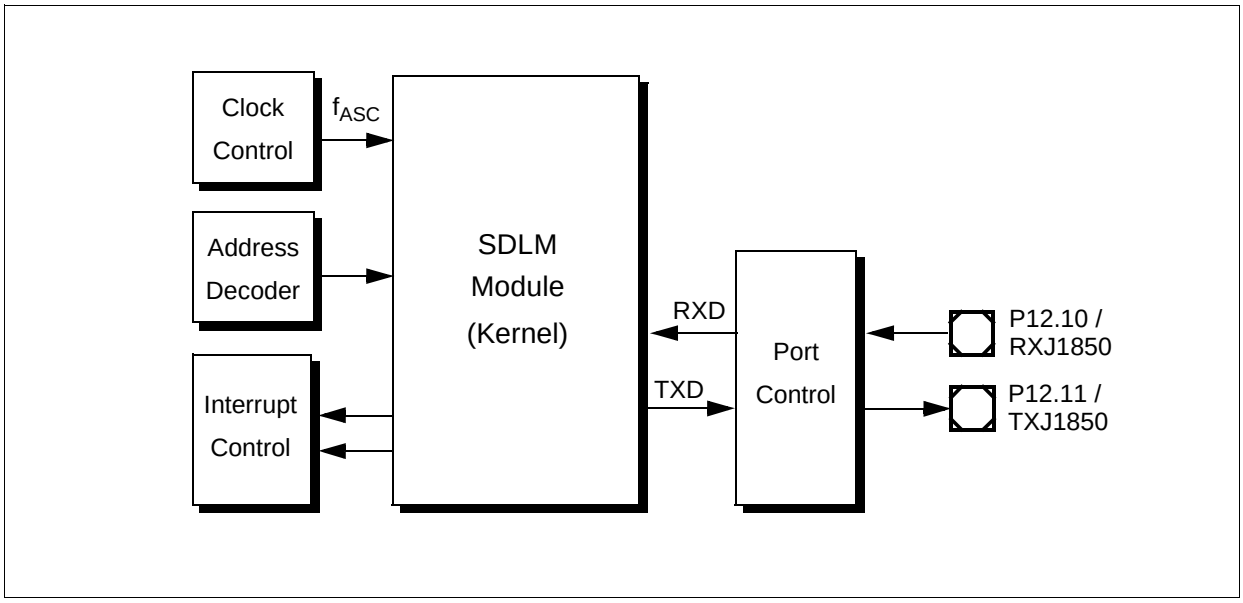


Figure 7 General Block Diagram of the SDLM Interface

The SDLM module communicates with the external world via two I/O lines located at port 12, the J1850 bus. The RXD line is the receive data input signal and TXD is the transmit data output signal.

The Serial Data Link Module provides serial communication to a J1850 based serial bus. J1850 bus transceivers have to be implemented externally in a system. The SDLM module is conform to the SAE Class B J1850 specification and compatible to class 2 protocol.

General SDLM Features

- Compliant to SAE Class B J1850 specification
- Full support of GM class 2 protocol
- Variable Pulse Width (VPW) format with 10.4 kBaud
- High speed receive/transmit 4x mode with 41.6 kBaud
- Digital noise filter
- Power save mode and automatic wake-up upon bus activity
- Support of single byte headers or consolidated headers
- CRC generation & check
- Support of block mode for receive and transmit

Advance Information

Data Link Operation Features

- 11 bytes transmit buffer
- Double buffered 11 bytes receive buffer
- Support of In-frame response (IFR) types 1,2,3
- Advanced interrupt handling for RX, TX and error conditions
- All interrupt sources can be enabled/disabled individually
- Support of automatic IFR Transmission for IFR types 1,2 for three byte consolidated headers

Advance Information

Timer Units

The TC1775 includes two timer units:

– the General Purpose Timer Array GPTA
– the General Purpose Timer Unit GPTU

General Purpose Timer Array

Figure 8 shows a global block diagram of the GPTA implementation.

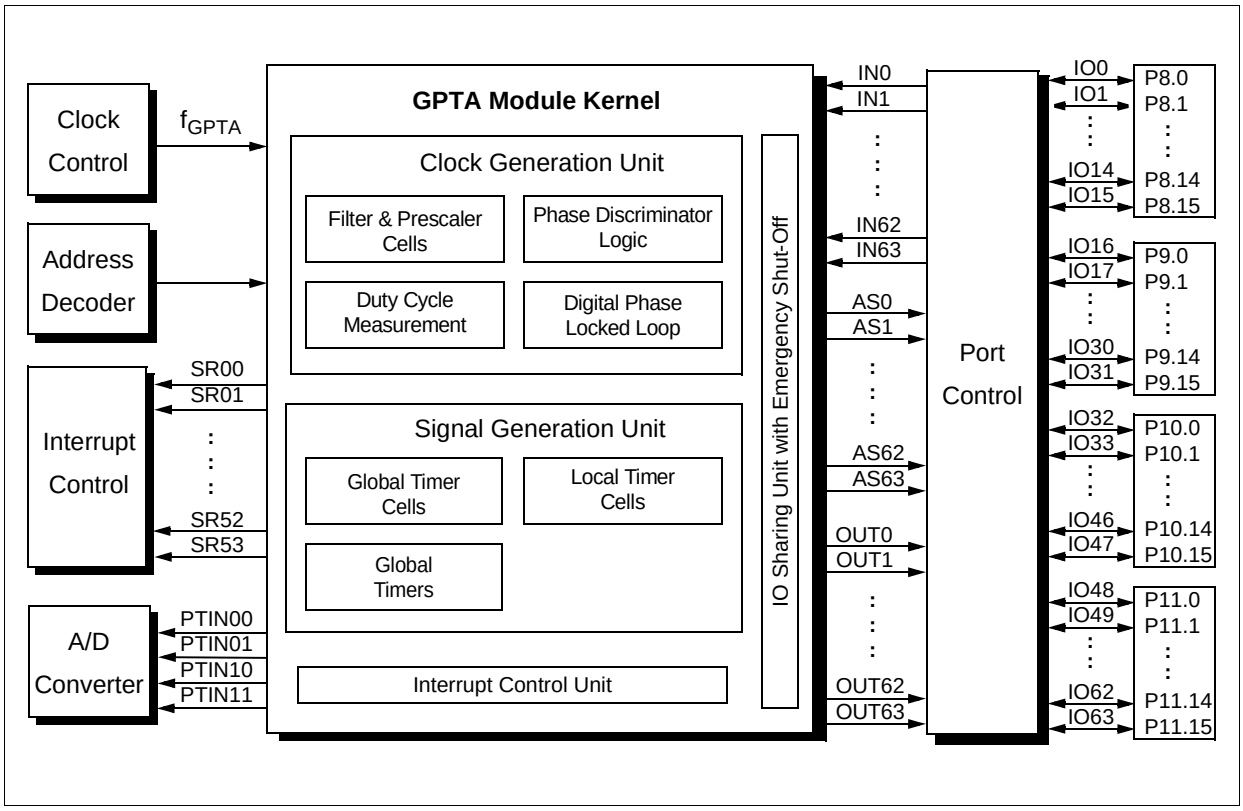


Figure 8 GPTA Module Block Diagram

The GPTA module has 64 input lines and 64 output lines which are connected with port 8, port 9, port 10, and port 11.

The general purpose timer array (GPTA) provides an important set of digital signal filtering and timer support, the combination of them makes autonomous and complex functionalities. This architecture allows an easy implementation, and easy validation of any kind of timer functions.

Advance Information

The General Purpose Timer Array (GPTA) provides a set of hardware modules required for high speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as time base for the associated "Global Timer Cells".
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an event occurred at an external port pin or at an internal FPC cell output. A GTC may be also used to control an external port pin with the result of an internal compare operation. GTC cells can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in timer, capture or compare mode may be also logically tied together driving a common external port pin with a complex signal waveform. LTC cells, enabled in timer or capture mode, can be clocked or triggered by
  - a prescaled GPTA module clock,
  - an FPC, PDL, DCM, PLL or GTC output signal line,
  - an external port pin.

Some input lines driven by processor I/O pads may be shared by an LTC and a GTC cell to trigger their programmed operation simultaneously.

The following list summarizes the features of the GPTA functional units:

Clock Generation Unit:

- Filter and Prescaler Cell (FPC)
  - 6 independent units
  - 3 operating modes
    (Prescaler, Delayed Debounce Filter, Immediate Debounce Filter)
  - f_{GPTA} down-scaling capability
  - $f_{GPTA}/2$ maximum input signal frequency in Filter Mode

- Phase Discriminator Logic (PDL)
  - 2 independent units.
  - 2 operating modes (2 and 3 sensor signals).
  - $f_{GPTA}/4$ maximum input signal frequency in 2 sensor mode,
    $f_{GPTA}/6$ maximum input signal frequency in 3 sensor mode

Advance Information

- Duty Cycle Measurement (DCM)
  - 4 independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

- Digital Phase Locked Loop (PLL)
  - 1 unit
  - arbitrary multiplication factor between 1 - 65.535
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

Signal Generation Unit:

- Global Timers (GT)
  - 2 independent units
  - 2 operating modes (Free Running Timer and Reload Timer)
  - 24 bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

- Global Timer Cell (GTC)
  - 32 independent units
  - 3 operating modes (capture, compare, and capture after compare)
  - 24 bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

- Local Timer Cell (LTC)
  - 64 independent units
  - 3 operating modes (Timer, Capture and Compare)
  - 16 bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

Interrupt Control Unit

- 111 interrupt sources generating 54 service requests

I/O Sharing Unit

- Able to process lines from FPC, GTC and LTC
- Emergency function

General Purpose Timer Unit

Figure 9 shows a global view of all functional blocks of the GPTU module.

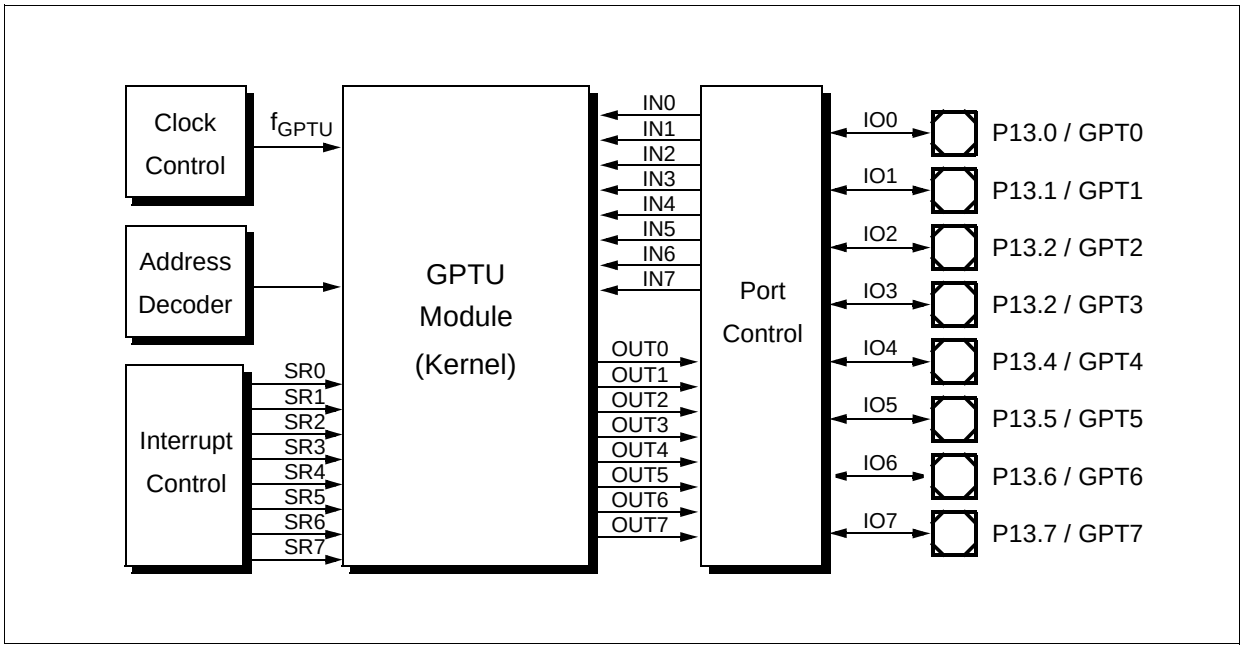


Figure 9 General Block Diagram of the GPTU Interface

The GPTU consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. The GPTU communicates with the external world via eight inputs and eight outputs which are located at Port 13.

The three timers of the GPTU module T0, T1, and T2 can operate independently from each other, or can be combined.

General Features

- All timers are 32-bit precision timers with a maximum input frequency of $f_{GPTU}/2$.
- Events generated in T0 or T1 can be used to trigger actions in T2
- Timer overflow or underflow in T2 can be used to clock either T0 or T1
- T0 and T1 can be concatenated to form one 64-bit timer

Features of T0 and T1

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers
- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Two input pins can determine a count option

Advance Information

Features of T2

- Optionally count up or down
- Operating modes:
  - Timer
  - Counter
  - Quadrature counter
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions.
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins
- T2 events are freely assignable to the service request nodes.

Advance Information

Analog Digital Converters

The two on-chip ADC modules of the TC1775 are analog to digital converters with 8-bit, 10-bit or 12-bit resolution including sample & hold functionality. The A/D converters operate by the method of the successive approximation. A multiplexer selects between up to 16 analog input channels for each ADC. Conversion requests are generated either under software control or by hardware. An automatic self-calibration adjusts the ADC modules to changing temperatures or process variations.

Features

The following functionality has been implemented in the two on chip ADC modules to fulfill the enhanced requirements of embedded control applications:

- 8-bit, 10-bit, 12-bit A/D Conversion
- Successive approximation with conversion time t_c (inc. sample time) of 5µs @ 10-bit resolution
- Total Unadjusted Error (TUE) of $\pm$ 2 LSB @ 10-bit resolution
- Integrated sample and hold functionality
- 16 analog input channels
- Dedicated control and status registers for each analog channel
- Flexible conversion request mechanisms
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Broken wire - short circuit detection
- Flexible ADC module service request control unit
- Synchronization of the two on-chip A/D Converters
- Automatic control of external analog multiplexer
- Equidistant samples initiated by timer
- External trigger inputs for conversion requests
- Two external trigger inputs, connected with the General Purpose Timer Array (GPTA)
- Power reduction and clock control feature

Figure 10 shows a global view of the ADC module kernel with the module specific interface connections.

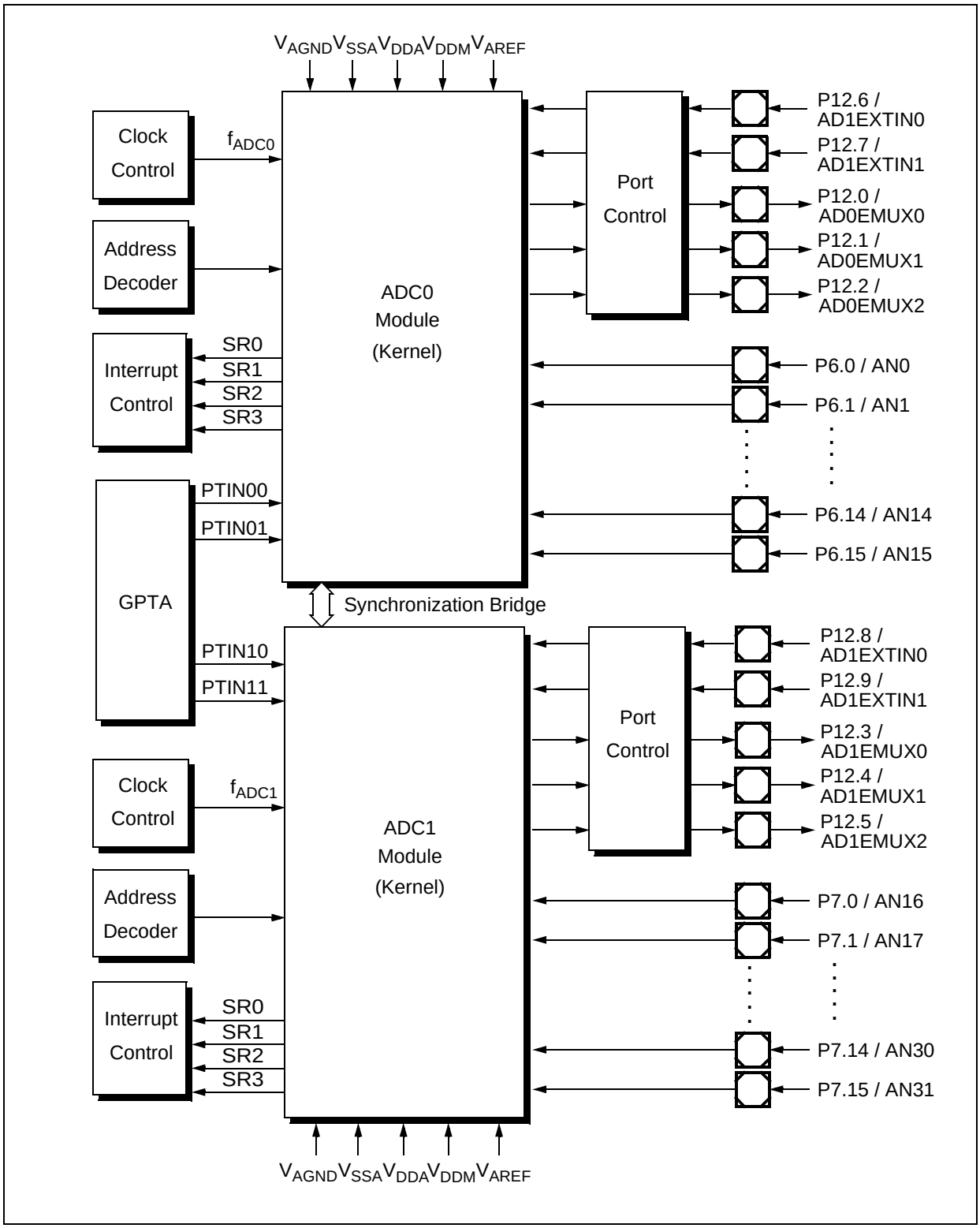


Figure 10 ADC0/ADC1 Modules with Interconnections

Advance Information

On-Chip Memories

The TC1775 provides the following on-chip memories:

- Program Memory Unit (PMU) with
  - 4 KB Boot ROM
  - 32 KB Code Scratchpad RAM (SPRAM)
  - 1 KByte Instruction Cache (ICache)
- Data Memory Unit (DMU) with
  - 40 KB Data Memory (SRAM)
  - includes 8 KB static RAM (SBRAM) for standby operation using a battery
- Peripheral Control Processor (PCP) with
  - 16 KB Data Memory (PCODE)
  - 4 KB Parameter RAM (PRAM)

On-Chip FPI-Bus

The FPI-Bus interconnects the functional units of the TC1775 such as the CPU and on-chip peripheral components. Via the External Bus Controller (EBU), it also interconnects the TC1775 to external components. The FPI-Bus is designed to be quick to acquire by on-chip functional units, and quick to transfer data. The low setup overhead of the FPI-Bus access protocol guarantees fast FPI-Bus acquisition, which is required for time-critical applications. The FPI-Bus is designed to sustain high transfer rates. With the TC1775, on the internal FPI-Bus a peak transfer rate of up to 160 Mbytes/s can be achieved. Multiple data transfers per bus-arbitration cycle allow the FPI-Bus to operate at close to its peak bandwidth.

Features

- Supports multiple bus masters (PCP, DMU, PMU, EBU, OCDS)
- Supports demultiplexed address/data operation
- Address and data buses are 32 bits wide
- Data transfer types include 8-, 16-, and 32-bit sizes
- Single- and multiple-data transfers per bus acquisition cycle
- Designed to minimize EMI and power consumption
- Controlled by an FPI-Bus Control Unit (BCU)
  - arbitration of FPI-Bus master requests
  - handling of bus errors

External Bus Unit

The External Bus Unit (EBU) of the TC1775 is the interface between external memories or peripheral units and the internal memories and peripheral units. **Figure 11** shows the basic structure of the EBU.

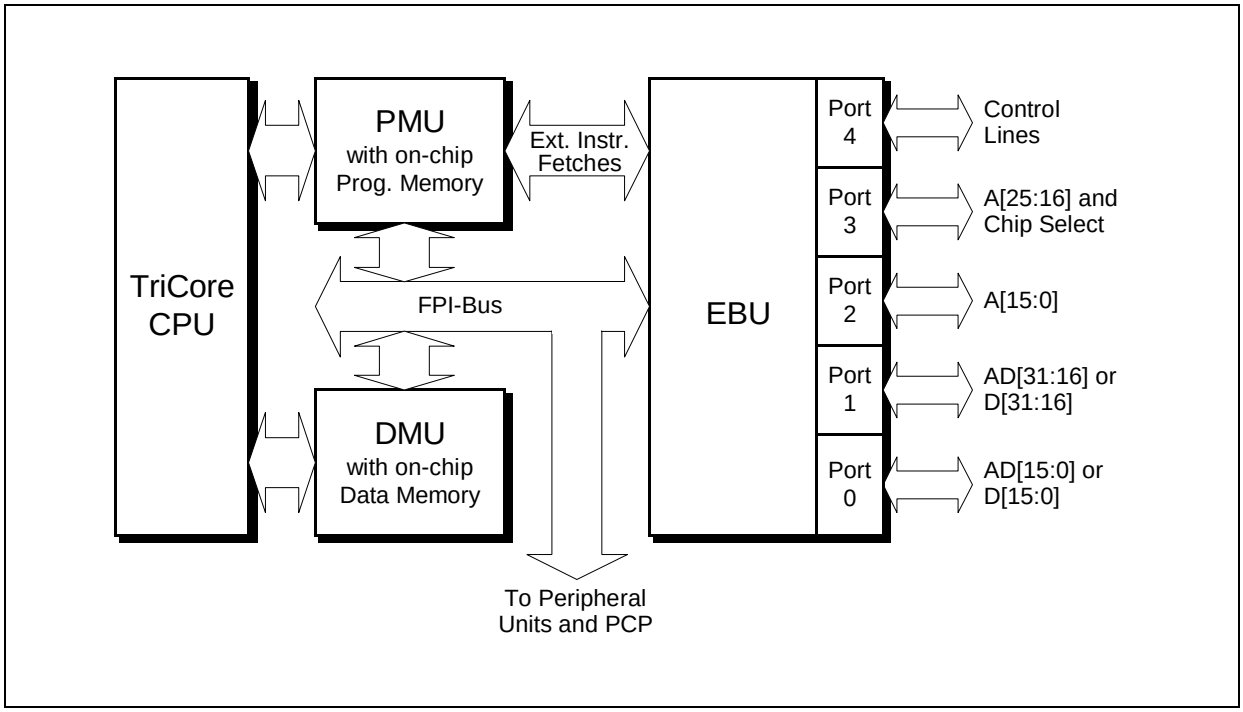


Figure 11 EBU Structure and Interfaces

The EBU is mainly used for the following two operations:

- Communication via the FPI-Bus with external memories or peripheral units
- Instruction fetches from the PMU to external Burst Flash program memories

The EBU controls all transactions required for these two operations and especially handles the arbitration between these two tasks.

The types of external devices/bus modes controlled by the EBU are:

- INTEL style peripherals (separate $\overline{RD}$ and $\overline{WR}$ signals)
- ROMs, EPROMs
- Static RAMs
- Burst Mode Flash Memories (AMD/INTEL)
- demultiplexed address and data bus
- multiplexed address/data bus

Advance Information

Peripheral Control Processor

The Peripheral Control Processor (PCP) performs tasks that would normally be performed by the combination of a DMA controller and its supporting CPU interrupt service routines in a traditional computer system. It could easily be considered as the host processor's first line of defense as an interrupt-handling engine. The PCP can off-load the CPU from having to service time-critical interrupts. This provides many benefits, including:

- Avoiding large interrupt-driven task context-switching latencies in the host processor
- Lessening the cost of interrupts in terms of processor register and memory overhead
- Improving the responsiveness of interrupt service routines to data-capture and data-transfer operations
- Easing the implementation of multitasking operating systems.

The PCP has an architecture which efficiently supports DMA type transactions to and from arbitrary devices and memory addresses within the TC1775 and also has reasonable stand alone computational capabilities.

The PCP is made up of several modular blocks as follows:

- PCP Processor Core
  - 16-bit Program Counter
- 16 KByte Code Memory (PCODE)
  - holds the channel programs, consisting of PCP instructions
- 4 KByte Parameter Memory (PRAM)
  - holds the Channel Program's context
  - used for general data storage
  - communication area for the CPU and other FPI-Bus masters
- PCP Interrupt Control Unit (PICU)
  - determines the request with the currently highest priority and routes the request together with its priority number to the PCP processor core. It also acknowledges the requesting source when the PCP starts the service of this interrupt.
- PCP Service Request Nodes (PSRN)
  - generation of service requests to the CPU
- System bus interface to the Flexible Peripheral Interface (FPI) Bus
  - access capability of all peripheral units on the FPI-Bus
  - FPI-Bus master can access code and PRAM memory and the PCP control and status registers

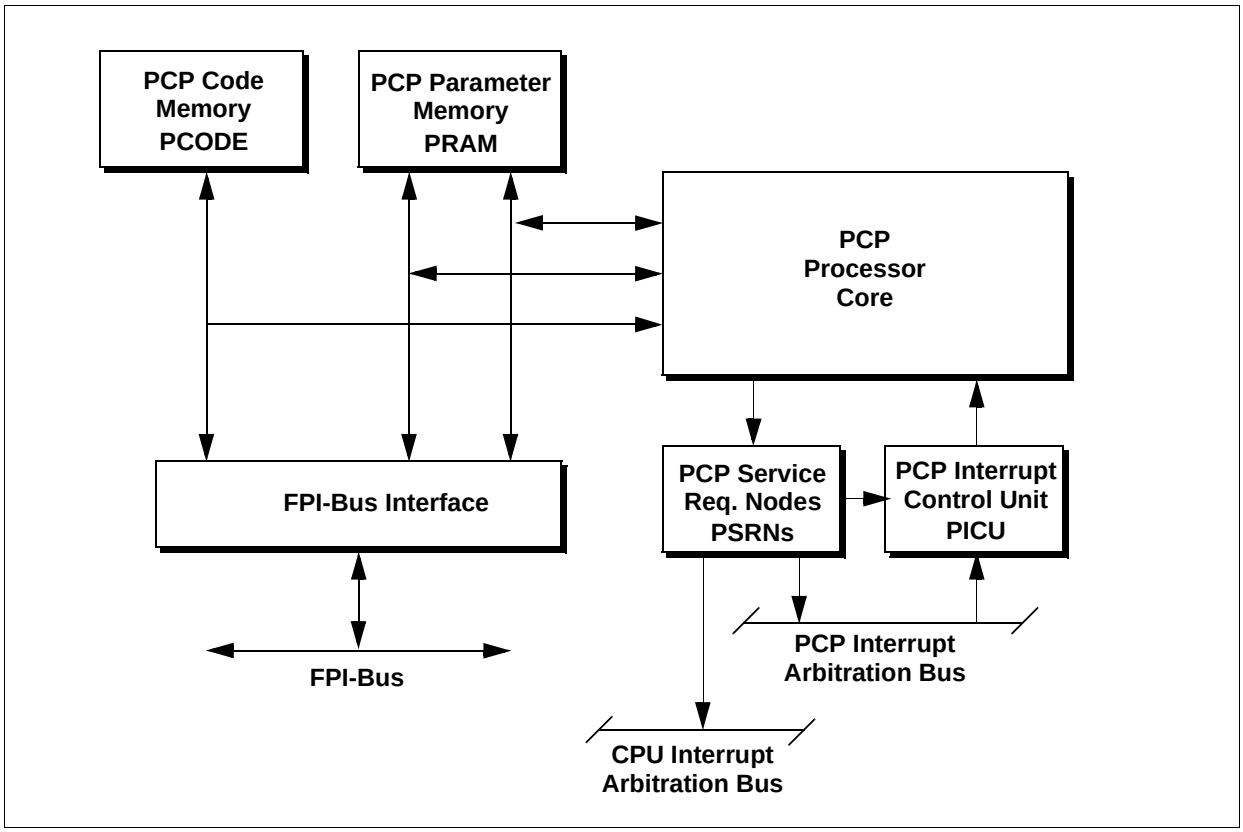


Figure 12 PCP Block Diagram

The PCP is fully interrupt-driven, meaning it is only activated through service requests; there is no main program running in the background as with a conventional processor.

Table 2 PCP Instruction Set Overview

Instruction Group	Description
DMA primitives	Efficient DMA channel implementation
Load/Store	Transfer data between PRAM or FPI memory and the general purpose registers, as well as move or exchange values between registers
Arithmetic	Add, subtract, compare and complement
Divide/Multiply	Divide and multiply
Logical	And, Or, Exclusive Or, Negate
Shift	Shift right or left, rotate right or left, prioritize
Bit Manipulation	Set, clear, insert and test bits
Flow Control	jump conditionally, jump long, exit
Miscellaneous	No operation, Debug

Advance Information

System Timer

The STM within the TC1775 is designed for global system timing applications requiring both high precision and long range. The STM provides the following features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Driven by clock, f_{STM} (identical with the system clock f_{SYSCLK}).
- Counting begins at power-on reset
- Continuous operation is not affected by any reset condition except power-on reset

The System Timer can be read in sections from seven registers, TIM0 through TIM6, which select increasingly higher-order 32-bit ranges of the System Timer. These can be viewed as individual 32-bit timers, each with a different resolution and timing range. Another register, CAP, is implemented to latch the contents of the STM high part each time when the STM low part, TIM0, is read.

The maximum clock period is $2^{56} * f_{STM}$. At f_{STM} = 40 MHz, for example, the STM counts 58.6 years before overflowing. Thus, it is capable of continuously timing the entire expected product life-time of a system without overflow.

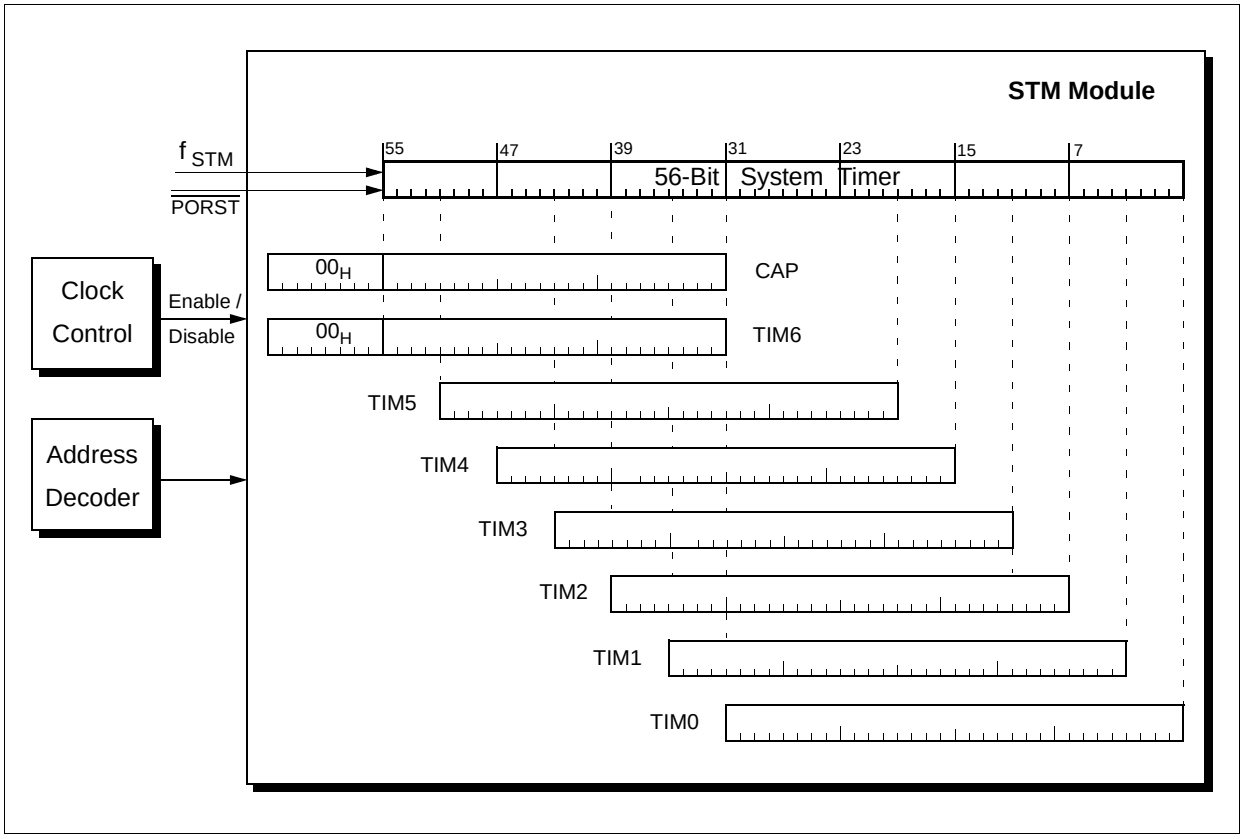


Figure 13 Block Diagram of the STM Module

Advance Information

Watchdog Timer

The Watchdog Timer provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps prevent the TC1775 from seriously malfunctioning for more than a user-specified time period. When enabled, the Watchdog Timer (WDT) will cause the TC1775 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1775 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard 'watchdog' function, the WDT incorporates the EndInit feature and monitors its modifications. A system-wide line is connected to the ENDINIT bit implemented in a WDT control register, serving as an additional write-protection for critical registers (besides Supervisor Mode protection).

A further enhancement in the TC1775's Watchdog Timer is its reset prewarning operation. Instead of immediately resetting the device on the detection of an error, as known from standard watchdogs, the WDT first issues a NMI to the CPU before finally resetting the device a certain time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, an important aid in debugging.

Features

- 16-bit watchdog counter.
- selectable input frequency: f_{SYSCLK}/256 or f_{SYSCLK}/16384.
- 16-bit user-definable reload value for normal watchdog operation, fixed reload value for Time-Out and Prewarning Modes.
- Incorporation of the ENDINIT bit and monitoring of its modifications.
- Sophisticated password access mechanism with fixed and user-definable password fields.
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT and limited.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the watchdog reset generation.
- Overflow Error Detection:
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a watchdog induced reset occurs twice without a proper access to its control register in between, a severe system malfunction is assumed and the TC1775 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.
- Important debugging support through the reset prewarning operation by first issuing a NMI to the CPU before finally resetting the device after a certain period of time.

Advance Information

Real Time Clock

Figure 14 shows a global view of all functional blocks oft he RTC interface.

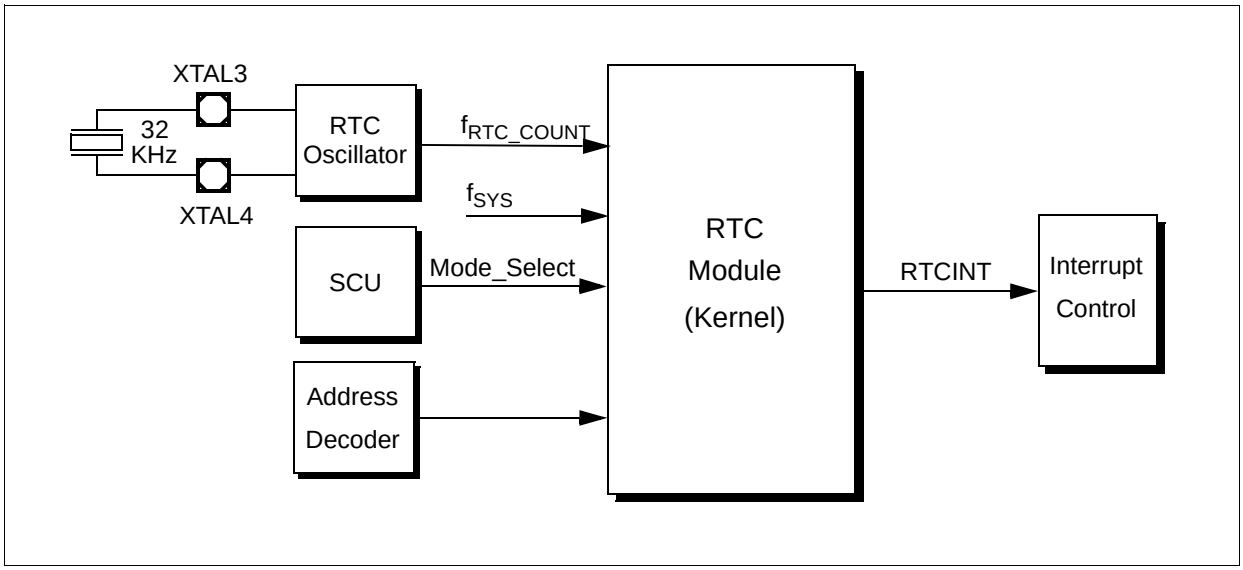


Figure 14 Block Diagram of the RTC Interface

The Real Time Clock (RTC) module basically is an independent timer chain which counts time ticks. The base frequency of the RTC can be programmed via a reload counter. The RTC can work fully asynchronous to the system frequency and is optimized on low power consumption.

Features

- 32.768 KHz clock for counting current time and date
- Cyclic time based interrupts
- Alarm interrupt for wake-up on a defined time
- 48-bit timer for long term measurements

Advance Information

Power Management System

The TC1775 power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application.

There are four power management modes:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Table 3 describes these features of the power management modes.

Table 3 Power Management Modes of the TC1775

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the NMI pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock continues to be distributed only to those peripherals programmed to operate in Sleep Mode. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the NMI pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.
Deep Sleep	The system clock is shut off, and only an external signal will restart the system. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.

Advance Information

On-Chip Debug Support

The On-Chip Debug Support of the TC1775 consists of four building blocks:

- OCDS module in the TriCore CPU
  - On-chip breakpoint hardware
  - Support of an external break signal
- OCDS module in the PCP
  - special DEBUG instruction for program execution tracing
- Trace module of the TriCore
  - outputs 16 bits per cycle with pipeline status information, PC bus information, and breakpoint qualification information
- Debugger Interface (Cerberus)
  - provided for debug purposes of emulation tool vendors
  - accessible through a JTAG standard interface with dedicated JTAG port pins

Figure 15 shows a basic block diagram of the building blocks.

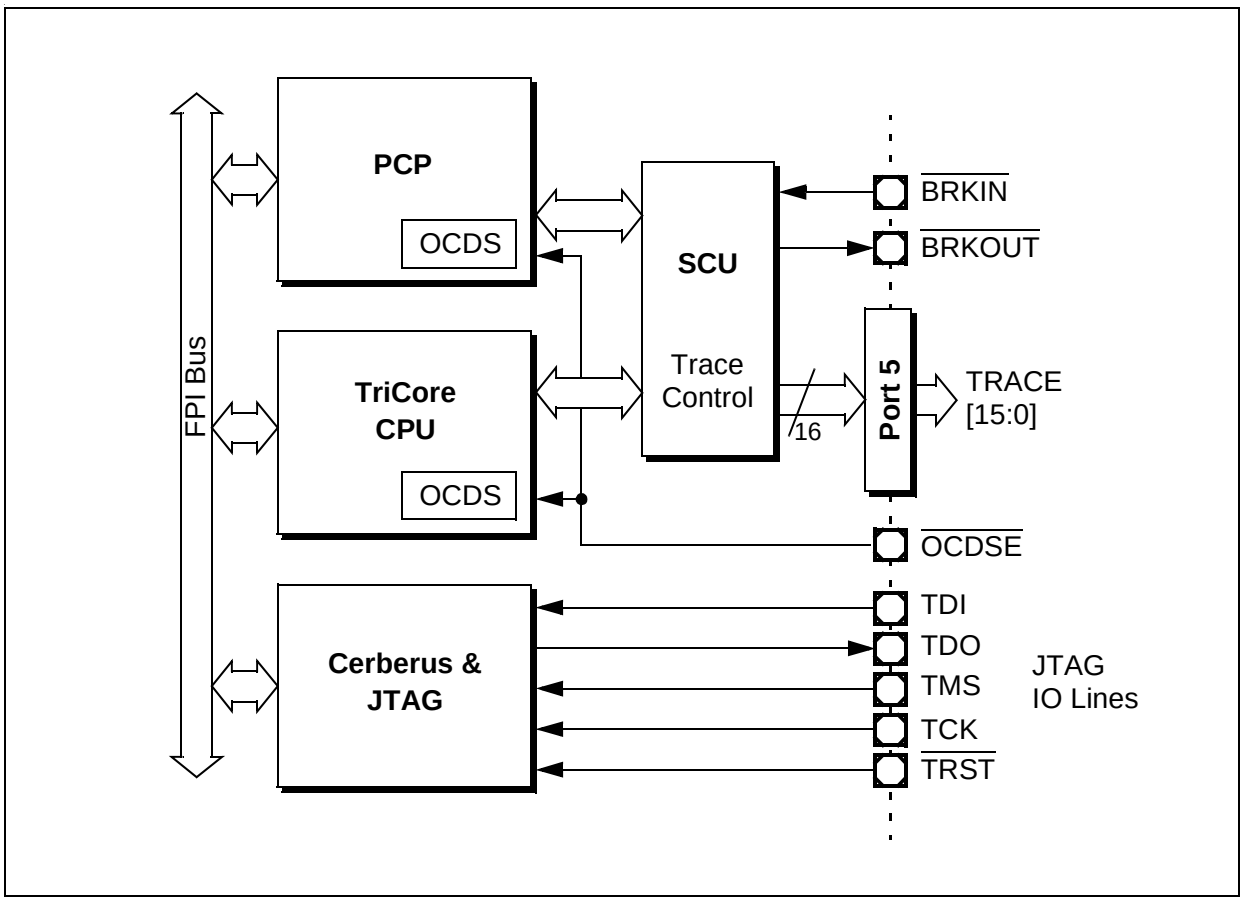


Figure 15 OCDS Support Basic Block Diagram

Advance Information

Clock Generation Unit

The Clock Generation Unit in the TC1775, shown in **Figure 16**, consists of an oscillator circuit and a Phase-Locked Loop (PLL). The PLL can convert a low-frequency external clock signal to a high-speed internal clock for maximum performance. The PLL also has fail-safe logic that detects degenerate external clock behavior such as abnormal frequency deviations or a total loss of the external clock. It can execute emergency actions if it looses its lock on the external clock.

In general, the Clock Generation Unit (CGU) is controlled through the System Control Unit (SCU) module of the TC1775.

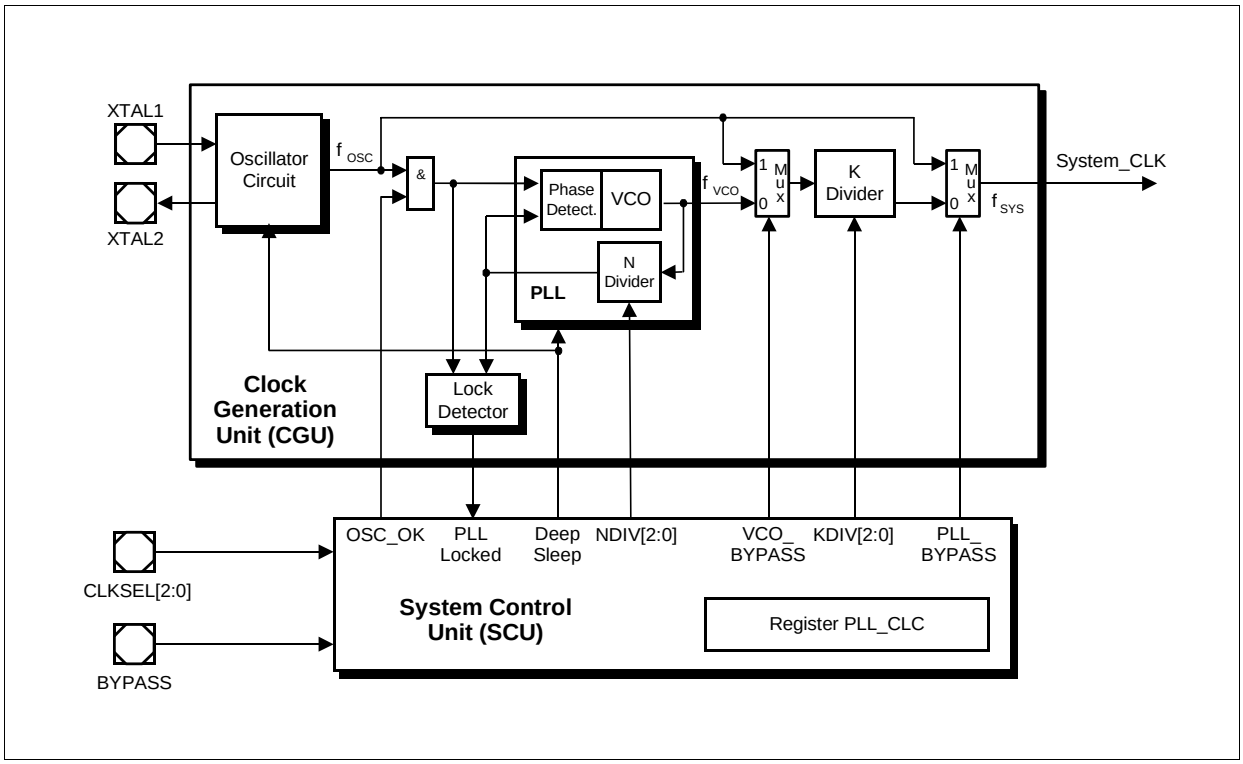


Figure 16 Clock Generation Unit Block Diagram

Besides the two XTAL pins for the oscillator, four other input pins are used for configuration of the clock generation unit: CLKSEL[2:0] and BYPASS. These inputs are checked by the SCU which generates the appropriate control signal and latches the state of these signals into register PLL_CLC.

Advance Information

Recommended Oscillator Circuits

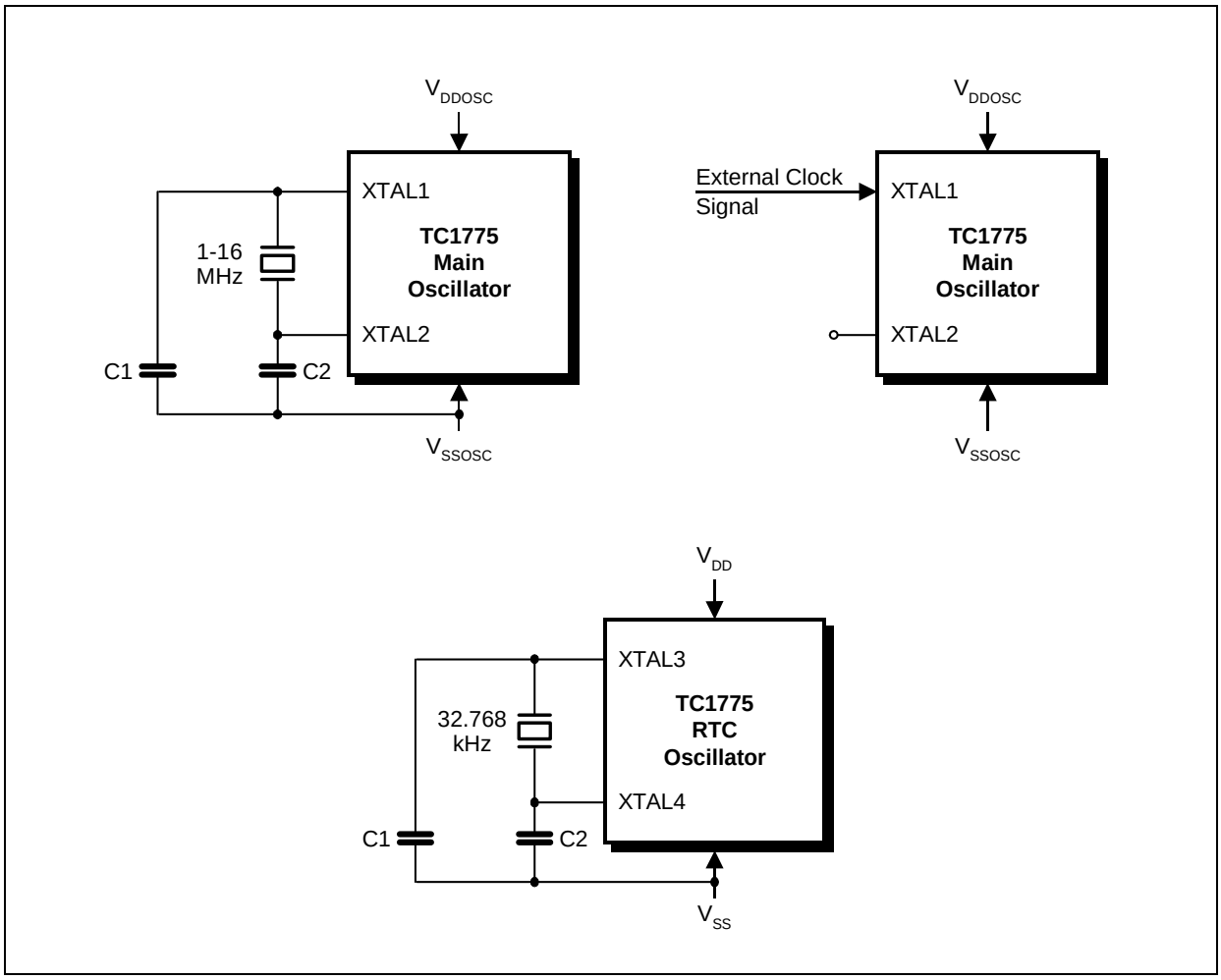


Figure 17 Oscillator Circuitries

For the main oscillator of the TC1775 the following external passive components are recommended:

- Crystal: max. 16 MHz, other characteristics are TBD.
- C1, C2: 18 pF

For the RTC oscillator of the TC1775 the following external passive components are recommended:

- Crystal: 32.768 KHz, other characteristics are TBD.
- C1, C2: 18 pF

A block capacitor between V_{DDOSC} and V_{SSOSC} is recommended, too,

Advance Information

Power Supply

The TC1775 provides an ingenious power supply concept in order to improve the EMI behavior as well as to minimize the crosstalk within on-chip modules.

Figure 18 shows the TC1775's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling. Also the operation margin is improved in sensitive modules like the A/D converter by noise reduction.

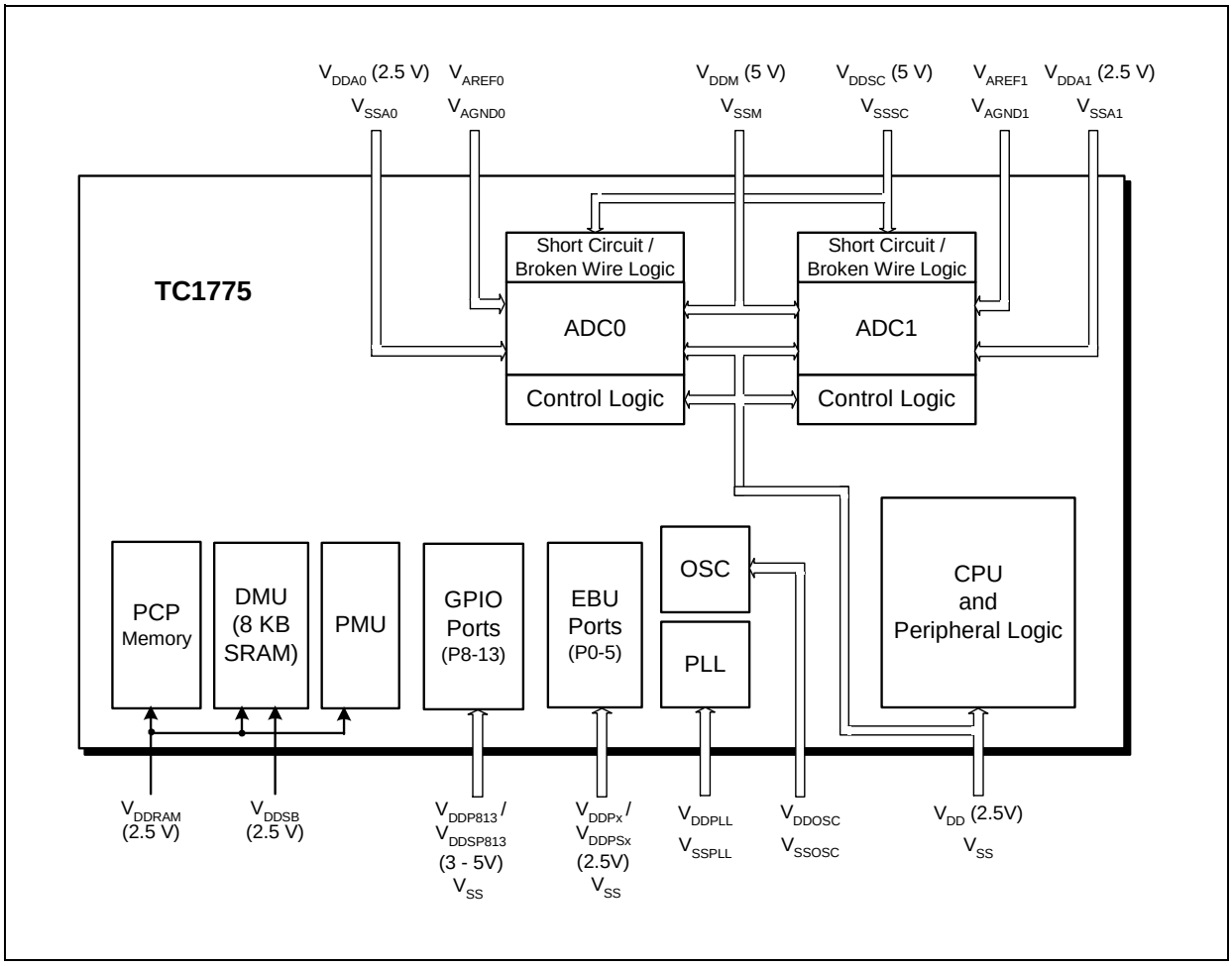


Figure 18 TC1775 Power Supply Concept

Advance Information

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature under bias	T_A	- 40	125	°C	-
Storage temperature	T_A	- 65	150	°C	-
Junction temperature	T_J	-	TBD	°C	-
Voltage on V_{DD} pins with respect to V_{SS} for 5.0V pins	V_{DD}	- 0.5	6.2	V	-
Voltage on V_{DD} pins with respect to V_{SS} for 2.5V pins	V_{DD}	- 0.5	3.25	V	-
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	- 0.5	V_{DD} + 0.5	V	-
Input current on any pin during overload condition	I_{IN}	- 10	10	mA	-
Absolute sum of all input currents during overload condition	ΣI_{IN}	-	| 100 |	mA	-
Power dissipation	V_{DISS}	-	TBD	W	-

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Advance Information

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1775. All parameters specified in the following table refer to these operating conditions, unless otherwise noticed.

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DD}	2.3	2.75	V	Logic and Bus (EBU) Ports
		3	5.5	V	Digital IO
Digital ground voltage	V_{SS}	0		V	-
Ambient temperature under bias	T_A	- 40	+ 125	°C	-
Analog supply voltage	V_{DDA}	-0.5	5.5	V	-
Analog reference voltage	V_{AREF}	4	V_{DDA} + 0.1	V	-
Analog ground voltage	V_{AGND}	V_{SS}	V_{SS} + 0.2	V	-
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	-
CPU clock	f_{CPU}	-	40	MHz	-
Overload current	I_{OV}	- 10	10	mA	1) 2) 3)
Short circuit current	I_{SC}	- 10	10	mA	1) 2) 4)
Absolute sum of overload + short circuit currents	$\Sigma \lvert I_{OV} \rvert + \lvert I_{SC} \rvert$	-	| 50 |	mA	2)
External Load Capacitance	C_L	-	40	pf	-

1) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$+0.5V or $V_{OV} < V_{SS}$-0.5V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

2) Not 100% tested, guaranteed by design and characterization.

3) Applicable for analog inputs.

4) Applicable for digital inputs.

Advance Information

Package Outline

Plastic Package, P-BGA-329-1 (SMD)
(Plastic Ball Grid Array Package)

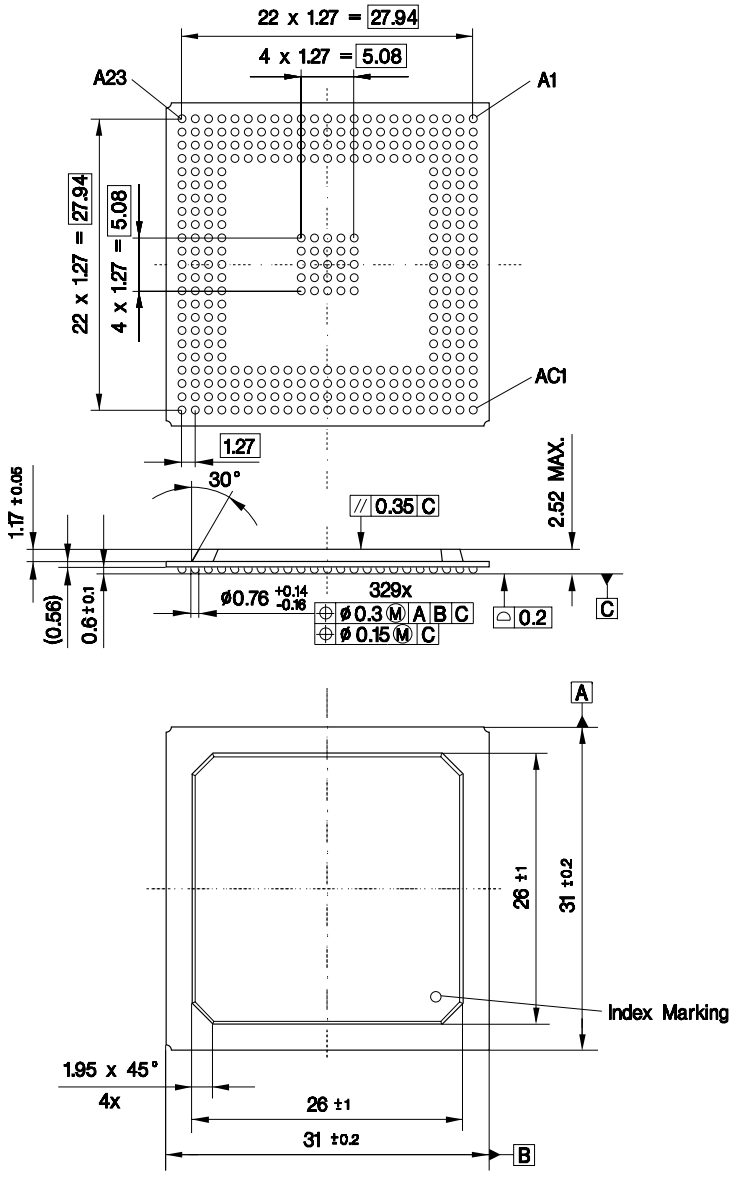


Figure 19 P-BGA-329-1 Package

Sorts of Packing

Package outlines for tubes, trays, etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device Dimensions in mm

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

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