

December 1995

Features

- 12A, 60V
- $r_{DS(ON)} = 0.150\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSpice Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RFD3055LE, RFD3055LESM, and RFP3055LE are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

The RFD3055LE, RFD3055LESM, and RFP3055LE incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

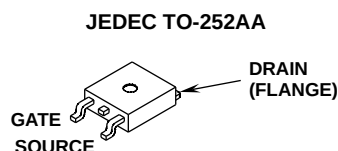
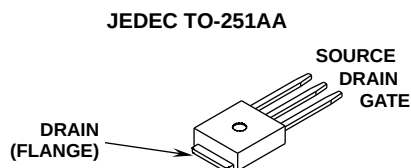
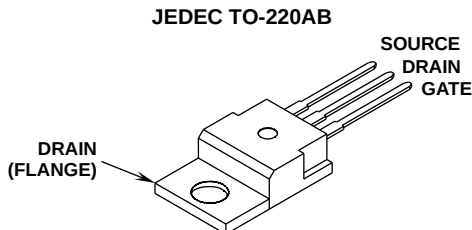
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFD3055LE	TO-251AA	F3055L
RFD3055LESM	TO-252AA	F3055L
RFP3055LE	TO-220AB	FP3055LE

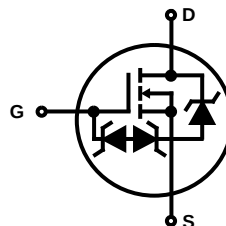
NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-252 variant in tape and reel, e.g. RFD3055LESM9A.

Formerly developmental type TA49158.

Packages



Symbol



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$

Drain-Source Voltage	V_{DSS}
Drain-Gate Voltage	V_{DGR}
Gate-Source Voltage	V_{GS}
Drain Current	
Continuous	I_D
Pulsed Drain Current	I_{DM}
Pulsed Avalanche Rating	E_{AS}
Power Dissipation	
$T_C = +25^\circ\text{C}$	P_D
Derate above $+25^\circ\text{C}$	
Operating and Storage Temperature	T_{STG}, T_J
Soldering Temperature of Leads for 10s	T_L
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD

RFD3055LE, RFD3055LESM, RFP3055LE	UNITS
60	V
60	V
± 10	V
12	A
Refer to Peak Current Curve	
Refer to UIS Curve	
48	W
0.323	W/ $^\circ\text{C}$
-55 to +175	$^\circ\text{C}$
260	$^\circ\text{C}$
2	kV

Specifications RFD3055LE, RFD3055LESM, RFP3055LE

Electrical Specifications $T_C = +25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V		60	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V	T _C = +25°C	-	-	1	μA
			T _C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±10V		-	-	10	μA
On Resistance	r _{DS(ON)}	I _D = 12A, V _{GS} = 5V		-	-	0.150	Ω
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 12A, R _L = 2.5Ω, V _{GS} = 5V, R _{GS} = 5Ω		-	-	120	ns
Turn-On Delay Time	t _{D(ON)}			-	10	-	ns
Rise Time	t _R			-	70	-	ns
Turn-Off Delay Time	t _{D(OFF)}			-	25	-	ns
Fall Time	t _F			-	30	-	ns
Turn-Off Time	t _{OFF}			-	-	85	ns
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 48V, I _D = 12A, R _L = 4Ω	-	28	35	nC
Gate Charge at 5V	Q _{G(5)}	V _{GS} = 0V to 5V		-	15	18	nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 0V to 1V		-	1.0	1.2	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		-	850	-	pF
Output Capacitance	C _{OSS}			-	170	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	100	-	pF
Thermal Resistance Junction-to-Case	R _{θJC}			-	-	3.1	°C/W
Thermal Resistance Junction-to-Ambient	R _{θJA}	TO-251, TO-252, TO-220		-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 12\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 12\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	100	ns

Typical Performance Curves

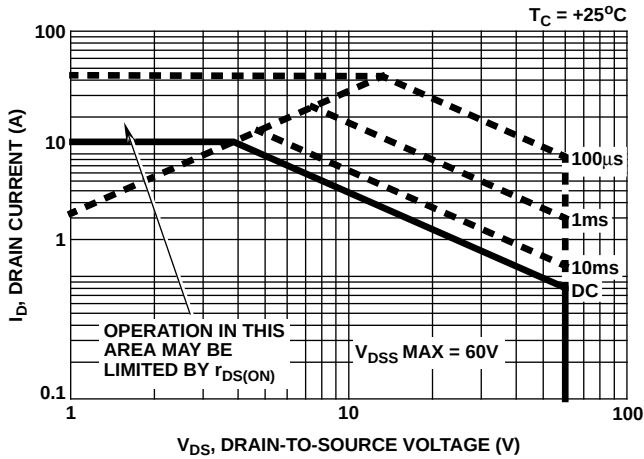


FIGURE 1. SAFE OPERATING AREA CURVE

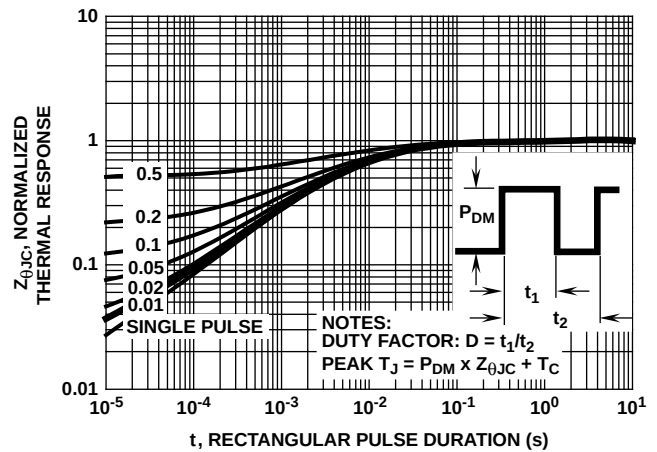


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

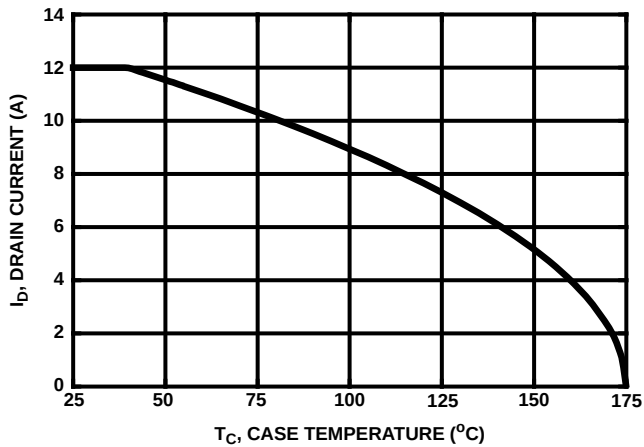


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

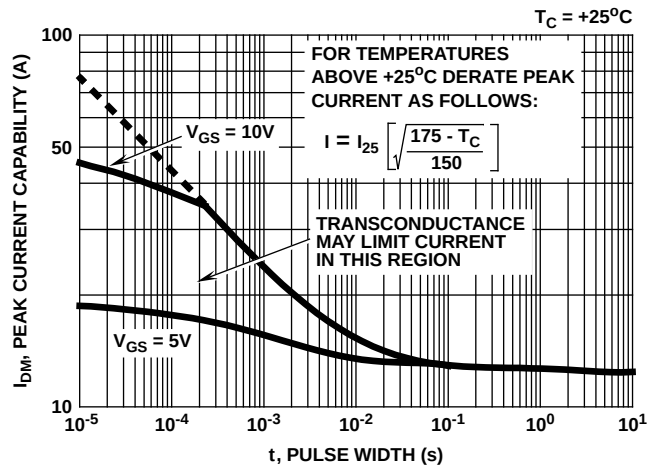


FIGURE 4. PEAK CURRENT CAPABILITY

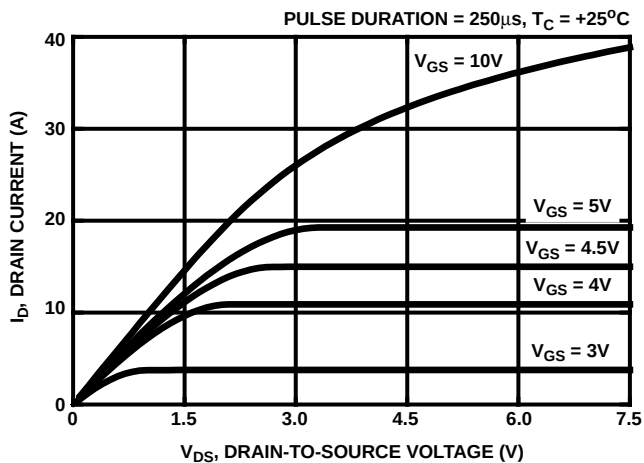


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

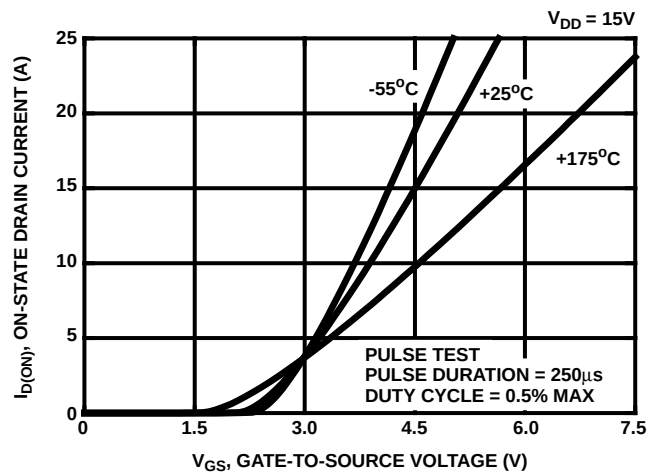


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

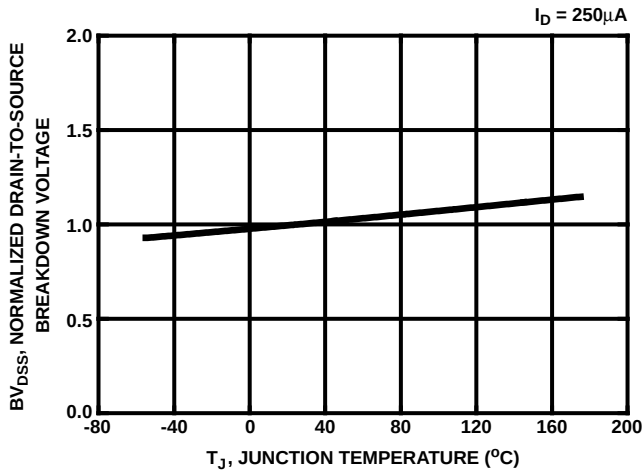


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

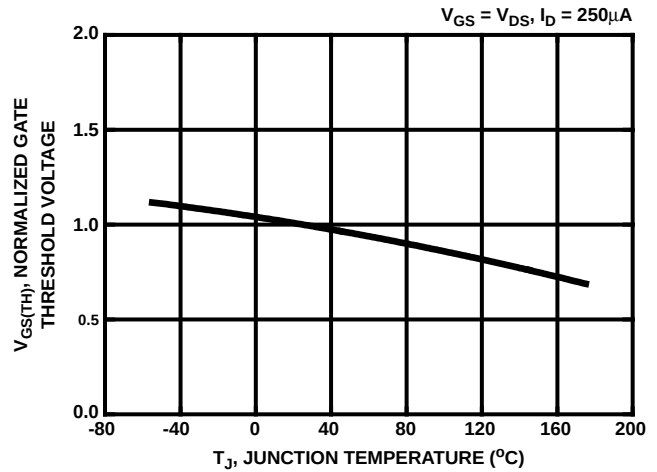


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

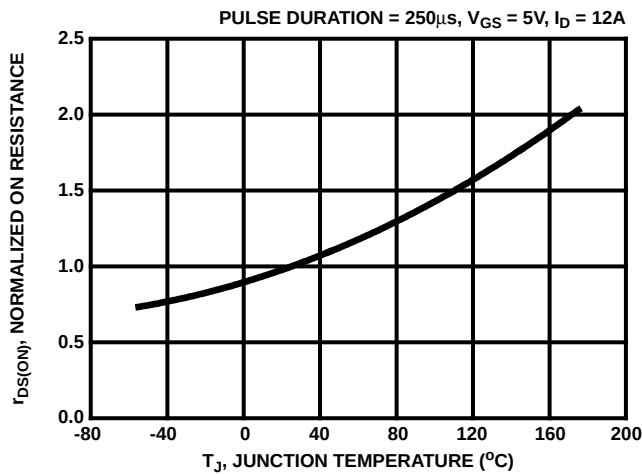


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

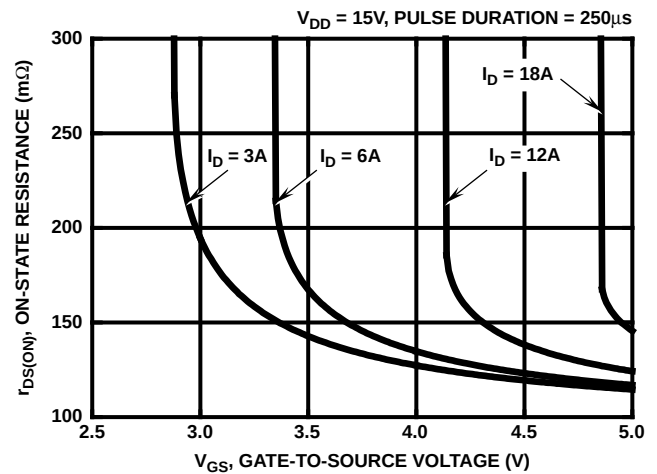


FIGURE 10. TYPICAL $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

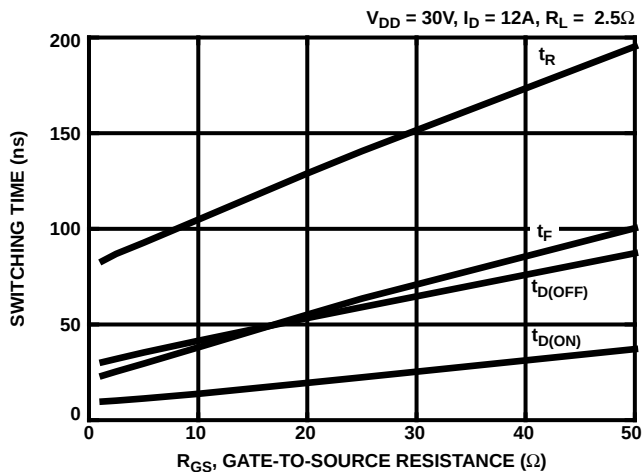


FIGURE 11. TYPICAL SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

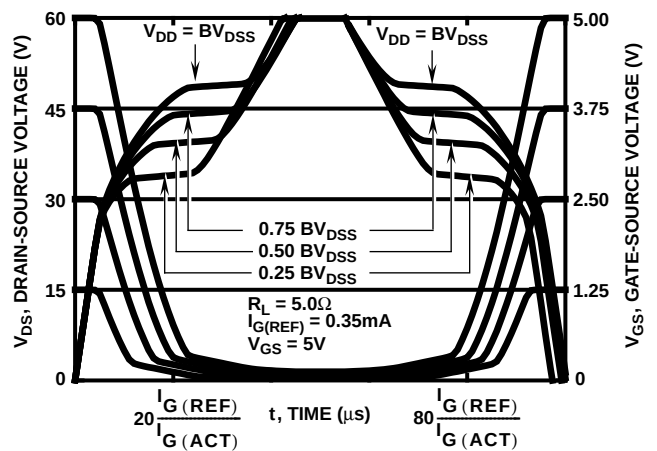


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

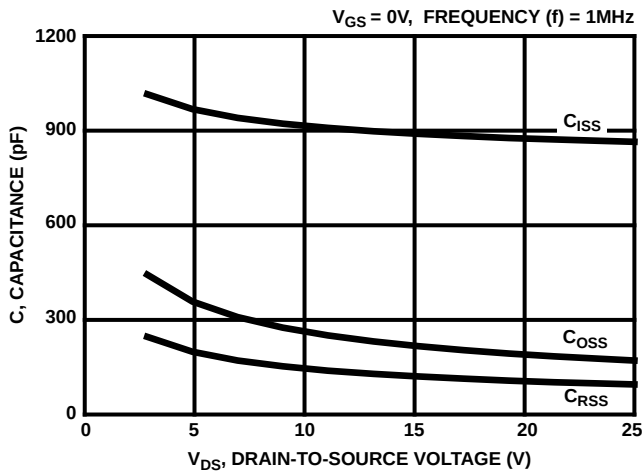


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

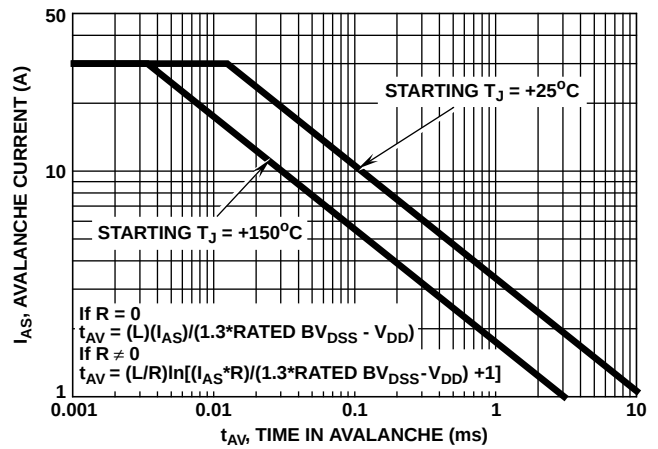


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

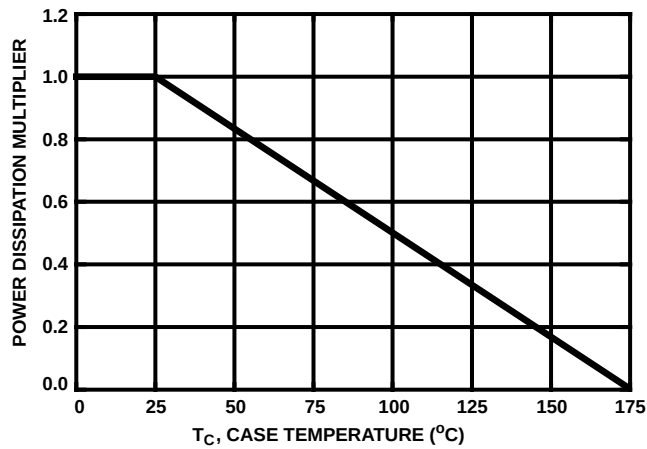


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

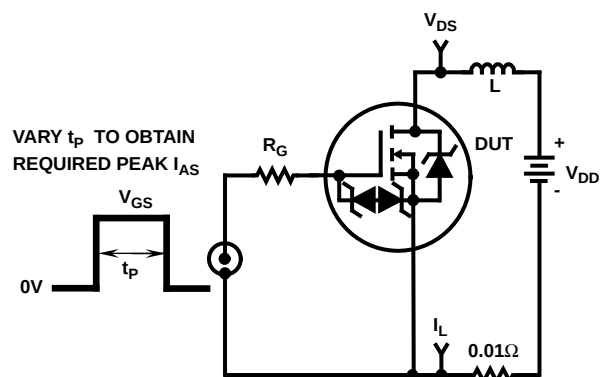


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

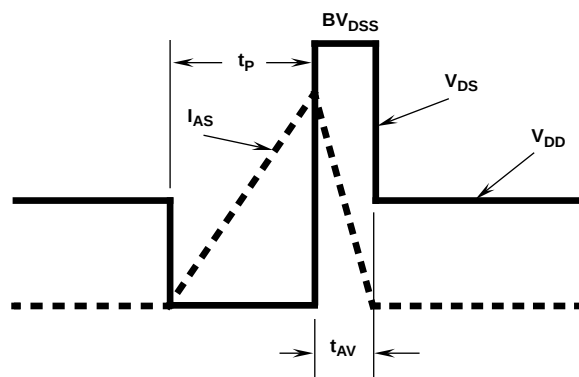


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

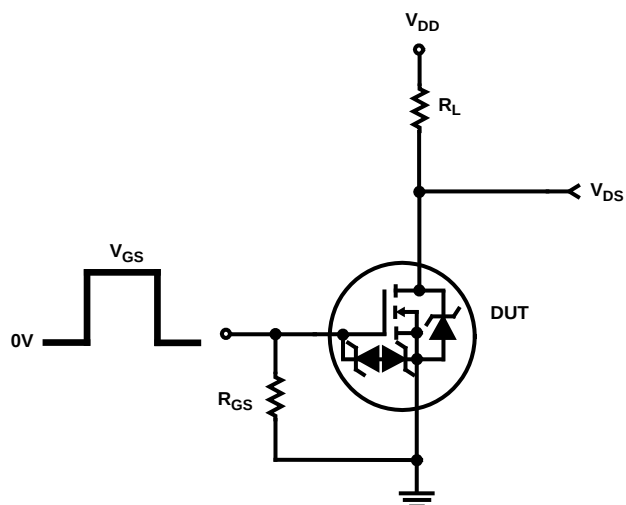


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

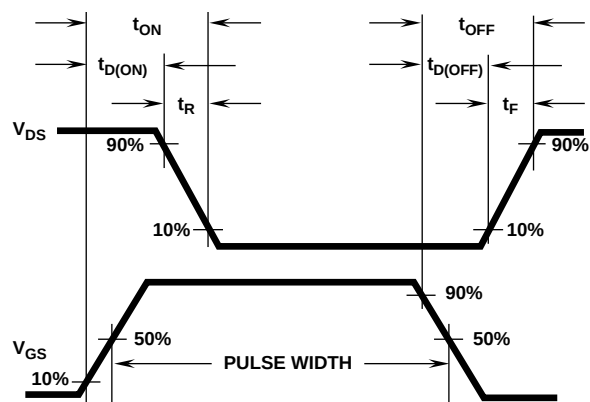


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD3055LE, RFD3055LESM, RFP3055LE

.SUBCKT RFD3055LE 2 1 3; rev 1/30/95

CA 12 8 1.68e-9
CB 15 14 1.78e-9
CIN 6 8 0.769e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.28
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.6e-9
LSOURCE 3 7 4.6e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.176e-3
RLDRAIN 2 5 10
RGATE 9 20 9.84
RLGATE 1 9 46
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 76.56e-3
RLSOURCE 3 7 46
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.516

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/31.7,6))}

.MODEL DBDMOD D (IS = 3.61e-13 RS = 1.78e-2 TRS1 = 1.70e-2 TRS2 = -4.69e-6 CJO = 3.88e-10 TT = 3.6e-8)
.MODEL DBKMOD D (RS = 0.4731 TRS1 = -2.19e-3 TRS2 = 4.7e-5)
.MODEL DESD1MOD D (BV = 13.5 NBV = 17.5 IBV = 2.5e-4 RS = 22.2 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 12.86 NBV = 22 IBV = 2.5e-4 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 0.48e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.082 KP = 18.36 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.06e-3 TC2 = -6.22e-7)
.MODEL RDSMOD RES (TC1 = 4.48e-3 TC2 = 1.77e-5)
.MODEL RSCLMOD RES (TC1 = 3.55e-3 TC2 = 0.20e-5)
.MODEL RVTOMOD RES (TC1 = -1.85e-3 TC2 = -4.13e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.4 VOFF = -2.4)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.4 VOFF = -4.4)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.85 VOFF = 2.15)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.15 VOFF = -2.85)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

