

N-channel dual-gate MOS-FET

BF909AWR

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

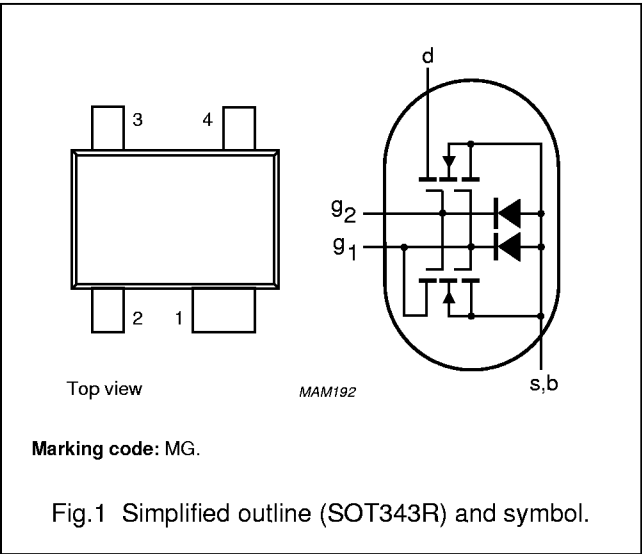
- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communication equipment.

DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g ₂	gate 2
4	g ₁	gate 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		–	–	7	V
I _D	drain current		–	–	40	mA
P _{tot}	total power dissipation		–	–	280	mW
T _j	operating junction temperature		–	–	150	°C
y _{fs}	forward transfer admittance		36	43	50	mS
C _{ig1-s}	input capacitance at gate 1		–	3.6	4.3	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	–	30	50	fF
F	noise figure	f = 800 MHz	–	2	2.8	dB

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

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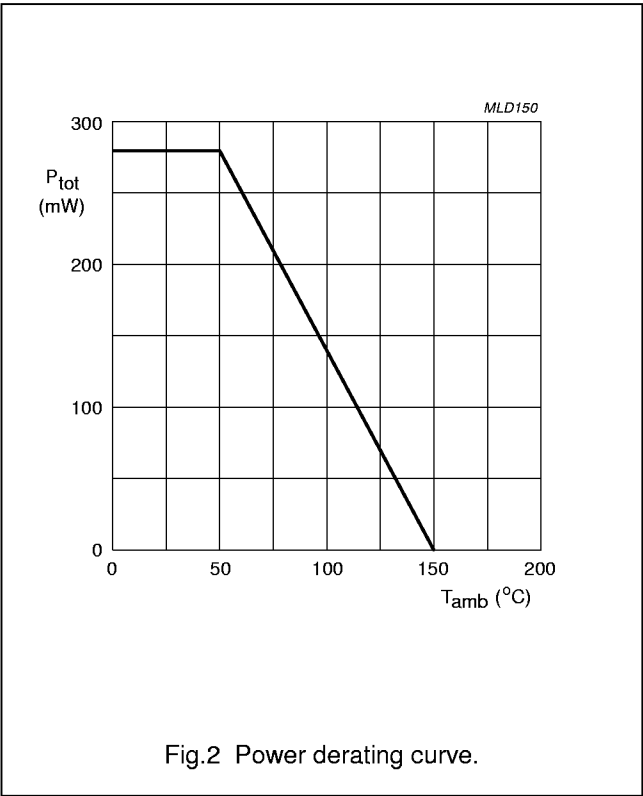
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	7	V
I _D	drain current		–	40	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	up to T _{amb} = 50 °C; see Fig.2; note 1	–	280	mW
T _{stg}	storage temperature range		–65	+150	°C
T _j	operating junction temperature		–	+150	°C

Note

- 1. Device mounted on a printed-circuit board.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point	note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. Soldering point of the source lead.

STATIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	15	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\text{ mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 20\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5\text{ V}$; $I_D = 20\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 120\text{ k}\Omega$; note 1	12	20	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 5\text{ V}$	—	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 5\text{ V}$	—	50	nA

Note

1. R_{G1} connects gate 1 to $V_{GG} = 5\text{ V}$.

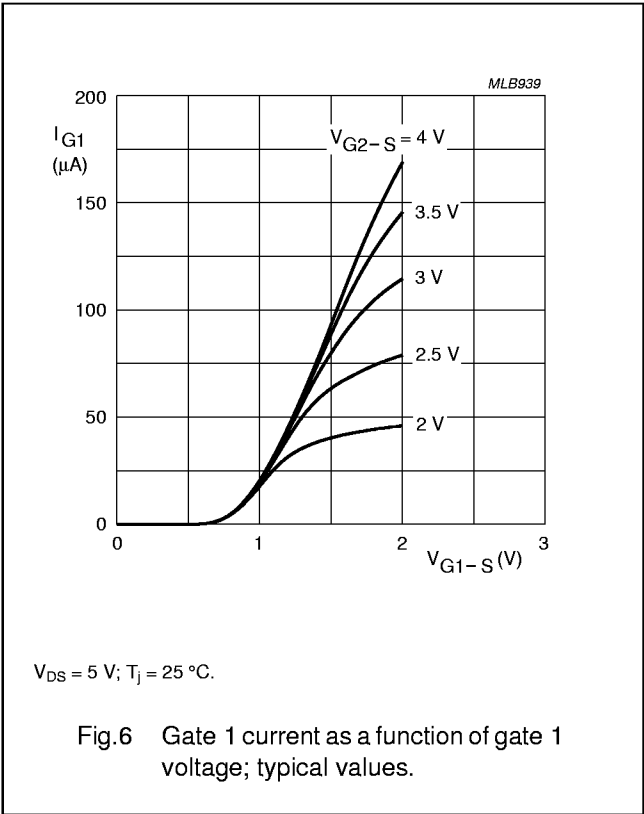
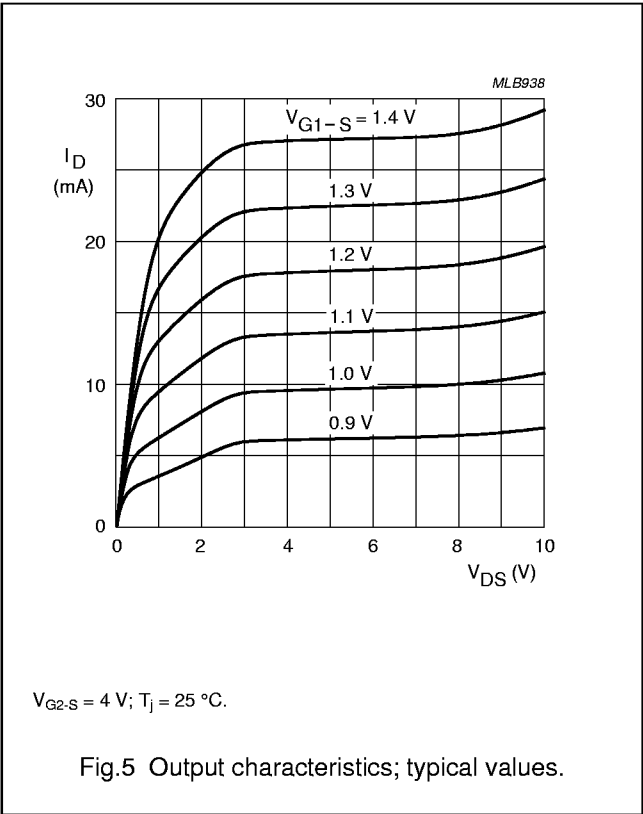
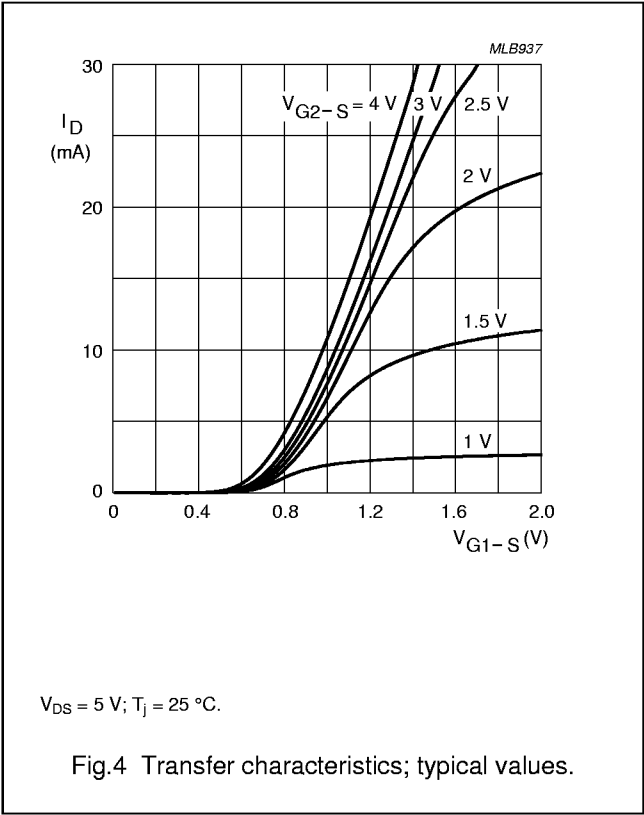
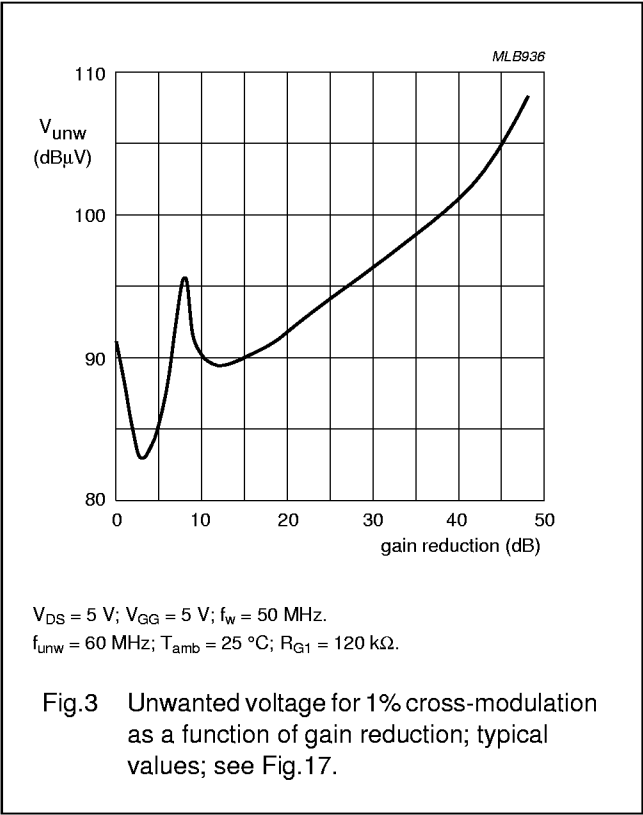
DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ }^{\circ}\text{C}$	36	43	50	mS
C_{ig1-s}	input capacitance at gate 1	$f = 1\text{ MHz}$	—	3.6	4.3	pF
C_{ig2-s}	input capacitance at gate 2	$f = 1\text{ MHz}$	—	2.3	3	pF
C_{os}	drain-source capacitance	$f = 1\text{ MHz}$	—	2.4	3	pF
C_{rs}	reverse transfer capacitance	$f = 1\text{ MHz}$	—	30	50	fF
F	noise figure	$f = 800\text{ MHz}$; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	—	2	2.8	dB

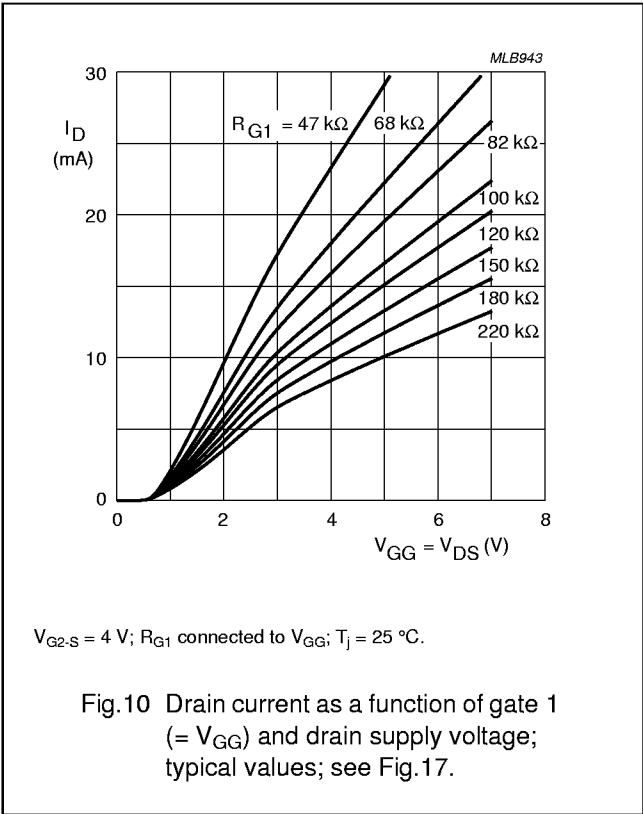
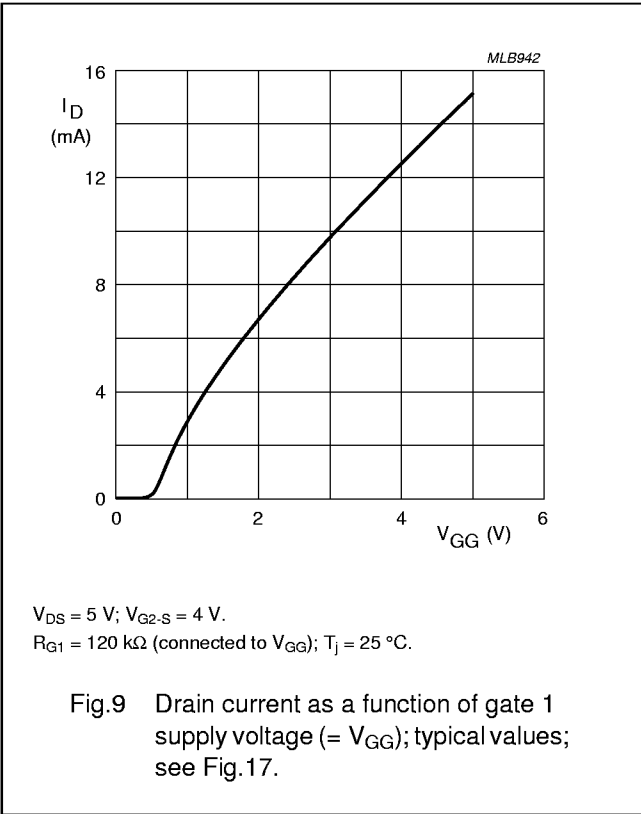
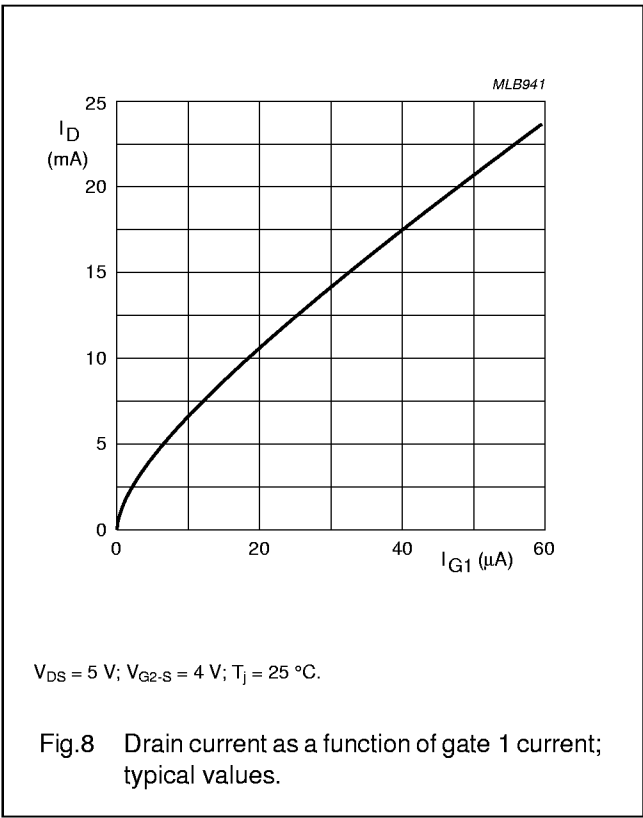
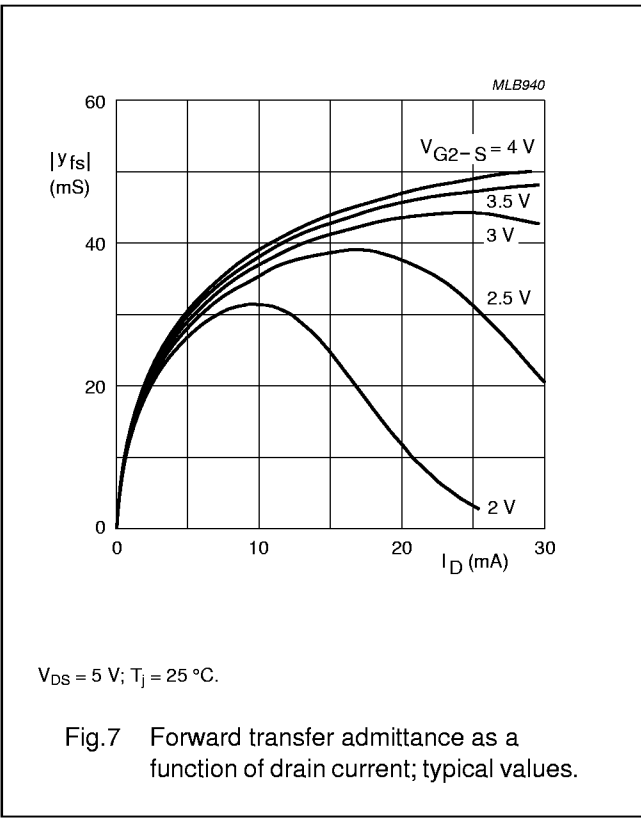
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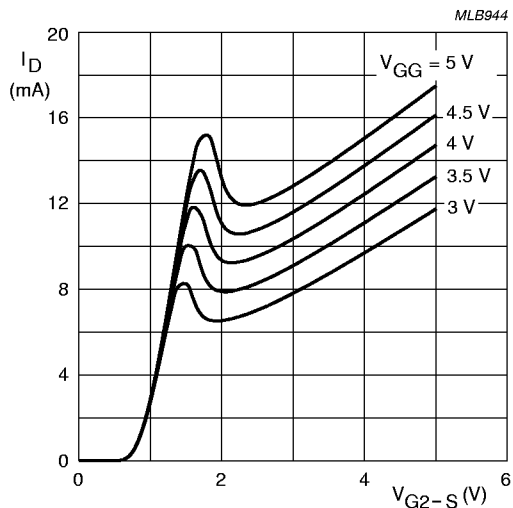
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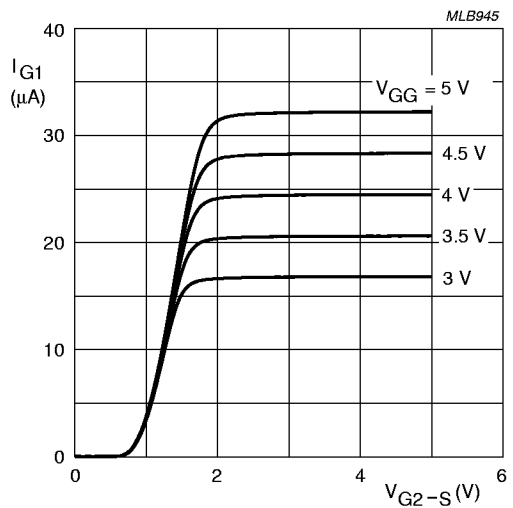
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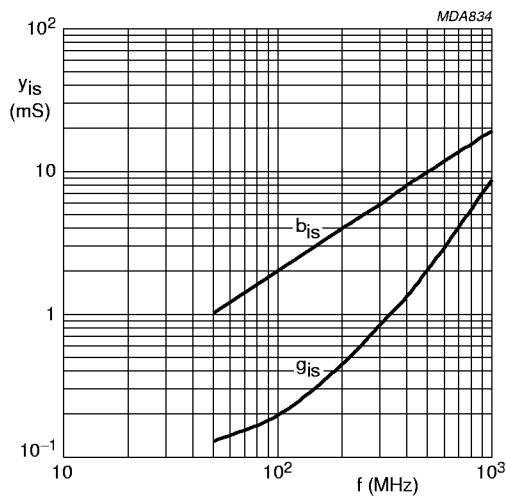
$V_{DS} = 5\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; $R_{G1} = 120\text{ k}\Omega$ (connected to V_{GG}).

Fig.11 Drain current as a function of gate 2 voltage; typical values; see Fig.17.



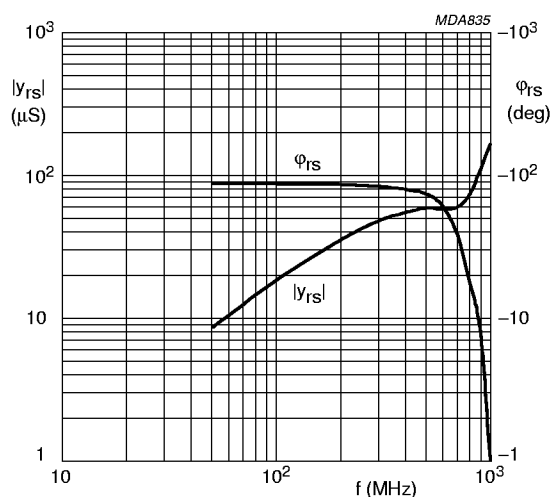
$V_{DS} = 5\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; $R_{G1} = 120\text{ k}\Omega$ (connected to V_{GG}).

Fig.12 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.17.



$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

Fig.13 Input admittance as a function of frequency; typical values.

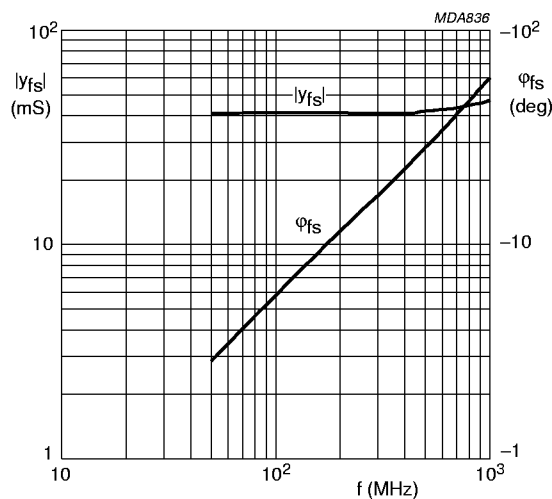


$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.

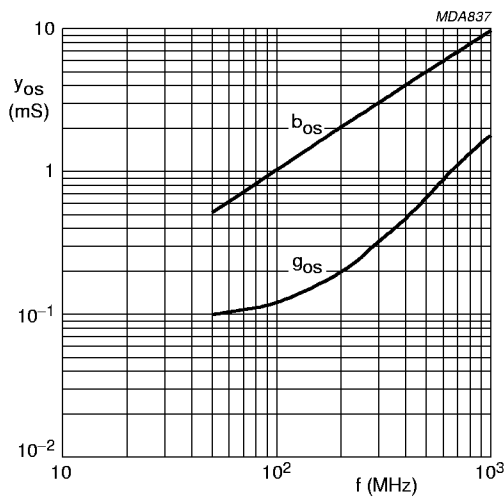
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$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.15 Forward transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.16 Output admittance as a function of frequency; typical values.

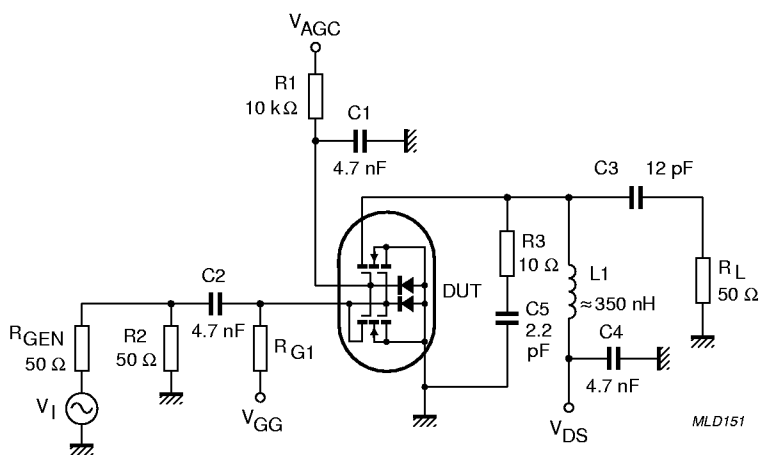


Fig.17 Cross-modulation test set-up.

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Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	-6.0	4.070	172.7	0.001	86.9	0.989	-3.1
100	0.980	-11.8	4.041	165.4	0.002	82.9	0.987	-6.1
200	0.956	-23.0	3.897	151.3	0.003	73.4	0.978	-12.1
300	0.911	-33.3	3.654	136.9	0.004	70.6	0.962	-17.7
400	0.888	-44.2	3.531	125.4	0.005	67.4	0.951	-23.3
500	0.845	-53.5	3.265	113.4	0.005	66.6	0.934	-28.6
600	0.803	-62.3	3.055	102.3	0.005	75.0	0.917	-33.6
700	0.758	-70.9	2.836	91.3	0.004	93.1	0.902	-38.5
800	0.719	-78.8	2.653	80.9	0.004	115.2	0.889	-43.5
900	0.683	-86.4	2.456	70.9	0.006	132.7	0.878	-48.3
1000	0.653	-93.9	2.299	61.4	0.008	141.0	0.870	-53.3

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	F _{min} (dB)	Γ _{opt}		r _n
		(ratio)	(deg)	
800	2.00	0.603	67.71	0.581

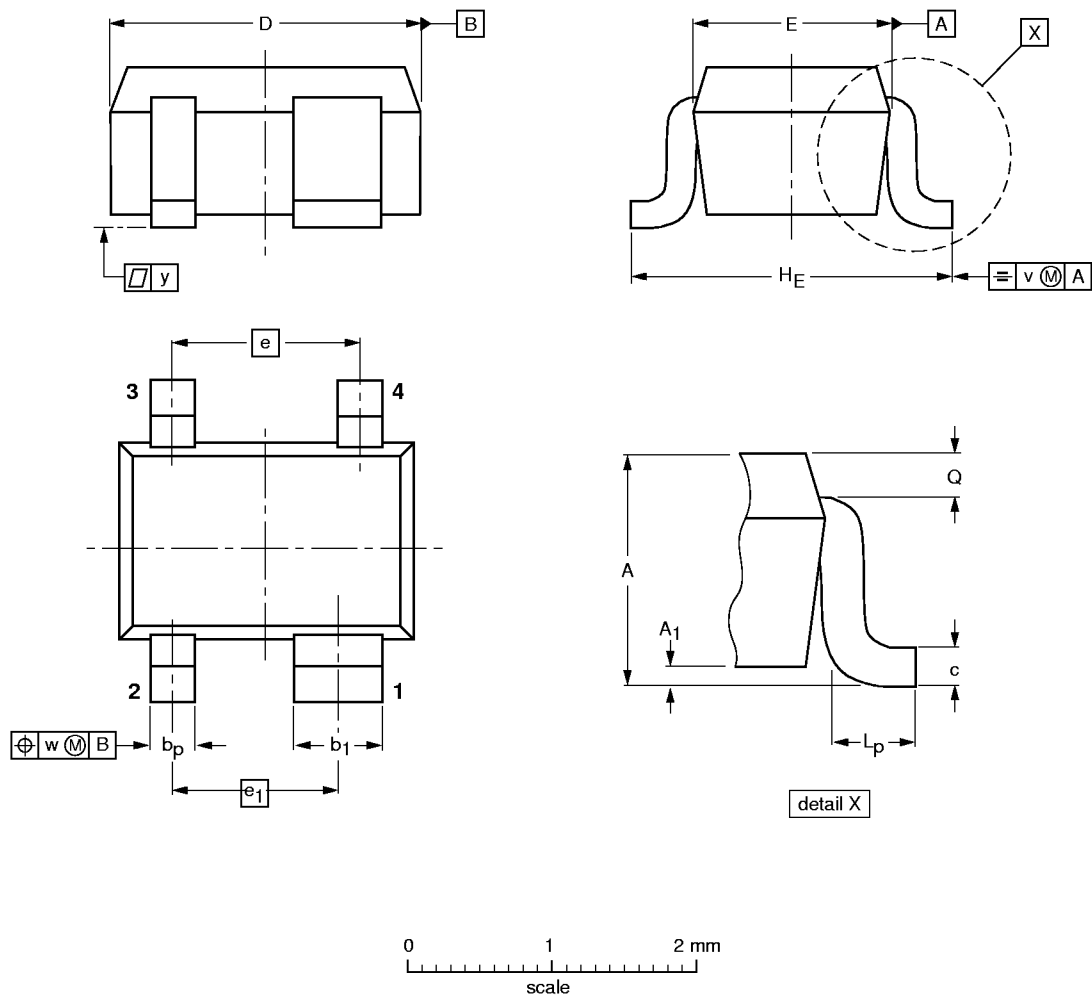
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PACKAGE OUTLINE

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21