

# High Precision Hall Effect Latch for 5V Applications

## TLI4963-1M

SP001370094

### Hall Effect Latch

### Data Sheet

Revision 1.0, 2016-01-11

Sense & Control

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**Product Description**

**1 Product Description**



**1.1 Overview**

The TLI4963-1M is a high precision Hall effect sensor with a latch characteristic and highly accurate switching thresholds for operating temperatures up to 125°C.

Characteristic	Supply Voltage	Supply Current	Sensitivity	Interface	Temperature
Hall Effect Latch	3.0 ~ 5.5 V	1.5 mA	High B <sub>OP</sub> : +2.0 mT B <sub>RP</sub> : -2.0 mT	Open Drain Output	-40°C to 125°C



**Figure 1 Image of TLI4963-1M in the PG-SOT23-3-15 Package**

**1.2 Features**

- 3.0 V to 5.5 V operating supply voltage
- Operation from regulated power supply
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 0.28 μs)
- 4kV ESD (HBM) performance
- Small SMD package PG-SOT23-3-15
- For industrial and consumer applications, not qualified for automotive applications

**1.3 Target Applications**

Target applications for the TLI4963-1M Hall switch are all applications which require a high precision Hall Switch with an operating temperature range from -40°C to 125°C.

The magnetic behavior as a latch and switching thresholds of typical 2mT make the device especially suited for the use with a pole wheel for index counting applications e.g. power closing and window lifter or brush less DC motors for commutation.

**Table 1 Ordering Information**

Product Name	Product Type	Ordering Code	Package
TLI4963-1M	Hall Latch	SP001370094	PG-SOT23-3-15

Functional Description

## 2 Functional Description

### 2.1 General

The TLI4963-1M is an integrated Hall effect latch designed specifically for highly accurate applications where the sensor is connected to a regulated power supply voltage in the range of 3.0V to 5.5V. It provides a temperature stability of the magnetic thresholds.

### 2.2 Pin Configuration (top view)

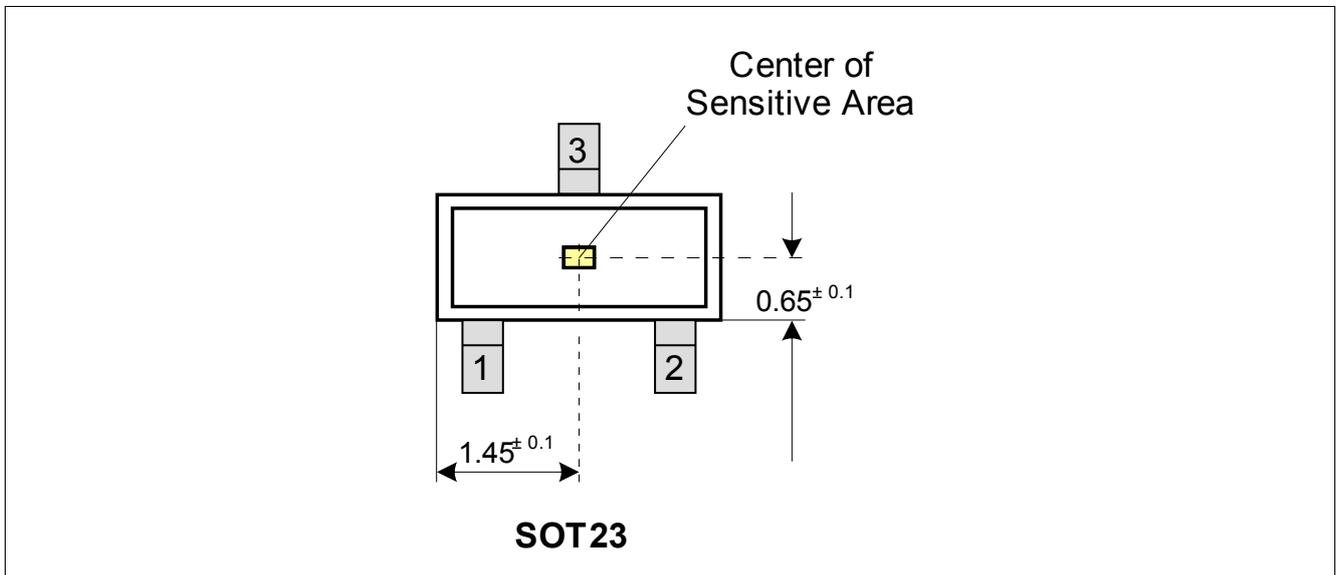


Figure 2 Pin Configuration and Center of Sensitive Area

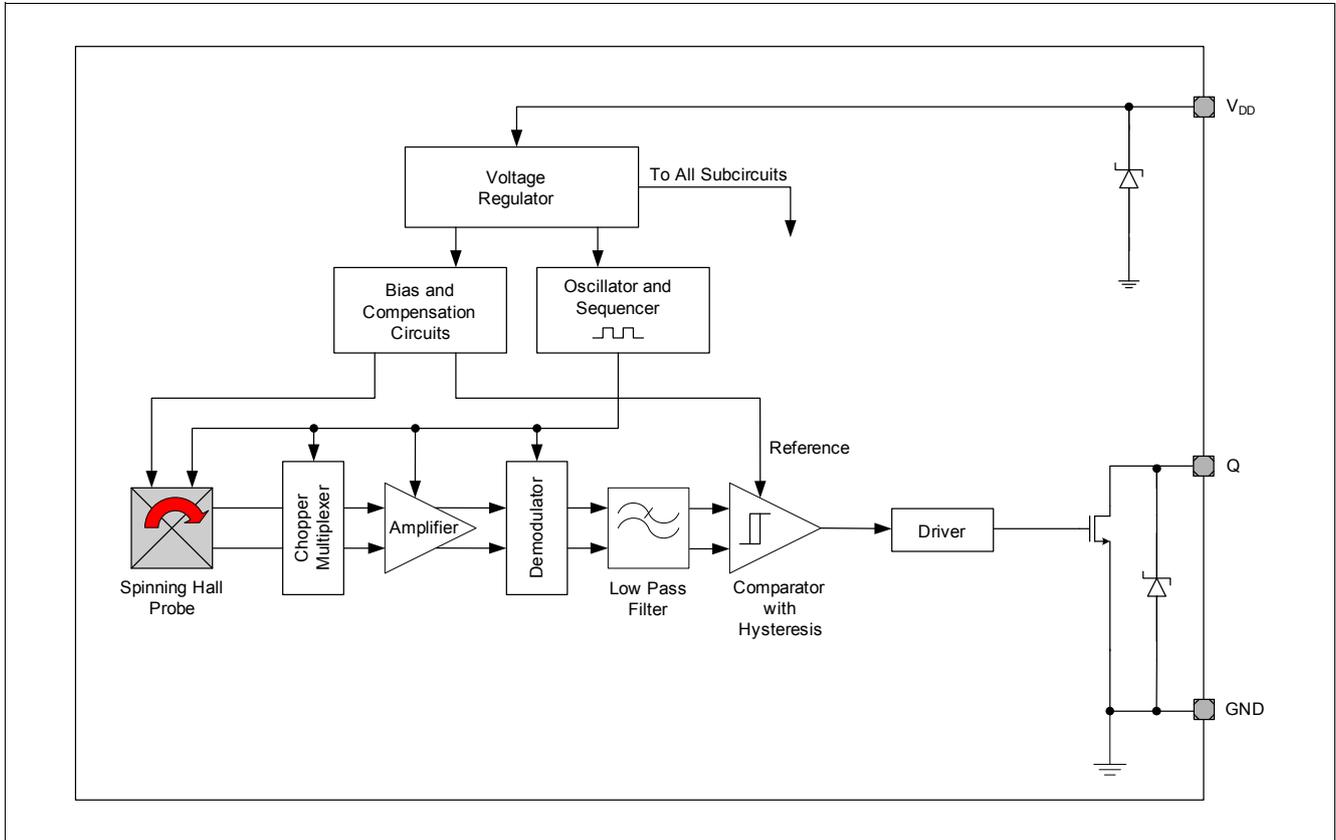
### 2.3 Pin Description

Table 2 Pin Description PG-SOT23-3-15

Pin No.	Symbol	Function
1	VDD	Supply voltage
2	Q	Output
3	GND	Ground

**Functional Description**

**2.4 Block Diagram**



**Figure 3 Functional Block Diagram TLI4963-1M**

**2.5 Functional Block Description**

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

Functional Description

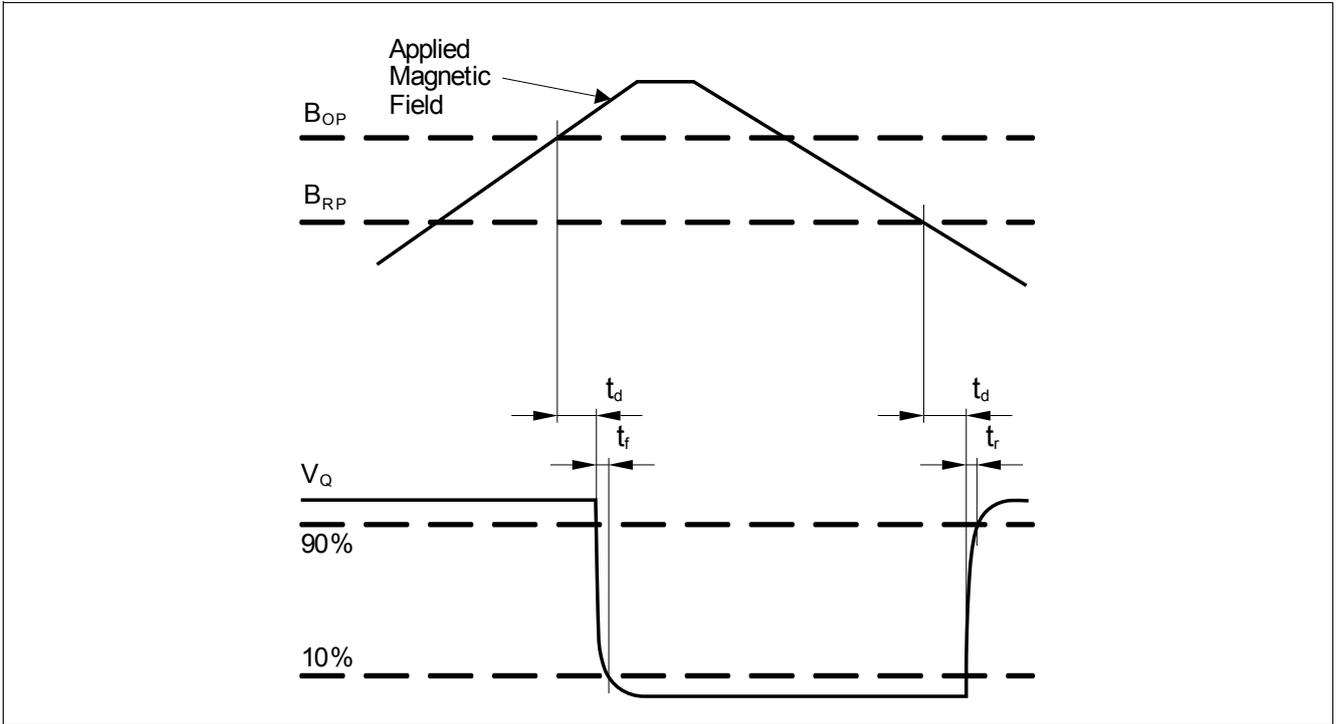


Figure 4 Timing Diagram TLI4963-1M

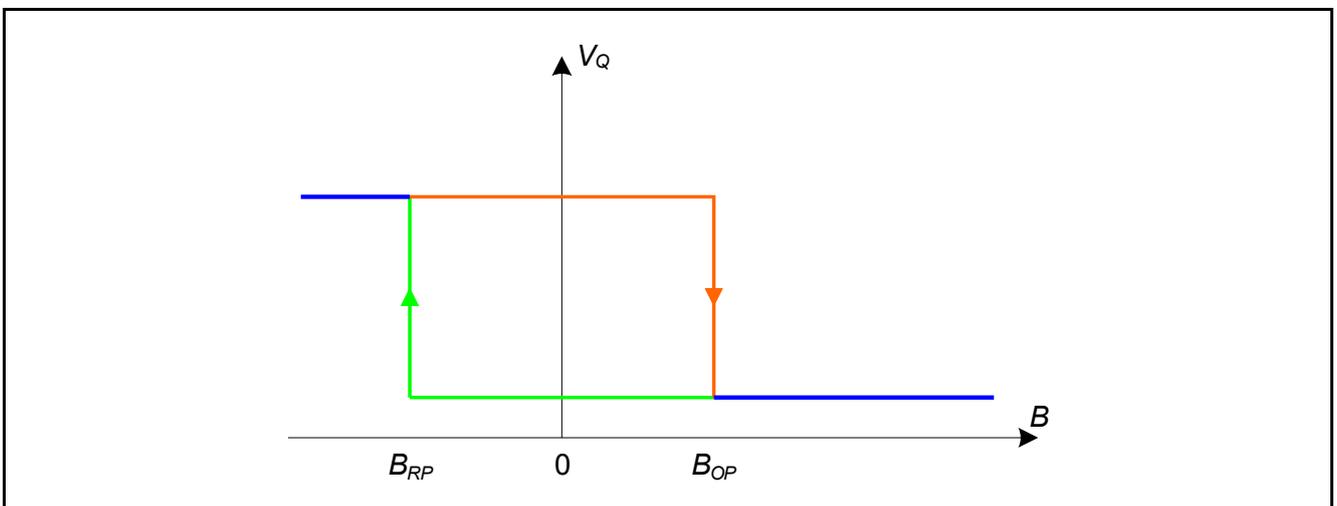


Figure 5 Output Signal TLI4963-1M

Functional Description

2.6 Default Start-up Behavior

The magnetic thresholds exhibit a hysteresis  $B_{HYS} = B_{OP} - B_{RP}$ . In case of a power-on with a magnetic field  $B$  within hysteresis ( $B_{OP} > B > B_{RP}$ ) the output of the sensor is set to the pull up voltage level ( $V_Q$ ) per default. After the first crossing of  $B_{OP}$  or  $B_{RP}$  of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

$V_{DDA}$  is the internal supply voltage which is following the external supply voltage  $V_{DD}$ .

This means for  $B > B_{OP}$  the output is switching, for  $B < B_{RP}$  and  $B_{OP} > B > B_{RP}$  the output stays at  $V_Q$ .

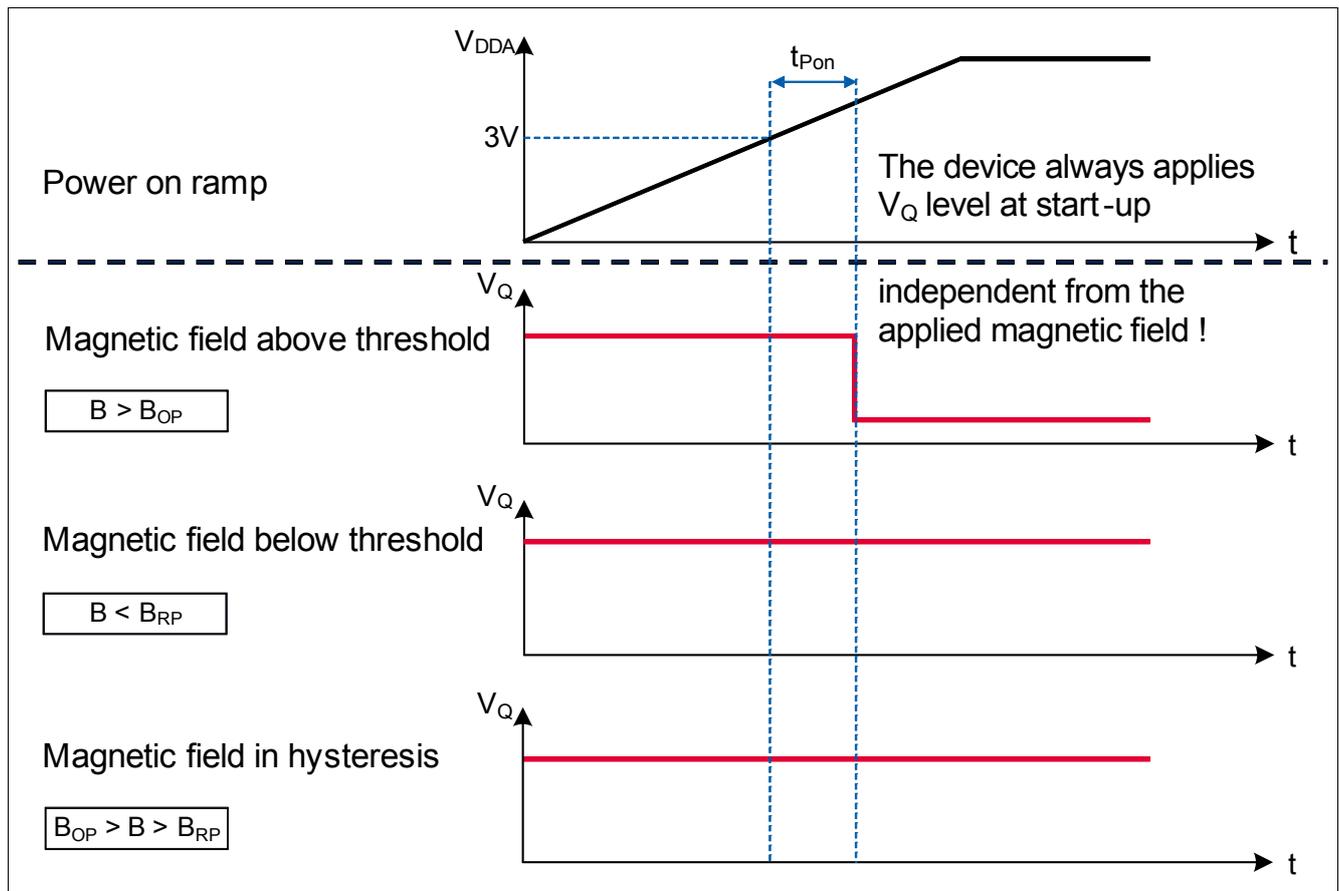
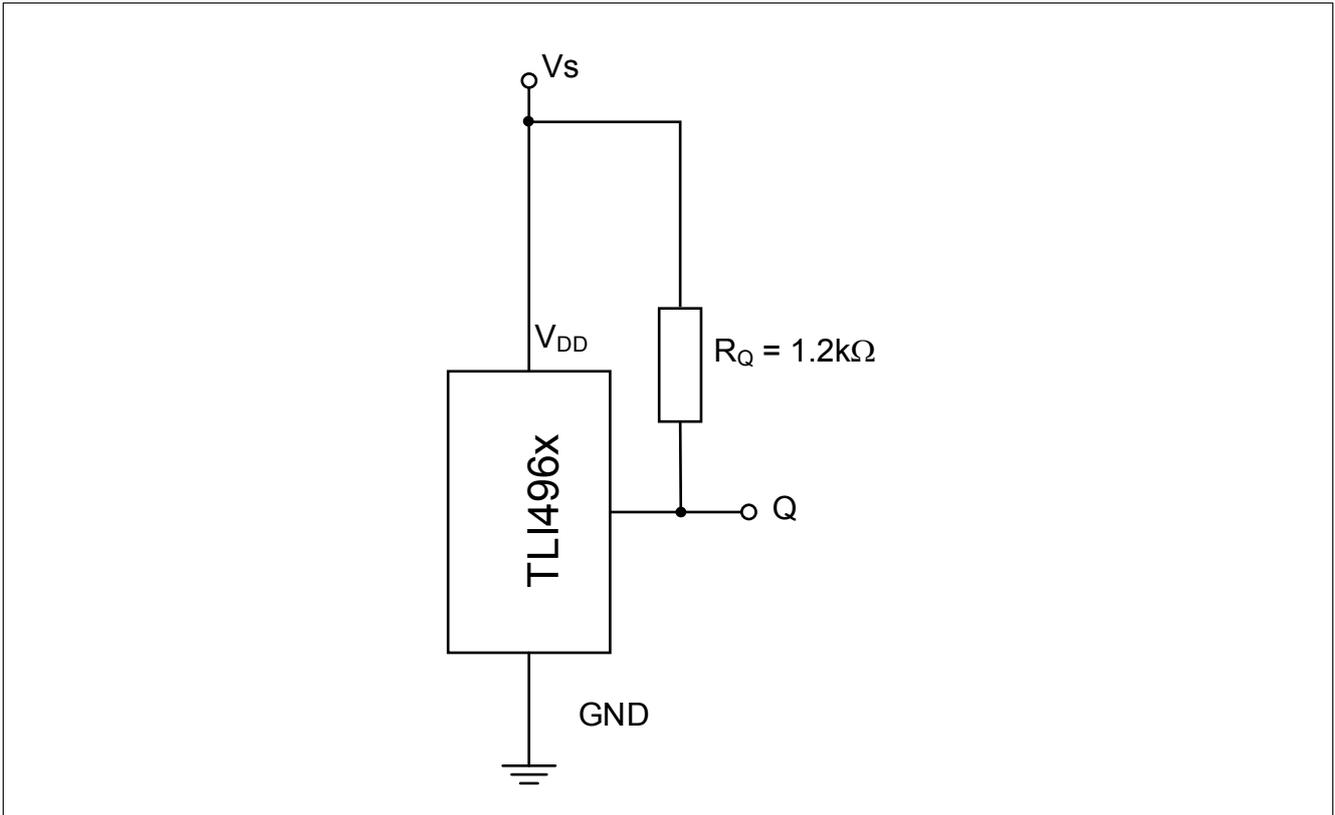


Figure 6 Illustration of the Start-up Behavior of the TLI4963-1M

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**Specification****3 Specification****3.1 Application Circuit**

The following **Figure 7** shows one option of an application circuit.



**Figure 7 Application Circuit**

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**Specification**
**3.2 Absolute Maximum Ratings**
**Table 3 Absolute Maximum Rating Parameters**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	-0.3		6	V	
Output voltage	$V_Q$	-0.5		6	V	
Ambient temperature <sup>1)</sup>	$T_A$	-40		150	°C	for 2000h (not additive)
Thermal resistance Junction ambient	$R_{thJA}$			300	K/W	for PG-SOT23-3-15 (2s2p)
Thermal resistance Junction lead	$R_{thJL}$			100	K/W	for PG-SOT23-3-15

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

Calculation of the dissipated power  $P_{DIS}$  and junction temperature  $T_J$  of the chip (SOT23 example):

e.g. for:  $V_{DD} = 5\text{ V}$ ,  $I_S = 2\text{ mA}$ ,  $V_{QSAT} = 0.5\text{ V}$ ,  $I_Q = 1\text{ mA}$

Power dissipation:  $P_{DIS} = 5\text{ V} \times 2\text{ mA} + 0.5\text{ V} \times 1\text{ mA} = 10\text{ mW} + 0.5\text{ mW} = 10.5\text{ mW}$

Temperature  $\Delta T = R_{thJA} \times P_{DIS} = 300\text{ K/W} \times 10.5\text{ mW} = 3.15\text{ K}$

For  $T_A = 150\text{ °C}$ :  $T_J = T_A + \Delta T = 150\text{ °C} + 3.15\text{ K} = 153.15\text{ °C}$

**Table 4 ESD Protection<sup>1)</sup> ( $T_A = 25\text{ °C}$ )**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM) <sup>2)</sup>	$V_{ESD}$	-4		4	kV	$R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$
ESD voltage (CDM) <sup>3)</sup>	$V_{ESD}$	-1		1	kV	

1) Characterization of ESD is carried out on a sample basis, not subject to production test.

2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.

3) Charged Device Model (CDM), ESD susceptibility according to JEDEC JESD22-C101.

Specification

### 3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLI4963-1M.

All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

**Table 5 Operating Conditions Parameters**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{DD}$	3.0		5.5	V	
Output voltage	$V_Q$	-0.3		5.5	V	
Ambient temperature	$T_A$	-40		125	°C	
Output current	$I_Q$	0		5	mA	
Magnetic signal input frequency <sup>1)</sup>	$f_{SW}$	0		10	kHz	

1) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3dB corner frequency of the internal low-pass filter in the signal path.

### 3.4 Electrical and Magnetic Characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to  $V_{DD} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ . The below listed specification is valid in combination with the application circuit shown in [Figure 7](#).

**Table 6 General Electrical Characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply current	$I_S$	1.1	1.5	2.5	mA	
Reverse current <sup>1)</sup>	$I_{SR}$			2.5	mA	for $V_{DD} = -0.3\text{ V}$ and $125^\circ\text{C}$
Output saturation voltage	$V_{QSAT}$		0.2	0.5	V	$I_Q = 5\text{ mA}$
Output leakage current	$I_{QLEAK}$			10	µA	
Output fall time <sup>1)</sup>	$t_f$	0.17	0.24	1	µs	1.2 kΩ / 50 pF, see <a href="#">Figure 4</a>
Output rise time <sup>1)</sup>	$t_r$	0.4	0.5	1	µs	1.2 kΩ / 50 pF, see <a href="#">Figure 4</a>
Output jitter <sup>1)2)</sup>	$t_{QJ}$		0.28	1	µs	For square wave signal with 1 kHz
Delay time <sup>1)3)</sup>	$t_d$	11.5	15	30	µs	see <a href="#">Figure 4</a>
Power-on time <sup>1)4)</sup>	$t_{PON}$		50	100	µs	$V_{DD} = 3\text{ V}$ , $B \leq B_{RP} - 0.5\text{ mT}$ or $B \geq B_{OP} + 0.5\text{ mT}$
Chopper frequency <sup>1)</sup>	$f_{OSC}$		350		kHz	

1) Not subject to production test, verified by design/characterization.

2) Output jitter is the 1σ value of the output switching distribution.

**Specification**

- 3) Systematic delay between magnetic threshold reached and output switching.
- 4) Time from applying  $V_{DD} = 3.0\text{ V}$  to the sensor until the output is valid.

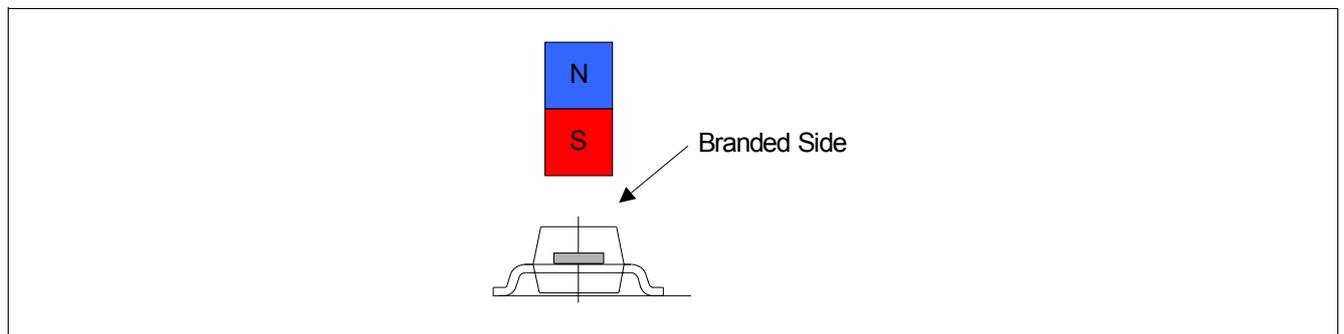
**Table 7 Magnetic Characteristics**

Parameter	Symbol	T (°C)	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Operating point	B <sub>OP</sub>	-40	0.6	2.2	3.7	mT	
		25	0.5	2.0	3.5		
		125	0.3	1.7	3.1		
Release point	B <sub>RP</sub>	-40	-3.7	-2.2	-0.6	mT	
		25	-3.5	-2.0	-0.5		
		125	-3.1	-1.7	-0.3		
Hysteresis	B <sub>HYS</sub>	-40	2.8	4.4	5.7	mT	
		25	2.6	4.0	5.4		
		125	2.2	3.4	4.6		
Effective noise value of the magnetic switching points <sup>1)2)</sup>	B <sub>Neff</sub>	25		39		μT	
Temperature compensation of magnetic thresholds <sup>2)</sup>	T <sub>C</sub>			-1500		ppm/K	

- 1) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents the rms-value and corresponds therefore to a 1  $\sigma$  probability of normal distribution. Consequently a 3  $\sigma$  value corresponds to 0.3% probability of appearance.
- 2) Not subject to production test, verified by design/characterization.

**Field Direction Definition**

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.



**Figure 8 Definition of Magnetic Field Direction PG-SOT23-3-15**

Package Information

### 4 Package Information

The TLI4963-1M is available in the small halogen free SMD package PG-SOT23-3-15.

#### 4.1 Package Outline PG-SOT23-3-15

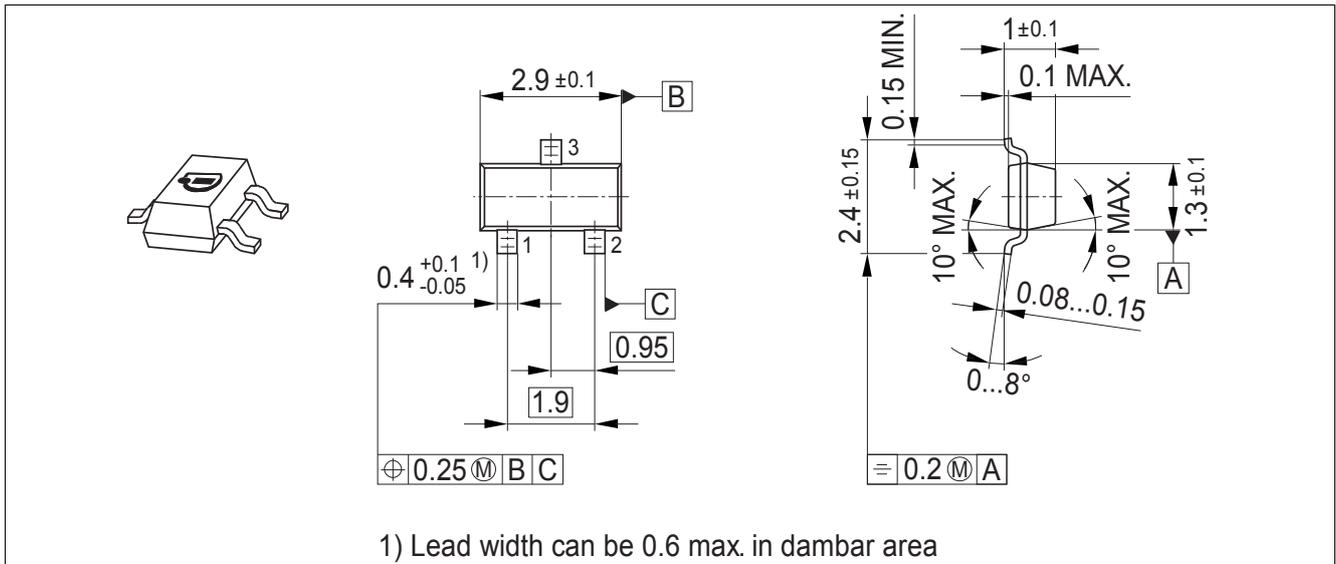


Figure 9 PG-SOT23-3-15 Package Outline (All Dimensions in mm)

#### 4.2 Footprint PG-SC59-3-5 and PG-SOT23-3-15

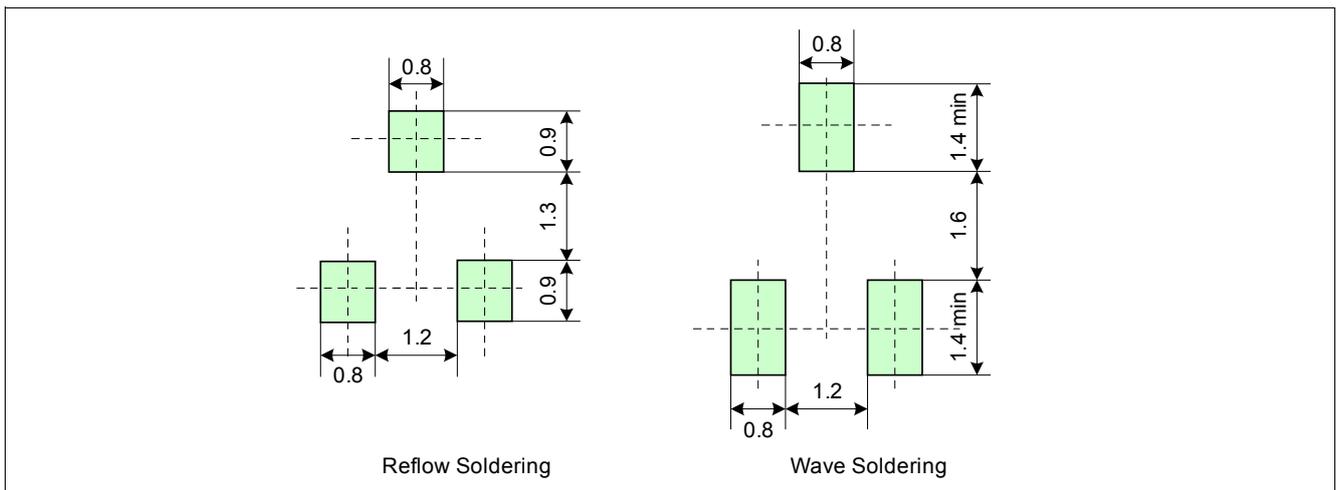


Figure 10 Footprint PG-SC59-3-5 and PG-SOT23-3-15

Package Information

4.3 Packing Information PG-SOT23-3-15

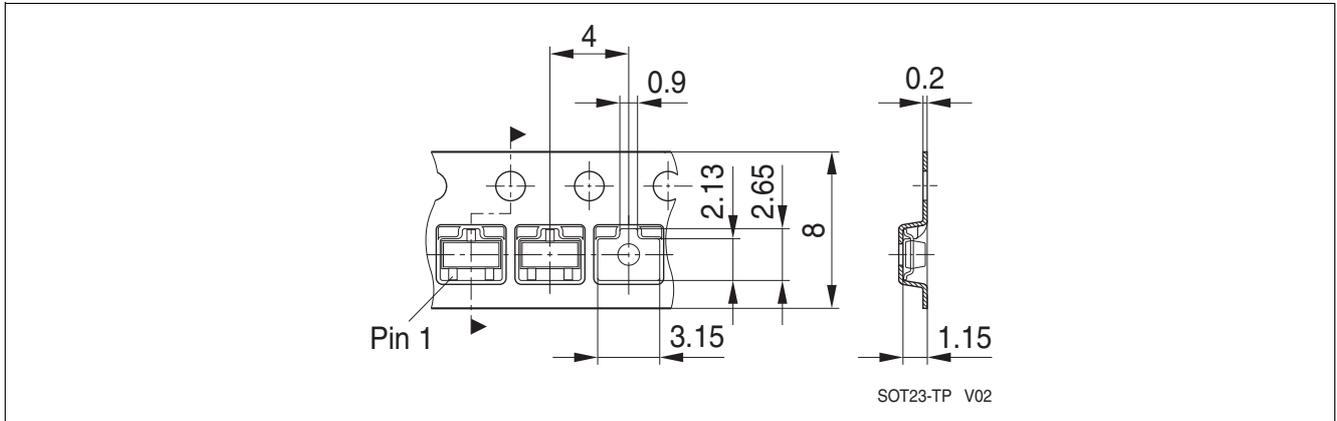


Figure 11 Packing of the PG-SOT23-3-15 in a Tape

4.4 PG-SOT23-3-15 Distance between Chip and Package

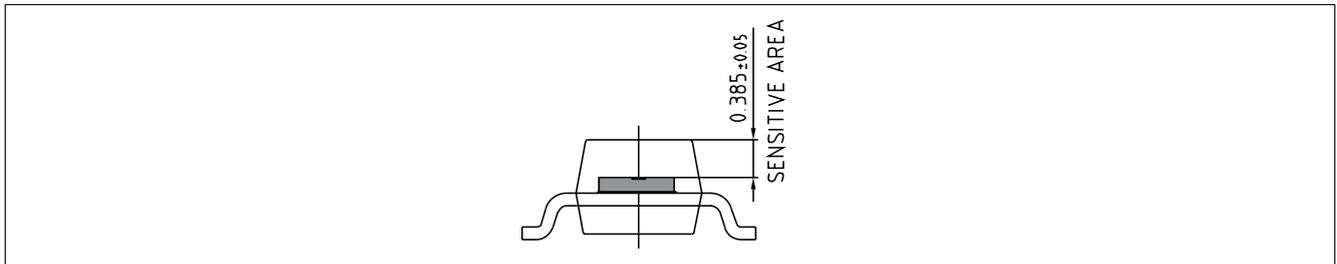


Figure 12 Distance between Chip and Package

4.5 Package Marking

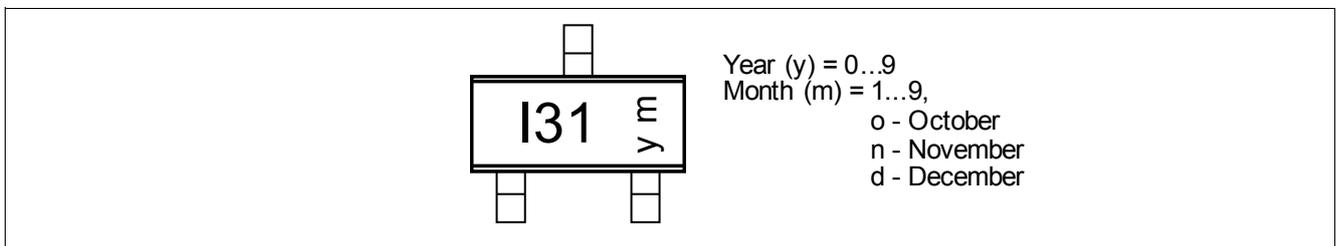


Figure 13 Marking of TLI4963-1M

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**Revision History****5 Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.0	2016-01-11	Initial release.

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