DATA SHEET

74F283
4-bit binary full adder with fast carry

Product specification

1989 Mar 03

IC15 Data Handbook

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4-bit binary full adder with fast carry

74F283

FEATURES

- High speed 4-bit addition
- Cascadable in 4-bit increments
- Fast Internal carry look-ahead

DESCRIPTION

The 74F283 adds two 4-bit binary words (An plus Bn) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma 0$–$\Sigma 3$) and the outgoing carry (C_{OUT}) according to the equation:

$C_{IN}+2^0(A0+B0)+2^1(A1+B1)+2^2(A2+B2)+2^3(A3+B3)$
$=\Sigma 0+2\Sigma 1+4\Sigma 2+8\Sigma 3+16C_{OUT}$

where (+)=plus

Due to the symmetry of the binary add function, the 74F283 can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). See Function Table. In case of all active-Low operands (negative logic) the results $\Sigma 1$–$\Sigma 4$ and C_{OUT} should be interpreted also as active-Low. With active-High inputs, C_{IN} cannot be left open; it must be held Low when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus A0, B0, C_{IN} can arbitrarily be assigned to pins 5, 6, 7, etc.

Due to pin limitations, the intermediate carries of the 74F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage.

PIN CONFIGURATION
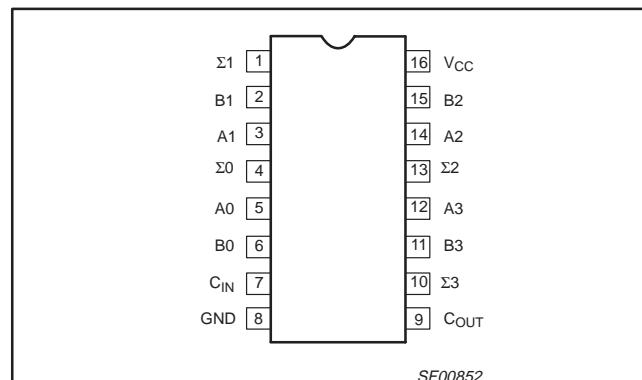
SF00852

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F283	6.5ns	40mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V $\pm$10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F283N	SOT38-4
16-pin plastic SO	N74F283D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A3	A operand inputs	1.0/2.0	20μA/1.2mA
B0 - B3	B operand inputs	1.0/2.0	20μA/1.2mA
C_{IN}	Carry input	1.0/1.0	20μA/0.6mA
C_{OUT}	Carry output	50/33	1.0mA/20mA
$\Sigma 0$–$\Sigma 3$	Sum outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL

V_{CC}=Pin 16
GND=Pin 8

SF00853
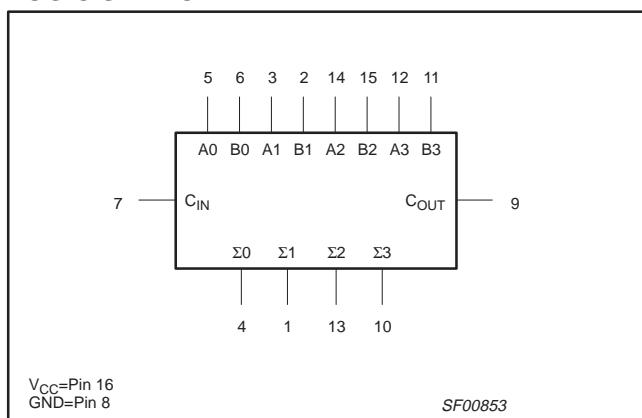
LOGIC SYMBOL (IEEE/IEC)

SF00854
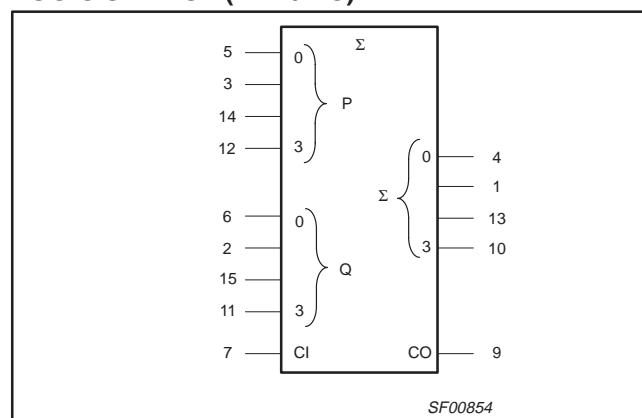
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LOGIC DIAGRAM

V_CC=Pin 16
GND=Pin 8

SF00855
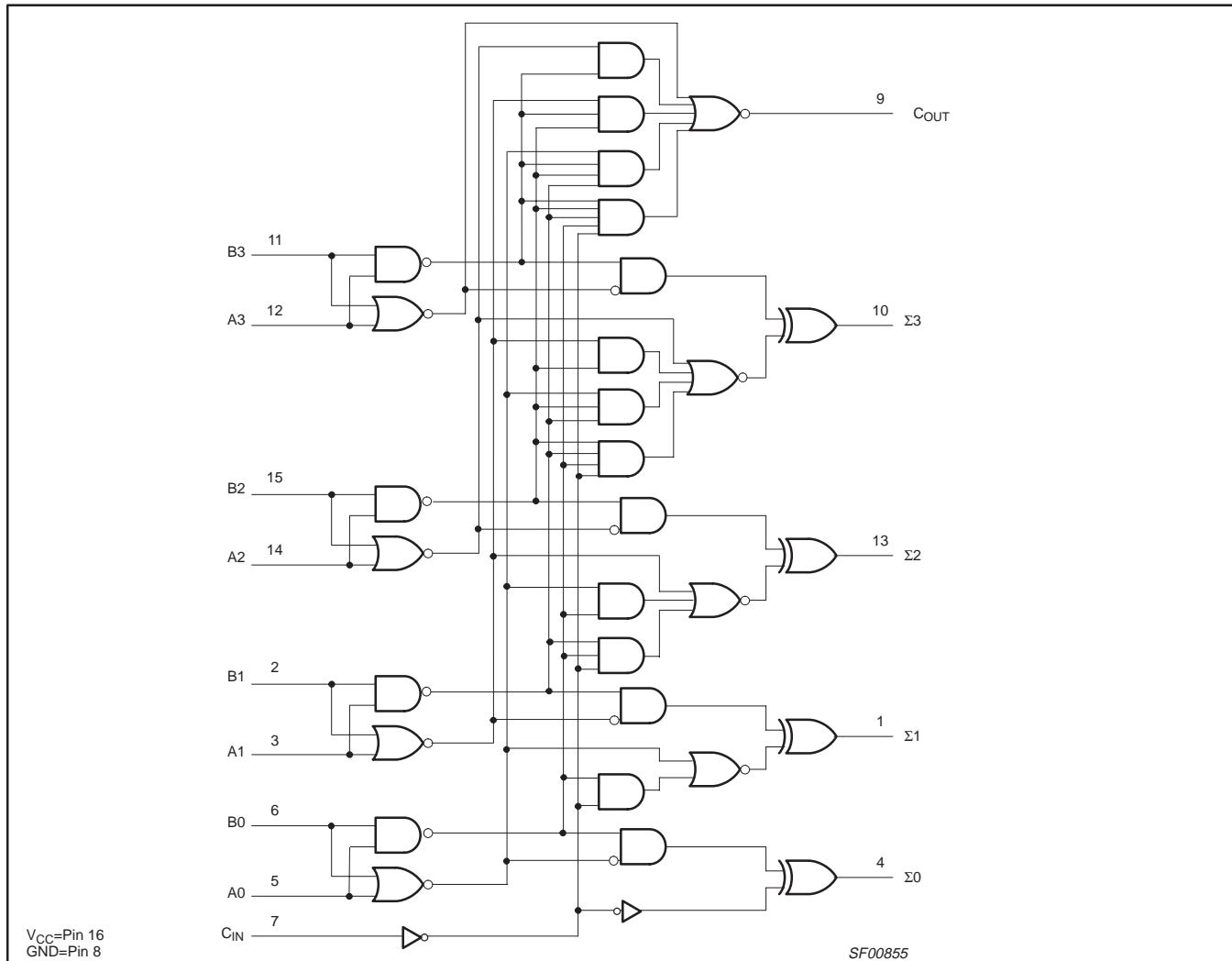
FUNCTION TABLE

PINS	C_{IN}	A0	A1	A2	A3	B0	B1	B2	B3	$\Sigma 0$	$\Sigma 1$	$\Sigma 2$	$\Sigma 3$	C_{OUT}	Example:
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	1001
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1	1010
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0	$\overline{10011}$

Example:
1001
1010
$\overline{10011}$
(10+9=19)
(carry+5+6=12)

H = High voltage level
L = Low voltage level

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Figure A shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A3, B3) Low makes $\Sigma 3$ dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure B shows a way of dividing the 74F283 into a 2-bit and a 1-bit adder. The third stage adder (A2, B2, $\Sigma 2$) is used as means of getting a carry (C10) signal into the fourth stage adder (via A2 and B2) and bringing out the carry from the second stage on $\Sigma 2$. Note that as long as A2 and B2 are the same, whether High or Low,

they do not influence $\Sigma 2$. Similarly, when A2 and B2 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure C shows a method of implementing a 5-input encoder where the inputs are equally weighted. The outputs $\Sigma 0$, $\Sigma 1$ and $\Sigma 2$ present a binary number of inputs I0–I4 that are true. Figure D shows one method of implementing a 5-input majority gate. When three or more of the inputs I0–I4 are true, the output M4 is true.

APPLICATIONS
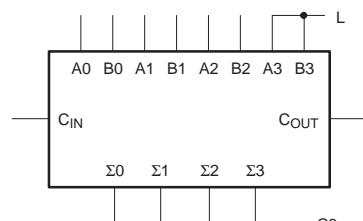
A. 3-bit Adder
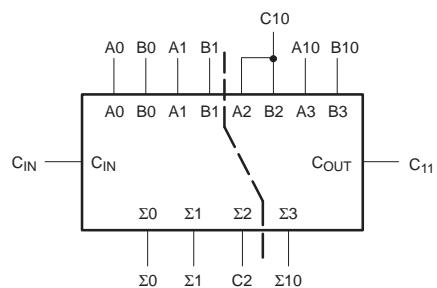
B. 2-bit and 1-bit Adder
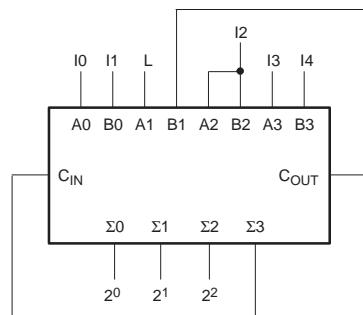
C. 5-input Encoder
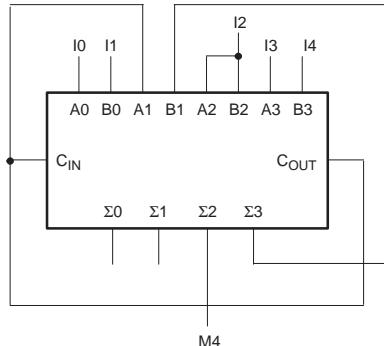
D. 5-input Majority Gate

SF00856

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[NO TAG]		LIMITS			UNIT
				MIN	TYP[NO TAG]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_{IN} only	V_{CC} = MAX, V_I = 0.5V			−0.6	mA
		An, Bn				−1.2	mA
I_{OS}	Short-circuit output current[NO TAG]	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			40	55	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} should be measured with all outputs open and the following conditions:
    Condition1: all inputs grounded
    Condition 2: all B inputs Low, other inputs at 4.5V
    Condition 3: all inputs at 4.5V

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σi	Waveform 1, 2	3.5 4.0	7.0 7.0	9.5 9.5	3.0 3.5	10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Ai or Bi to Σi	Waveform 1, 2	3.5 3.5	7.0 7.0	9.5 9.5	2.5 3.5	10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 2.5	8.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Ai or Bi to C_{OUT}	Waveform 1, 2	3.5 2.5	5.7 5.3	7.5 7.0	3.0 2.5	8.5 8.0	ns ns

AC WAVEFORMS

For all waveforms, V_M=1.5V.
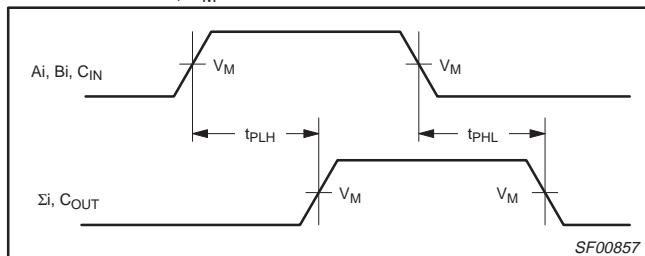
**Waveform 1.   Propagation Delay
Operands and Carry Inputs to Outputs**
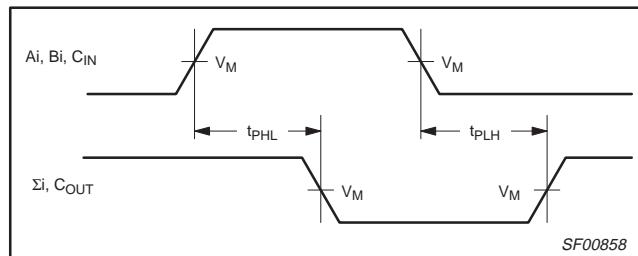
**Waveform 2.   Propagation Delay
Operands and Carry Inputs to Outputs**

TEST CIRCUIT AND WAVEFORM

Test Circuit for Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS:
R_L = Load resistor;
    see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance;
    see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of
    pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

4-bit binary full adder with fast carry

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## DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4
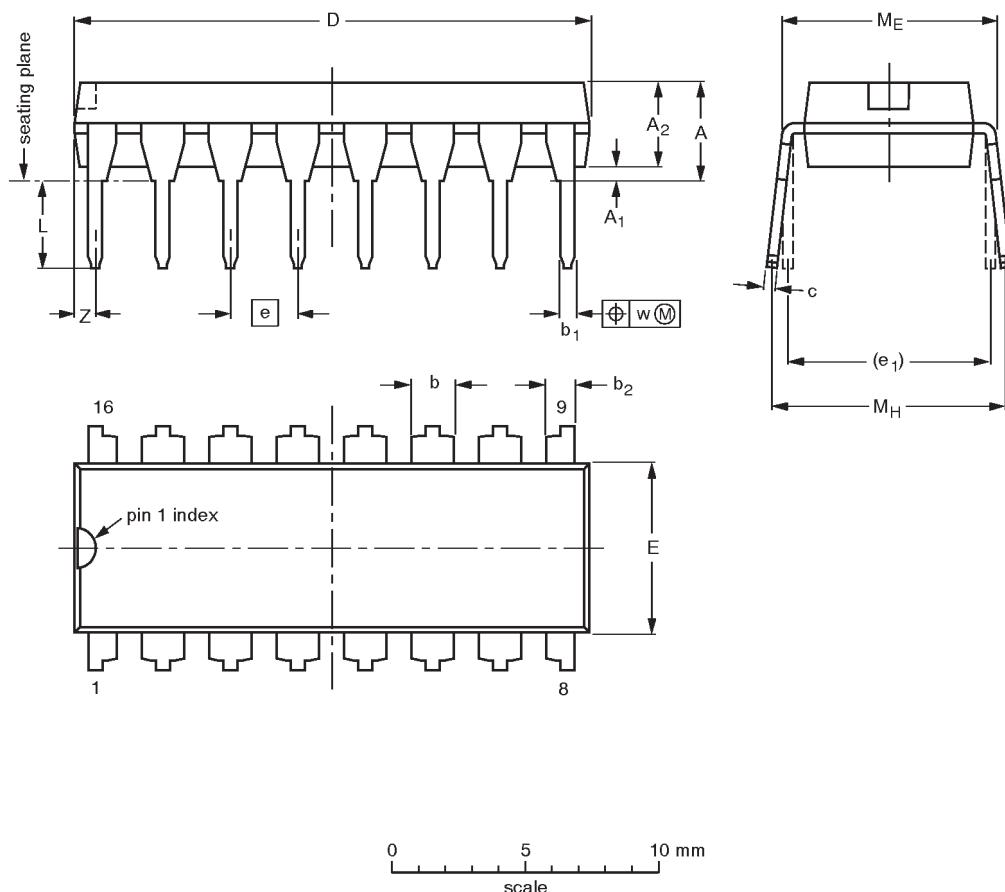
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	b₂	c	D [1]	E [1]	e	e₁	L	M_E	M_H	w	Z [1] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

4-bit binary full adder with fast carry

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1
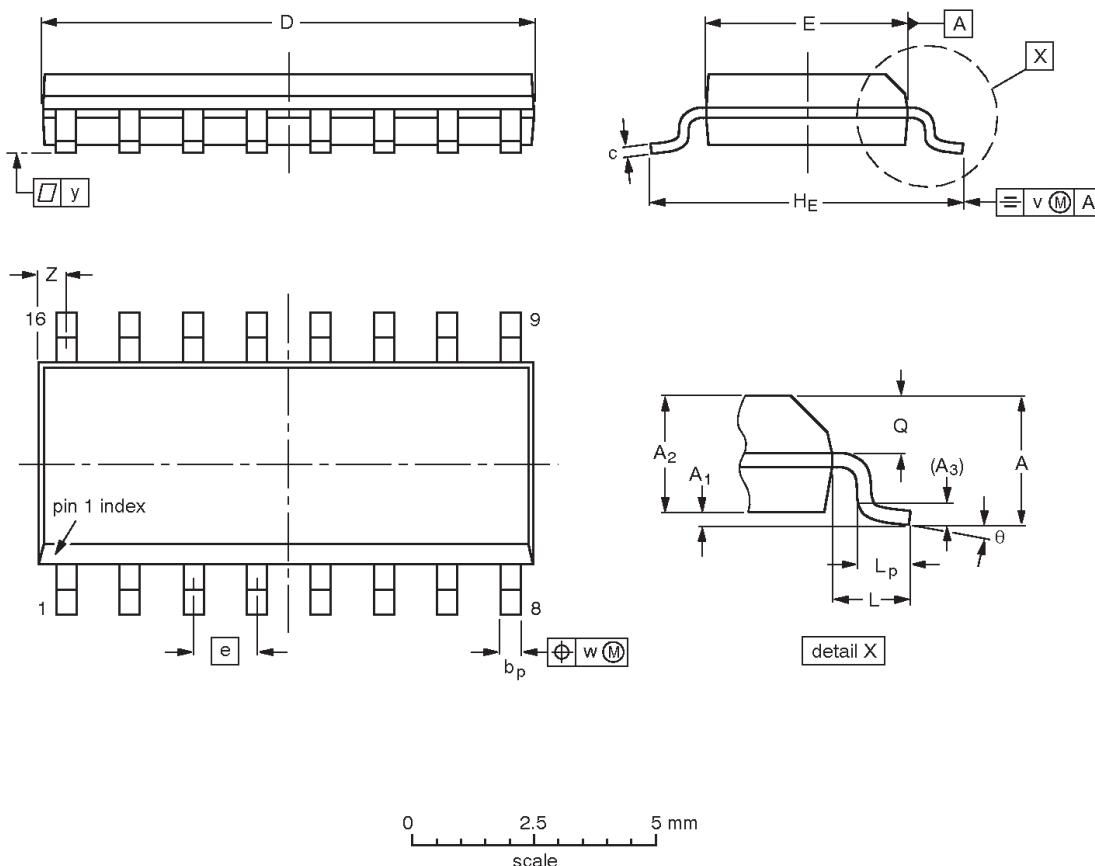
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

NOTES

4-bit binary full adder with fast carry

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1]   Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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