

IRFS3107PbF IRFSL3107PbF

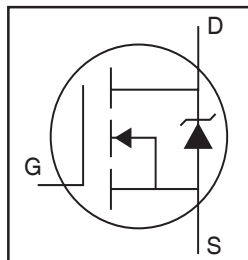
HEXFET® Power MOSFET

Applications

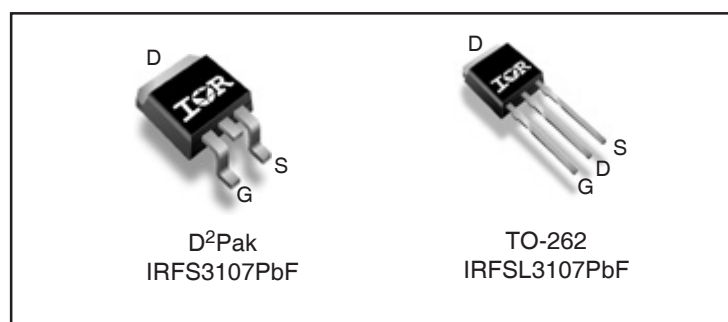
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



V_{DSS}	75V
$R_{DS(on)}$ typ.	2.5mΩ
max.	3.0mΩ
I_D (Silicon Limited)	230A ①
I_D (Package Limited)	195A



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	230①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	160	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	195	
I_{DM}	Pulsed Drain Current ②	900	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	14	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	300	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧⑨	—	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧⑨	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.09	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5mA$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.5	3.0	m Ω	$V_{GS} = 10V, I_D = 140A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 75V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	1.2	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

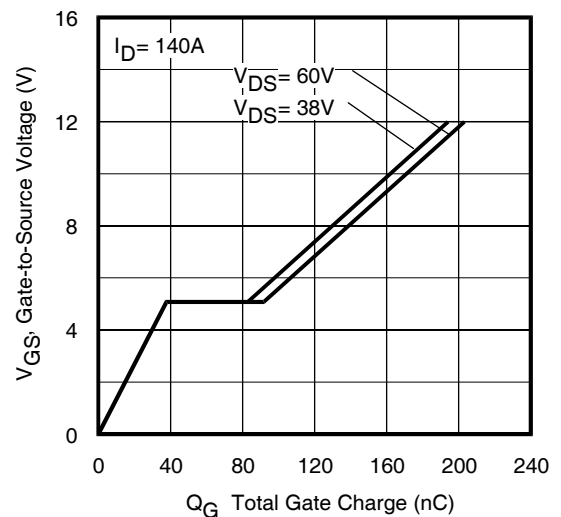
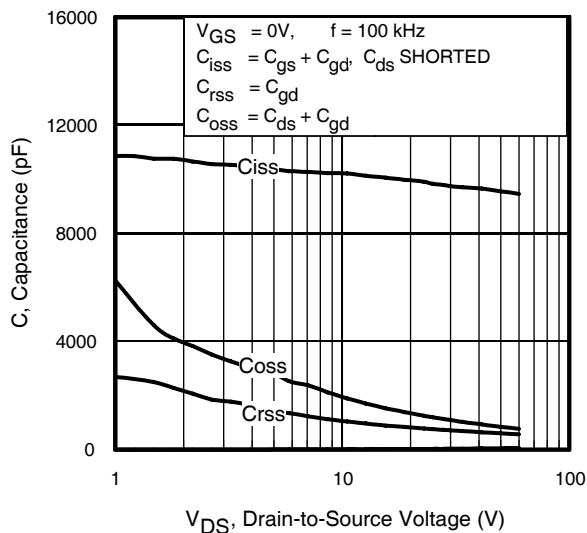
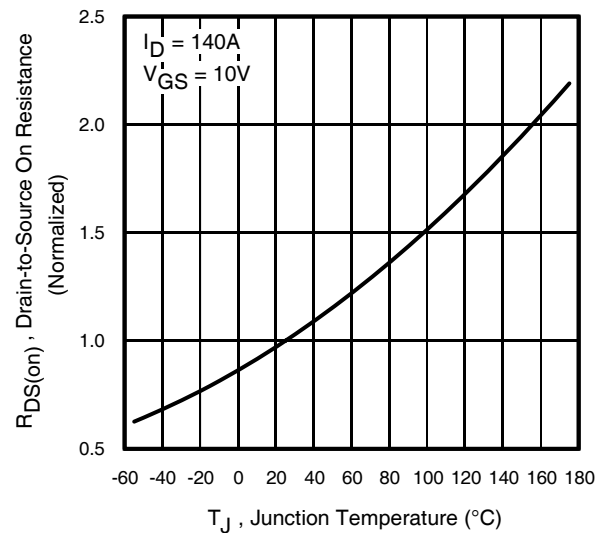
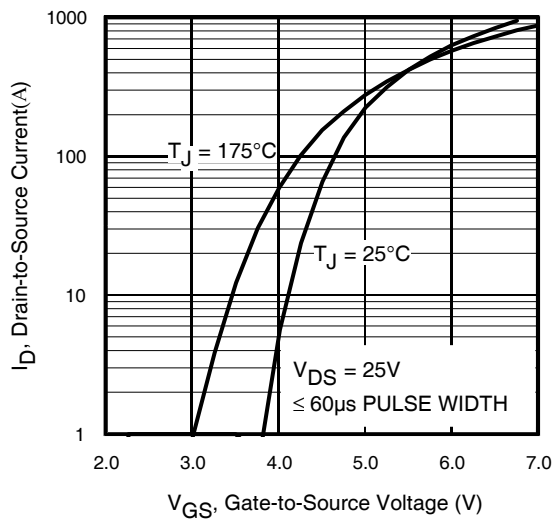
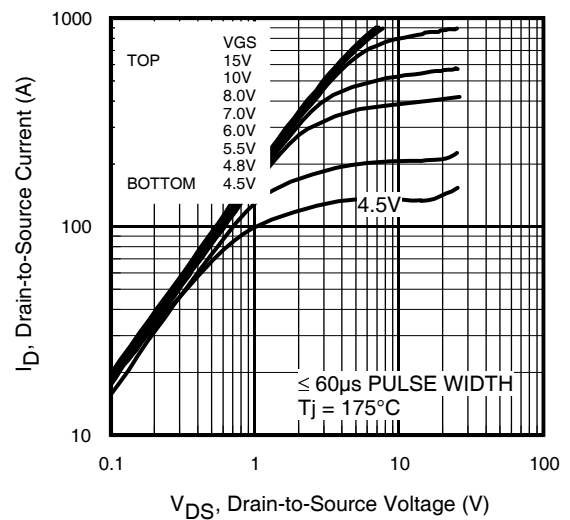
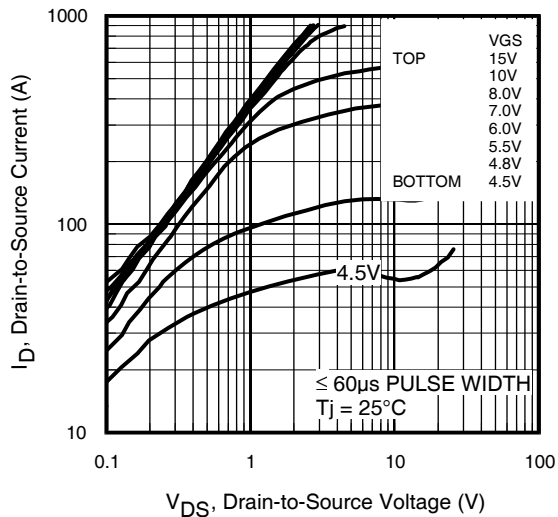
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	230	—	—	S	$V_{DS} = 50V, I_D = 140A$
Q_g	Total Gate Charge	—	160	240	nC	$I_D = 140A$
Q_{gs}	Gate-to-Source Charge	—	38	—		$V_{DS} = 38V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	54	—		$V_{GS} = 10V$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	106	—		$I_D = 140A, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	19	—	ns	$V_{DD} = 49V$
t_r	Rise Time	—	110	—		$I_D = 140A$
$t_{d(off)}$	Turn-Off Delay Time	—	99	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	100	—		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	9370	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	840	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	580	—		$f = 1.0\text{ MHz}$, See Fig. 5
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	1130	—		$V_{GS} = 0V, V_{DS} = 0V$ to $60V$ ⑦, See Fig. 11
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑥	—	1500	—		$V_{GS} = 0V, V_{DS} = 0V$ to $60V$ ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	230①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	900	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 140A, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	54	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 64V$,
		—	60	—		$T_J = 125^\circ\text{C}$ $I_F = 140A$
Q_{rr}	Reverse Recovery Charge	—	103	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	132	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	3.6	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.045mH$
 $R_G = 25\Omega$, $I_{AS} = 140A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 140A$, $di/dt \leq 1380A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss\text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to $80\% V_{DSS}$.
- ⑦ $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to $80\% V_{DSS}$.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C
- ⑩ $R_{\theta JC}$ value shown is at time zero.



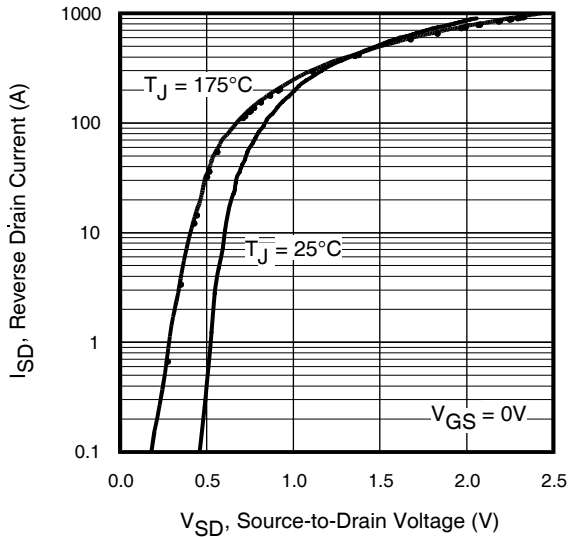


Fig 7. Typical Source-Drain Diode Forward Voltage

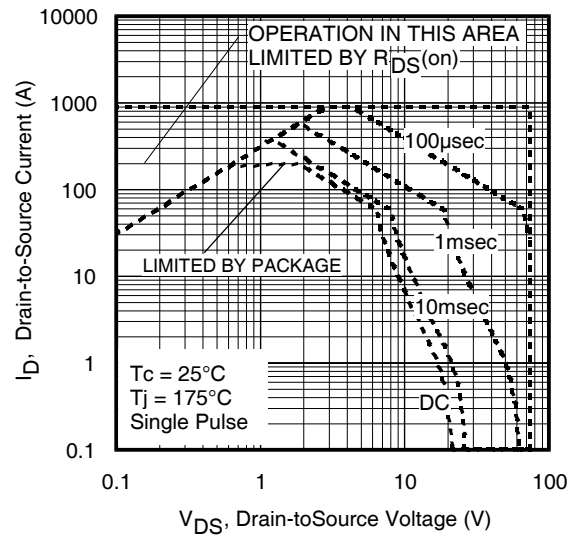


Fig 8. Maximum Safe Operating Area

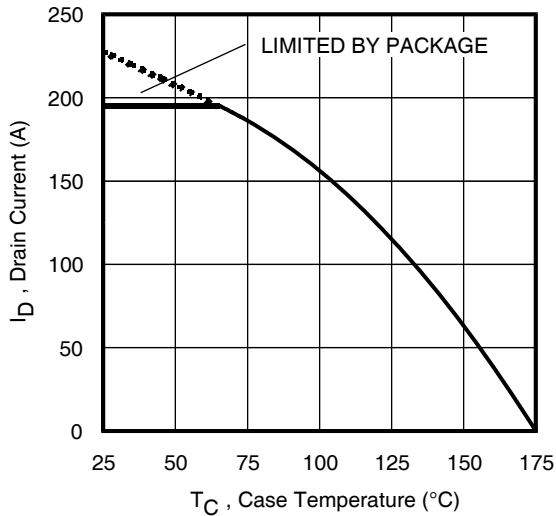


Fig 9. Maximum Drain Current vs. Case Temperature

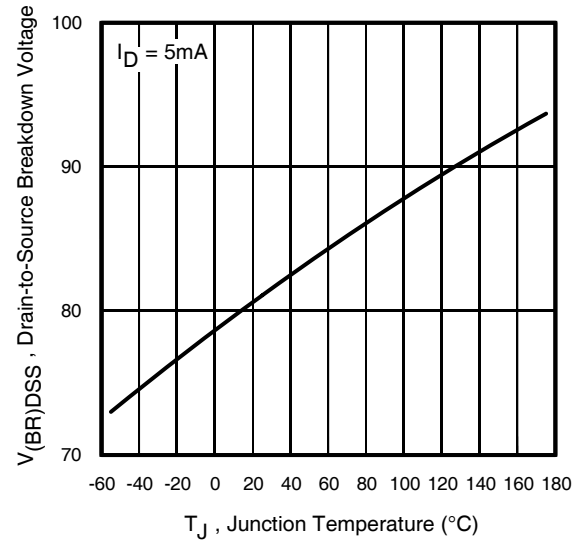


Fig 10. Drain-to-Source Breakdown Voltage

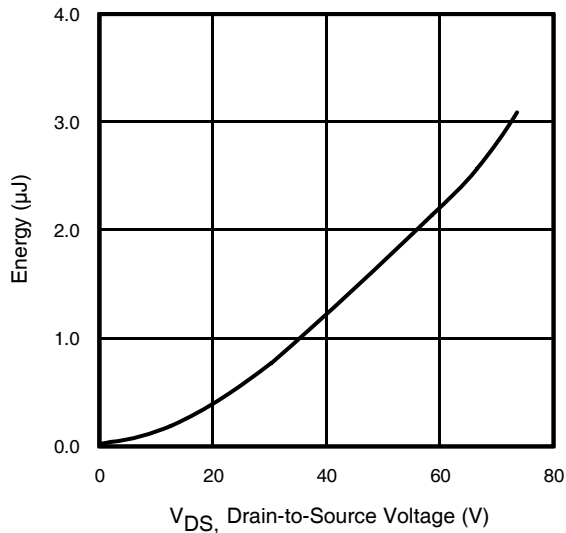


Fig 11. Typical C_{OSS} Stored Energy

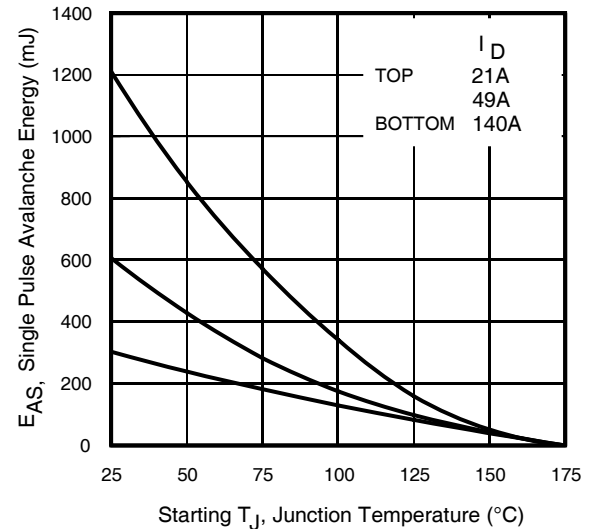


Fig 12. Maximum Avalanche Energy Vs. Drain Current
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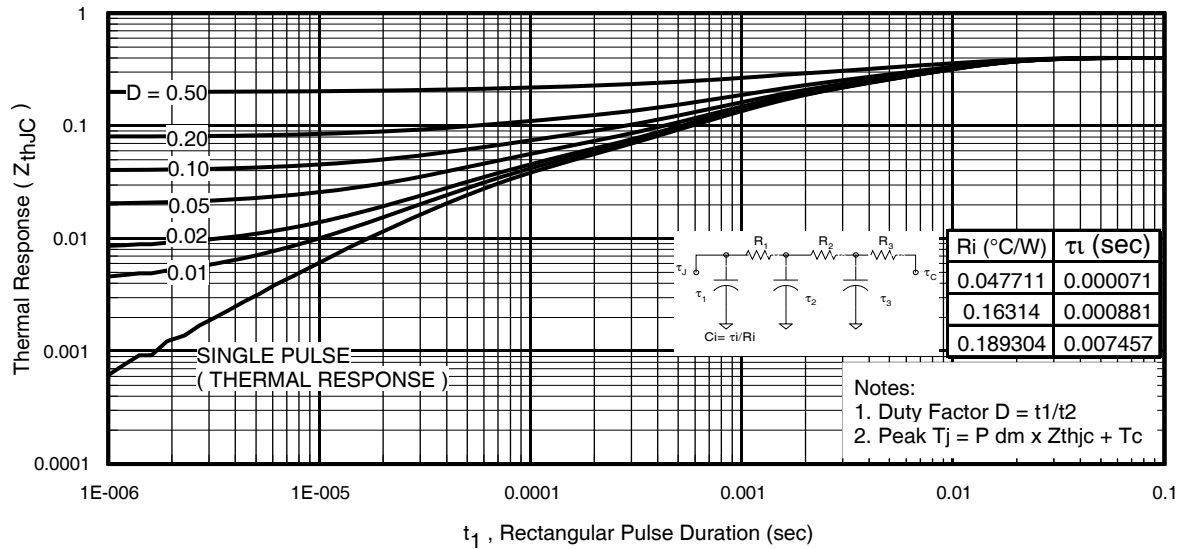


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

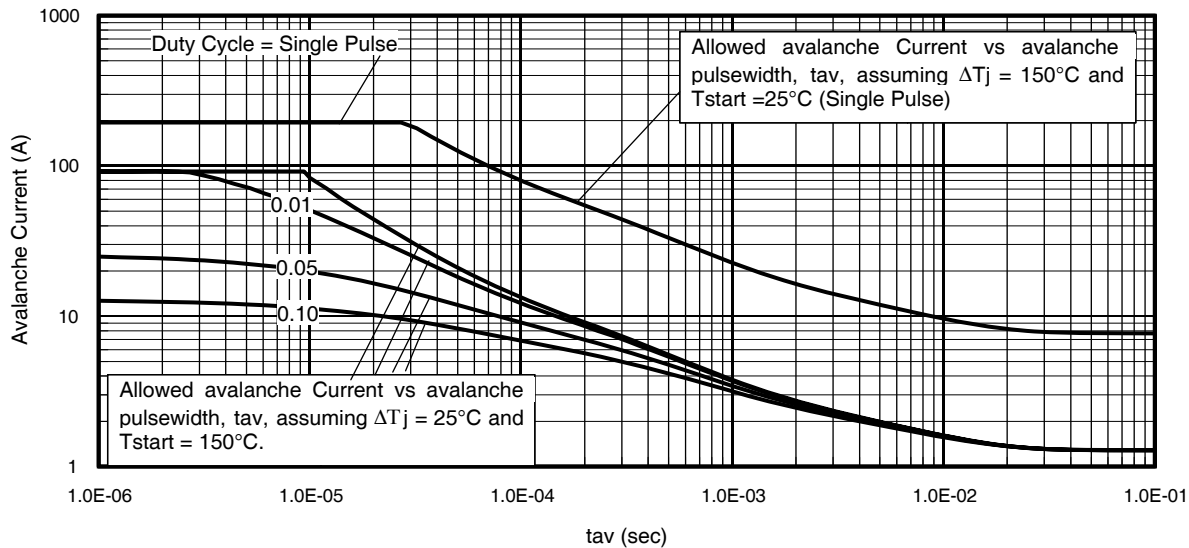
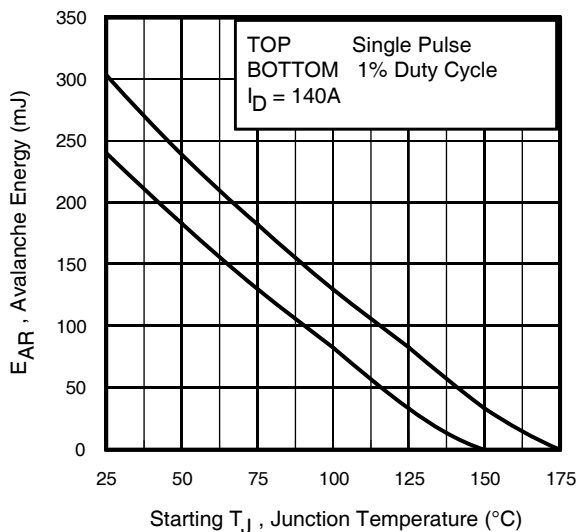


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

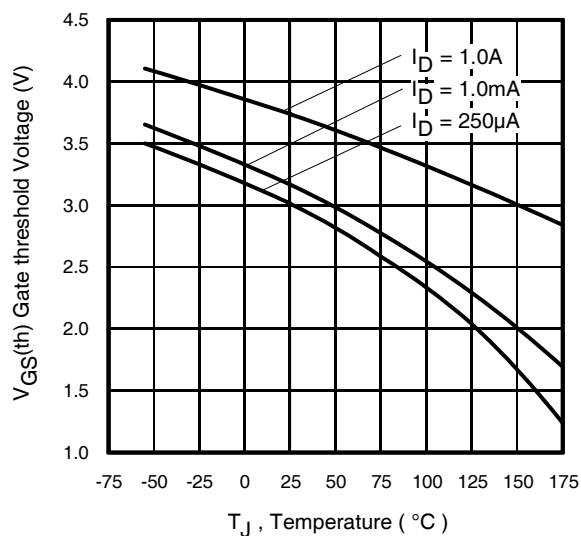
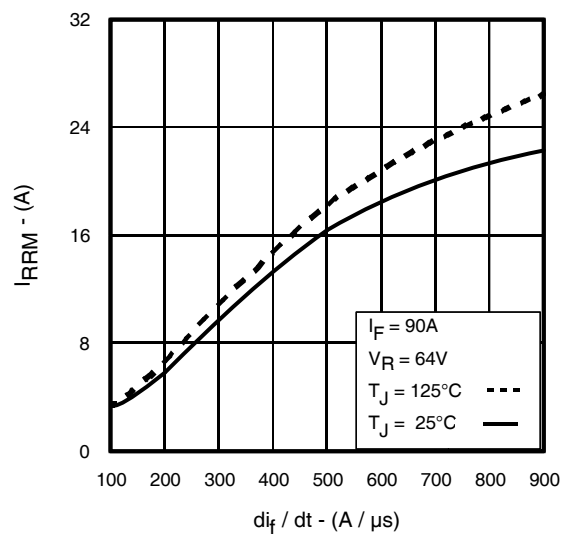
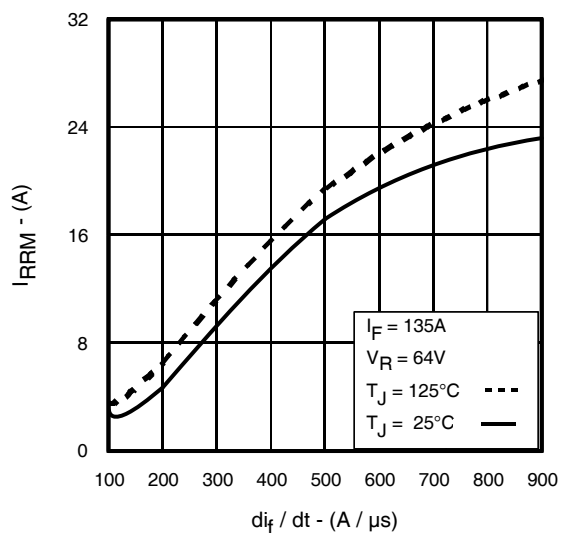
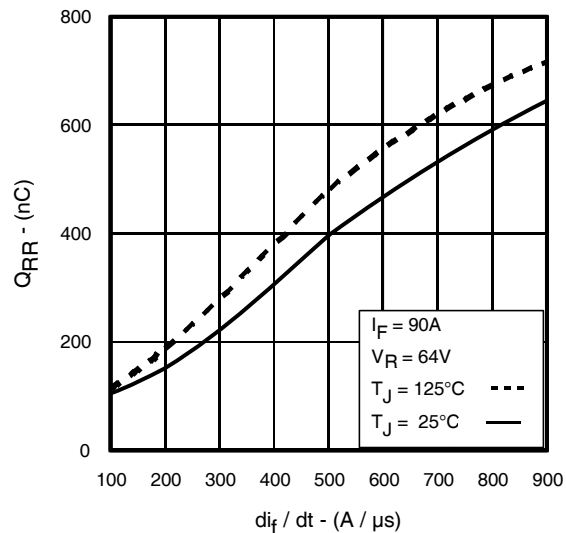
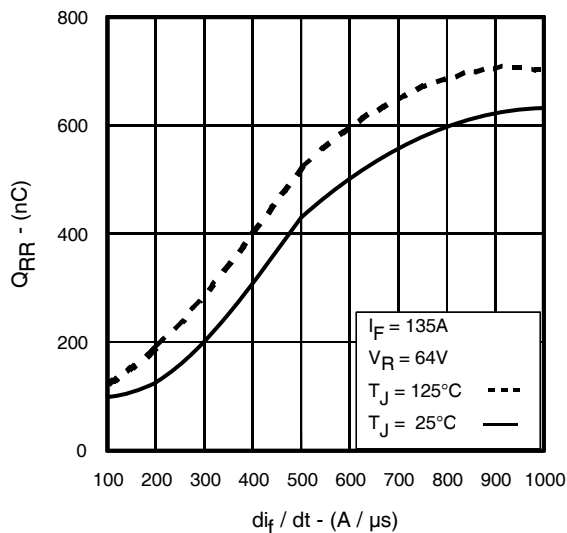
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

**Fig. 16.** Threshold Voltage Vs. Temperature**Fig. 17 -** Typical Recovery Current vs. di_f/dt **Fig. 18 -** Typical Recovery Current vs. di_f/dt **Fig. 19 -** Typical Stored Charge vs. di_f/dt **Fig. 20 -** Typical Stored Charge vs. di_f/dt

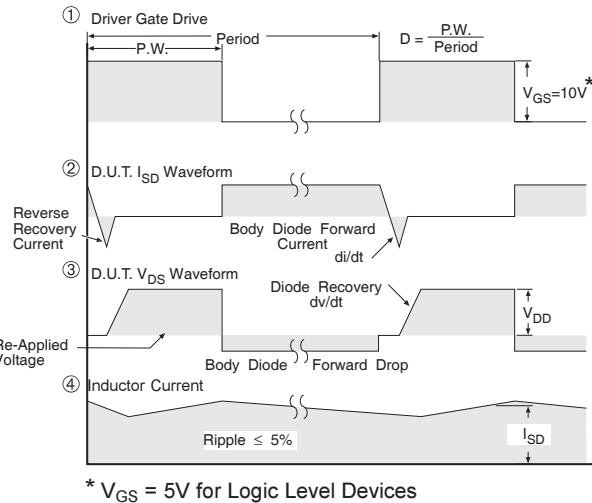
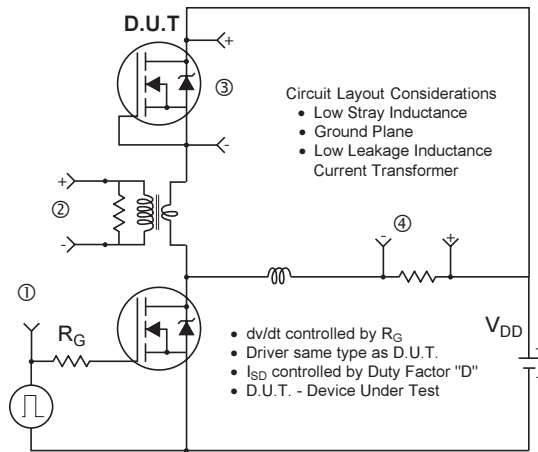


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

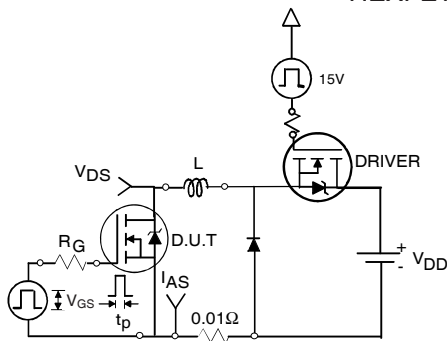


Fig 22a. Unclamped Inductive Test Circuit

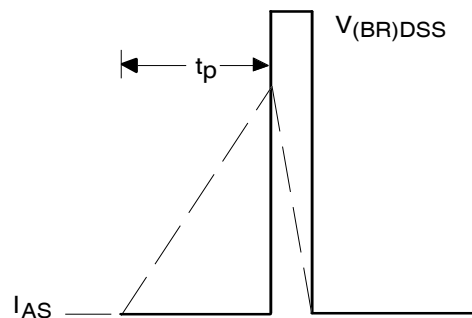


Fig 22b. Unclamped Inductive Waveforms

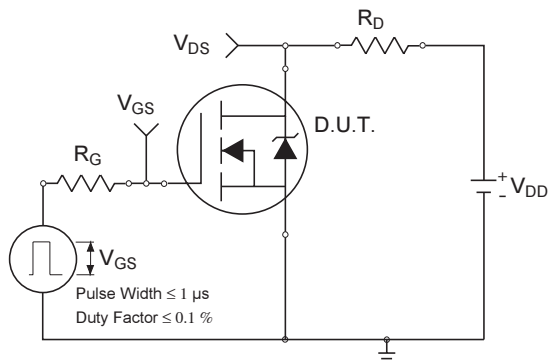


Fig 23a. Switching Time Test Circuit



Fig 23b. Switching Time Waveforms

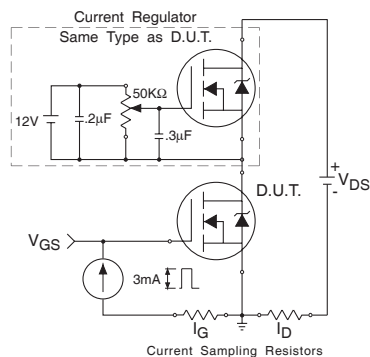


Fig 24a. Gate Charge Test Circuit

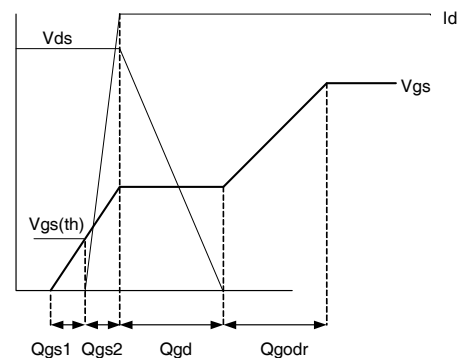
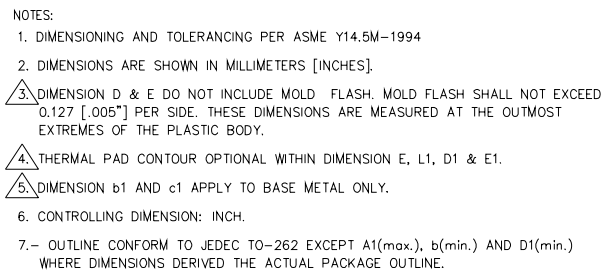


Fig 24b. Gate Charge Waveform

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	
E	9.65	10.67	.380	.420	3, 4
E1	6.22	—	.245	—	
e	BSC		BSC		4
L	13.46	14.10	.530	.555	
L1	1.65		.065		
L2	3.56	3.71	.140	.146	

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE

IRL3103L

TOR P719A

17 89

PART NUMBER

DATE CODE

P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)

YEAR 7 = 1997

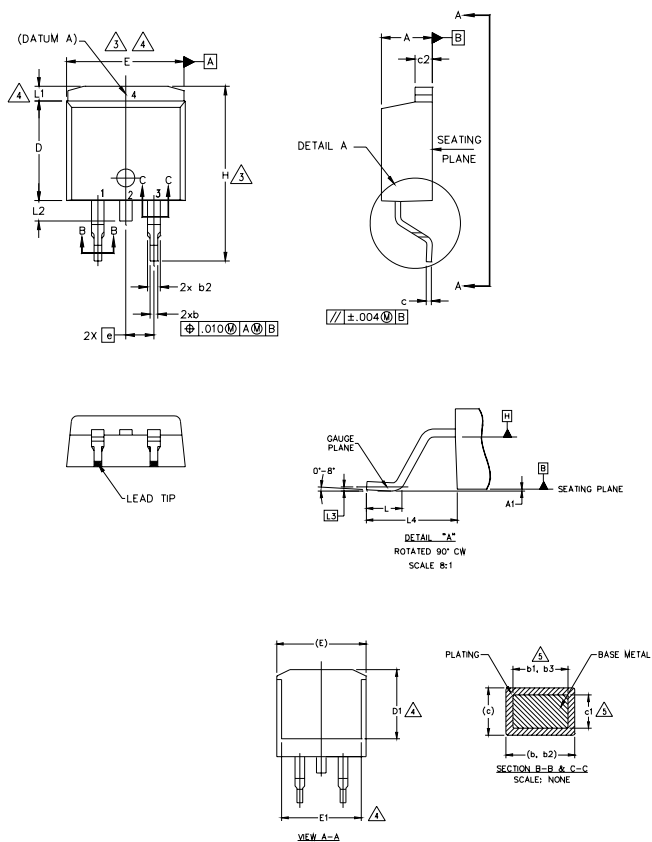
WEEK 19

A = ASSEMBLY SITE CODE

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D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b1	0.51	0.99	.020	.039	
b2	0.51	0.89	.020	.035	
b3	1.14	1.78	.045	.070	
c	1.14	1.73	.045	.068	5
c1	0.38	0.74	.015	.029	5
c2	0.38	0.58	.015	.023	
D	1.14	1.65	.045	.065	
D2	8.38	9.65	.330	.380	3
D1	6.86	—	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	4
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	
L2	1.27	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

1. - GATE
- 2, 4. - COLLECTOR
3. - EMITTER

DIODES

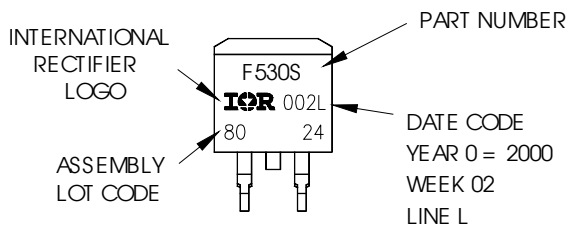
- 1.- ANODE *
- 2, 4.- CATHODE
- 3.- ANODE

* PART DEPENDENT.

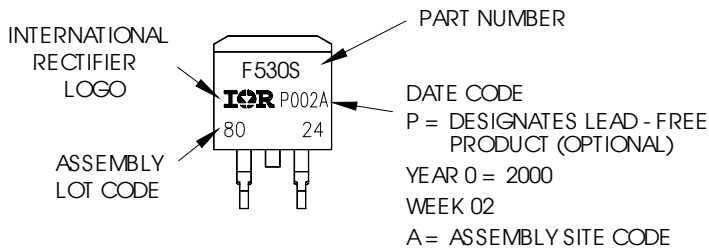
D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"



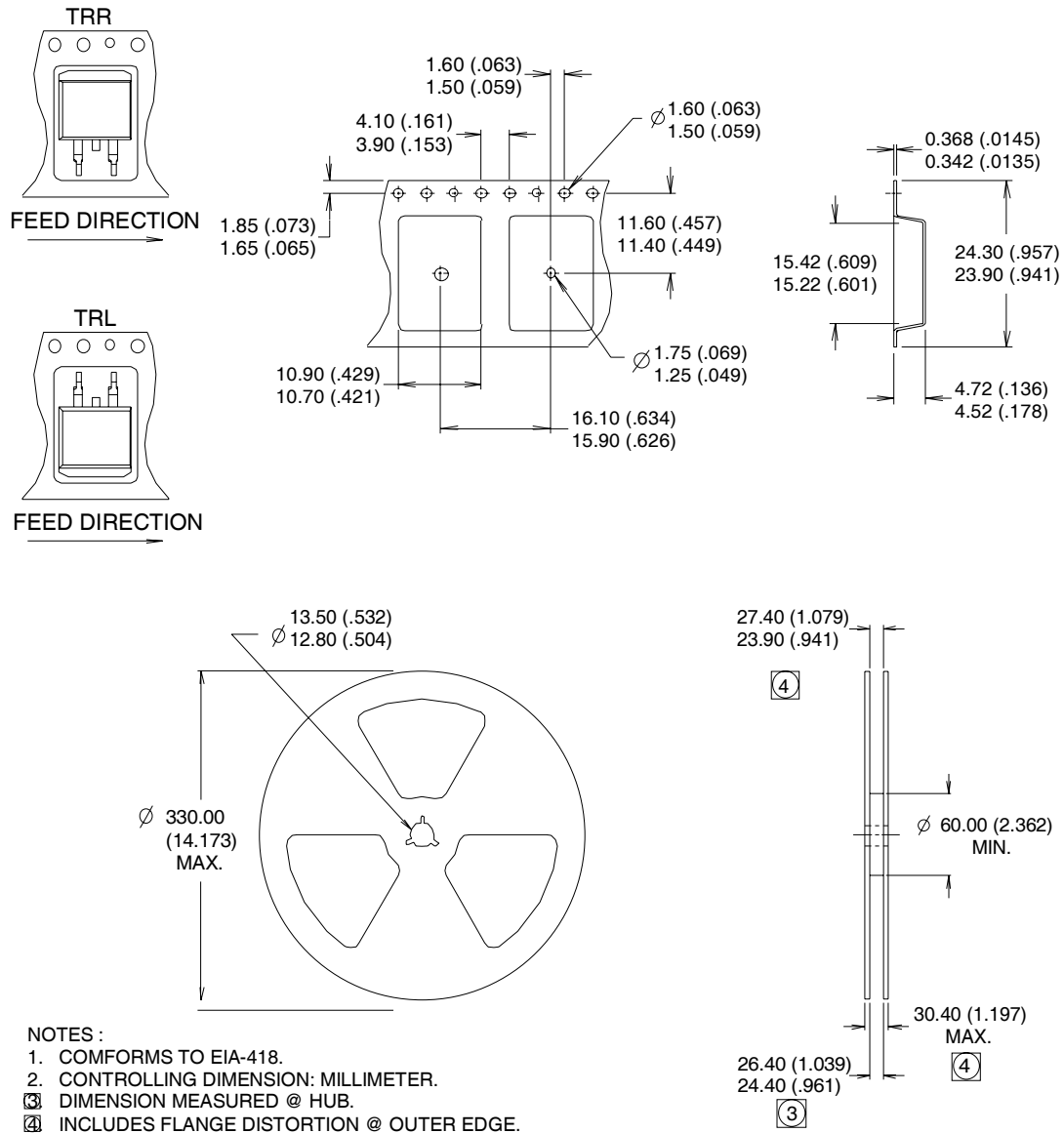
OR



Note: For the most current drawing please refer to IRF website at <http://www.irf.com/package/www.irf.com>

D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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TAC Fax: (310) 252-7903

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