

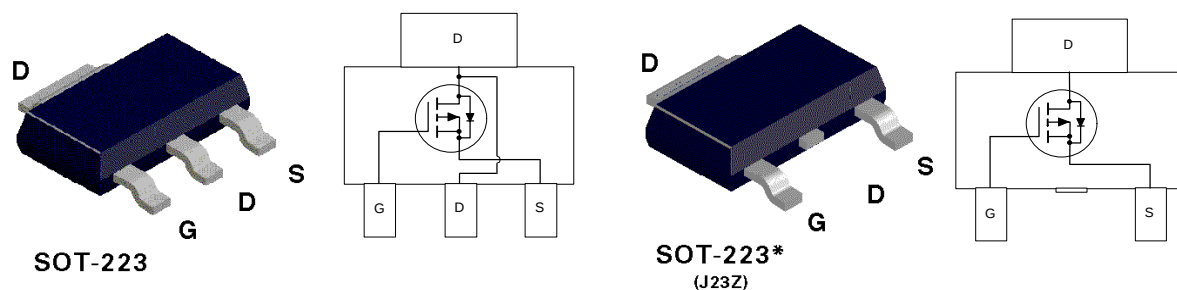
## NDT456P P-Channel Enhancement Mode Field Effect Transistor

### General Description

Power SOT P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management, battery powered circuits, and DC motor control.

### Features

- -7.5 A, -30 V.  $R_{DS(ON)} = 0.030 \Omega$  @  $V_{GS} = -10$  V  
 $R_{DS(ON)} = 0.045 \Omega$  @  $V_{GS} = -4.5$  V.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol         | Parameter                               | NDT456P    | Units            |
|----------------|-----------------------------------------|------------|------------------|
| $V_{DSS}$      | Drain-Source Voltage                    | -30        | V                |
| $V_{GSS}$      | Gate-Source Voltage                     | $\pm 20$   | V                |
| $I_D$          | Drain Current - Continuous (Note 1a)    | $\pm 7.5$  | A                |
|                | - Pulsed                                | $\pm 20$   |                  |
| $P_D$          | Maximum Power Dissipation (Note 1a)     | 3          | W                |
|                | (Note 1b)                               | 1.3        |                  |
|                | (Note 1c)                               | 1.1        |                  |
| $T_J, T_{STG}$ | Operating and Storage Temperature Range | -65 to 150 | $^\circ\text{C}$ |

### THERMAL CHARACTERISTICS

|                 |                                                   |    |                    |
|-----------------|---------------------------------------------------|----|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 42 | $^\circ\text{C/W}$ |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Note 1)     | 12 | $^\circ\text{C/W}$ |

# Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

| Symbol                             | Parameter                         | Conditions                                                                                           | Min  | Typ   | Max   | Units |
|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------|------|-------|-------|-------|
| OFF CHARACTERISTICS                |                                   |                                                                                                      |      |       |       |       |
| BV <sub>DSS</sub>                  | Drain-Source Breakdown Voltage    | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA                                                       | -30  |       |       | V     |
| I <sub>DSS</sub>                   | Zero Gate Voltage Drain Current   | V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V                                                       |      |       | -1    | μA    |
|                                    |                                   | T <sub>J</sub> = 55°C                                                                                |      |       | -10   | μA    |
| I <sub>GSSF</sub>                  | Gate - Body Leakage, Forward      | V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V                                                        |      |       | 100   | nA    |
| I <sub>GSSR</sub>                  | Gate - Body Leakage, Reverse      | V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V                                                       |      |       | -100  | nA    |
| ON CHARACTERISTICS (Note 2)        |                                   |                                                                                                      |      |       |       |       |
| V <sub>GS(th)</sub>                | Gate Threshold Voltage            | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA                                        | -1   | -1.5  | -3    | V     |
|                                    |                                   | T <sub>J</sub> = 125°C                                                                               | -0.5 | -1.1  | -2.6  |       |
| R <sub>DS(on)</sub>                | Static Drain-Source On-Resistance | V <sub>GS</sub> = -10 V, I <sub>D</sub> = -7.5 A                                                     |      | 0.026 | 0.03  | Ω     |
|                                    |                                   | T <sub>J</sub> = 125°C                                                                               |      | 0.035 | 0.054 |       |
|                                    |                                   | V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6 A                                                      |      | 0.041 | 0.045 |       |
| I <sub>D(on)</sub>                 | On-State Drain Current            | V <sub>GS</sub> = -10 V, V <sub>DS</sub> = -5 V                                                      | -20  |       |       | A     |
|                                    |                                   | V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -5 V                                                     | -10  |       |       |       |
| G <sub>fs</sub>                    | Forward Transconductance          | V <sub>GS</sub> = -10 V, I <sub>D</sub> = -7.5 A                                                     |      | 13    |       | S     |
| DYNAMIC CHARACTERISTICS            |                                   |                                                                                                      |      |       |       |       |
| C <sub>iss</sub>                   | Input Capacitance                 | V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V,<br>f = 1.0 MHz                                       |      | 1440  |       | pF    |
| C <sub>oss</sub>                   | Output Capacitance                |                                                                                                      |      | 905   |       | pF    |
| C <sub>rss</sub>                   | Reverse Transfer Capacitance      |                                                                                                      |      | 355   |       | pF    |
| SWITCHING CHARACTERISTICS (Note 2) |                                   |                                                                                                      |      |       |       |       |
| t <sub>D(on)</sub>                 | Turn - On Delay Time              | V <sub>DD</sub> = -15 V, I <sub>D</sub> = -7 A,<br>V <sub>GEN</sub> = -10 V, R <sub>GEN</sub> = 12 Ω |      | 10    | 20    | ns    |
| t <sub>r</sub>                     | Turn - On Rise Time               |                                                                                                      |      | 65    | 120   | ns    |
| t <sub>D(off)</sub>                | Turn - Off Delay Time             |                                                                                                      |      | 70    | 130   | ns    |
| t <sub>f</sub>                     | Turn - Off Fall Time              |                                                                                                      |      | 70    | 130   | ns    |
| Q <sub>g</sub>                     | Total Gate Charge                 | V <sub>DS</sub> = -10 V,<br>I <sub>D</sub> = -7.5 A, V <sub>GS</sub> = -10 V                         |      | 47    | 67    | nC    |
| Q <sub>gs</sub>                    | Gate-Source Charge                |                                                                                                      |      | 5     |       | nC    |
| Q <sub>gd</sub>                    | Gate-Drain Charge                 |                                                                                                      |      | 12    |       | nC    |

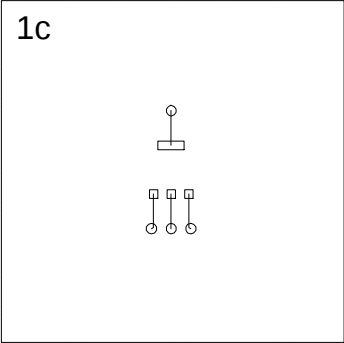
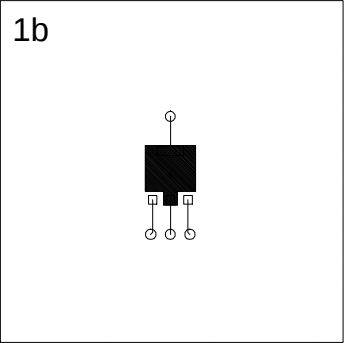
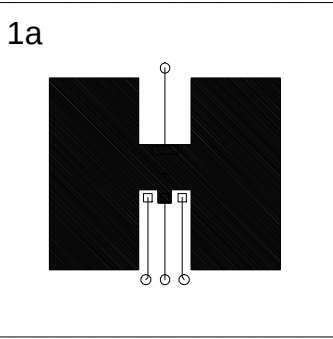
Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

| Symbol                                                 | Parameter                                             | Conditions                                                                     | Min | Typ    | Max  | Units |
|--------------------------------------------------------|-------------------------------------------------------|--------------------------------------------------------------------------------|-----|--------|------|-------|
| DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS |                                                       |                                                                                |     |        |      |       |
| I <sub>S</sub>                                         | Maximum Continuous Drain-Source Diode Forward Current |                                                                                |     |        | -2.5 | A     |
| V <sub>SD</sub>                                        | Drain-Source Diode Forward Voltage                    | V <sub>GS</sub> = 0 V, I <sub>S</sub> = - 2.5 A (Note 2)                       |     | - 0.85 | -1.2 | V     |
| t <sub>rr</sub>                                        | Reverse Recovery Time                                 | V <sub>GS</sub> = 0 V, I <sub>F</sub> = - 2.5 A dI <sub>F</sub> /dt = 100 A/μs |     |        | 140  | ns    |

Notes:

1.  $P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$  R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is defined by users. For general reference: Applications on 4.5"x5" FR-4 PCB under still air environment, typical R<sub>θJA</sub> is found to be:

- a. 42°C when mounted on a 1 in<sup>2</sup> pad of 2oz copper.
- b. 95°C when mounted on a 0.066in<sup>2</sup> pad of 2oz copper.
- c. 110°C/W when mounted on a 0.00123in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

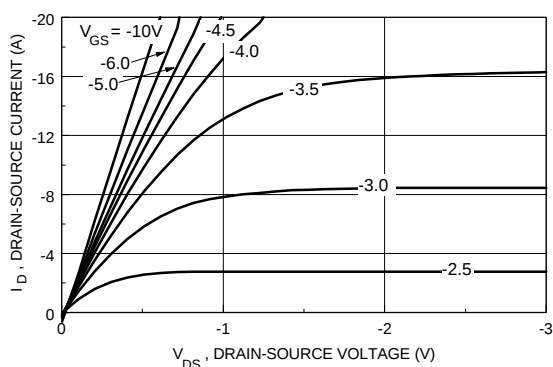


Figure 1. On-Region Characteristics.

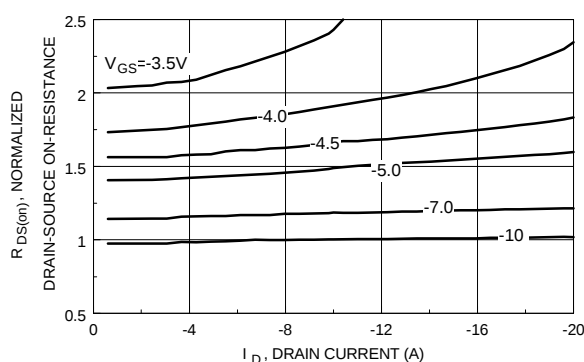


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

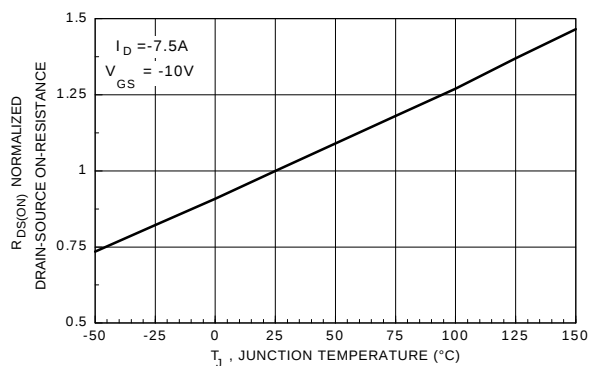


Figure 3. On-Resistance Variation with Temperature.

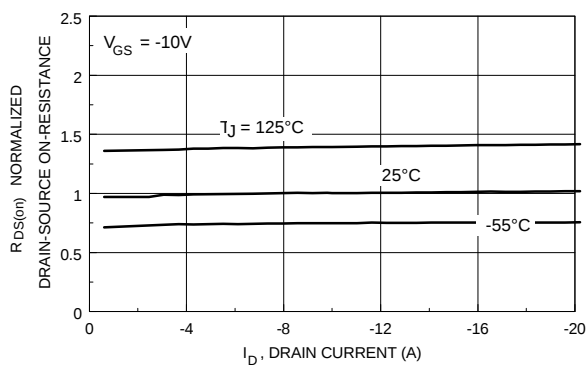


Figure 4. On-Resistance Variation with Drain Current and Temperature.

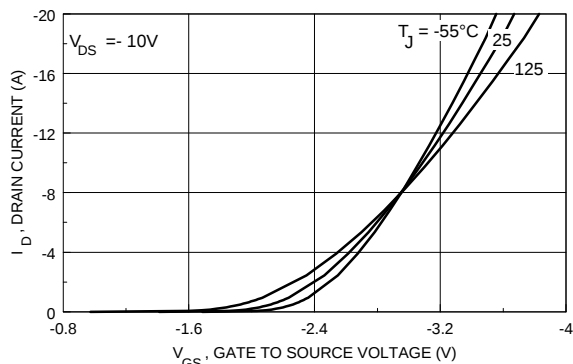


Figure 5. Transfer Characteristics.

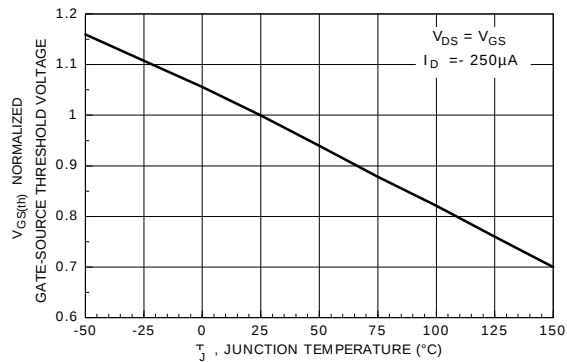
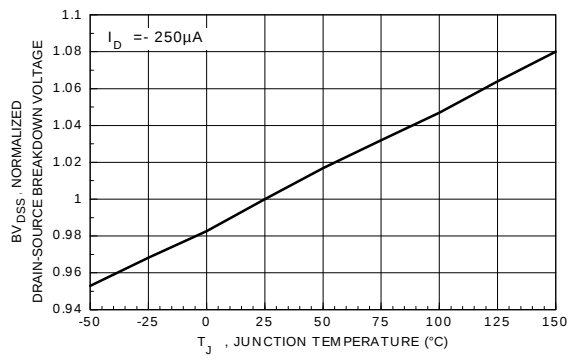
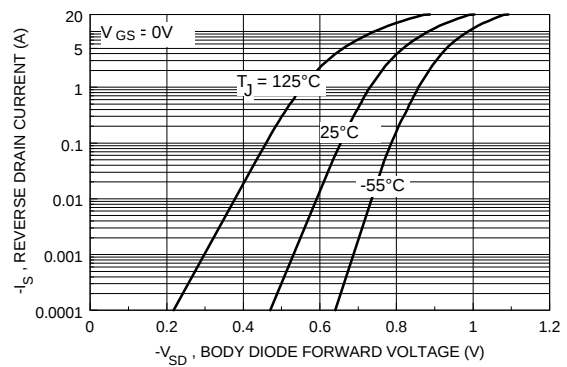


Figure 6. Gate Threshold Variation with Temperature.

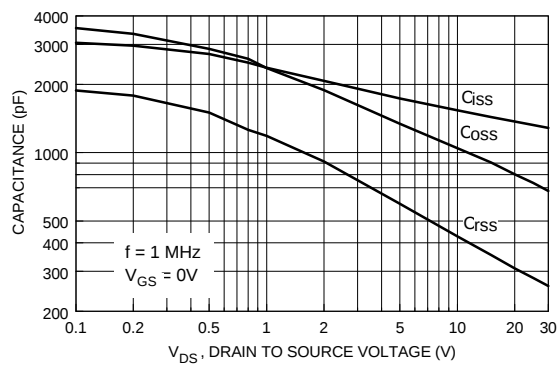
## Typical Electrical Characteristics



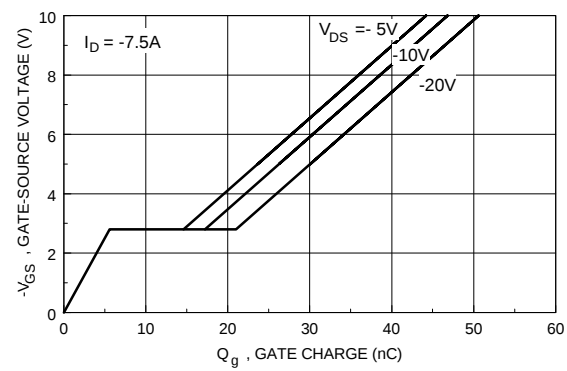
**Figure 7. Breakdown Voltage Variation with Temperature.**



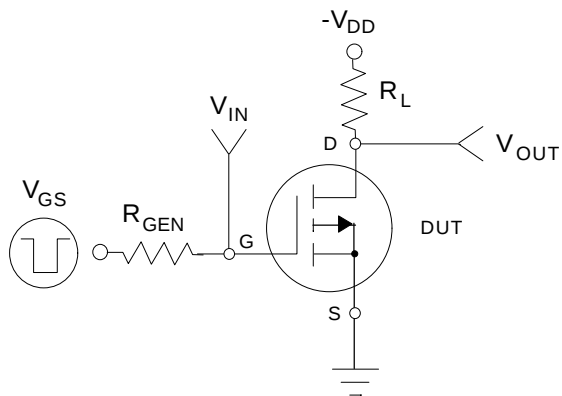
**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.**



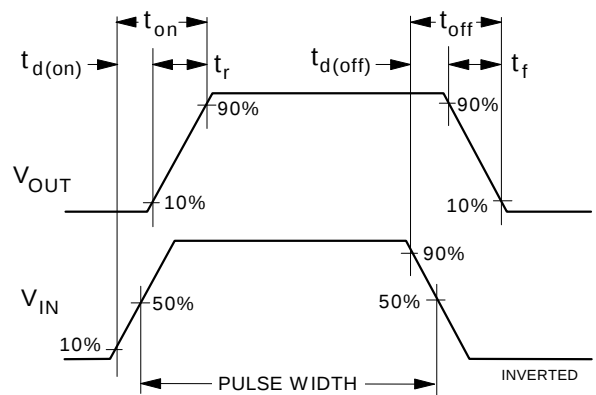
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**



**Figure 11. Switching Test Circuit.**



**Figure 12. Switching Waveforms.**

## Typical Thermal Characteristics

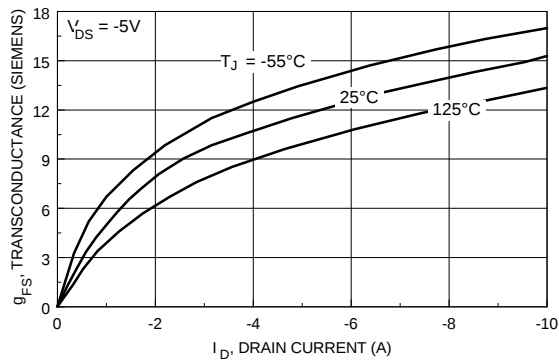


Figure 13. Transconductance Variation with Drain Current and Temperature.

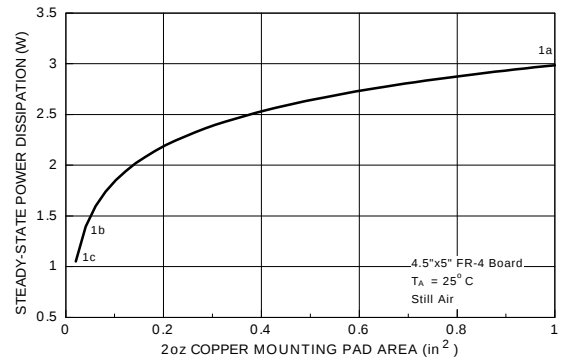


Figure 14. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

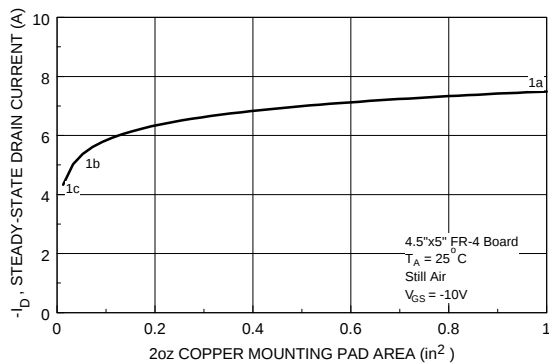


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

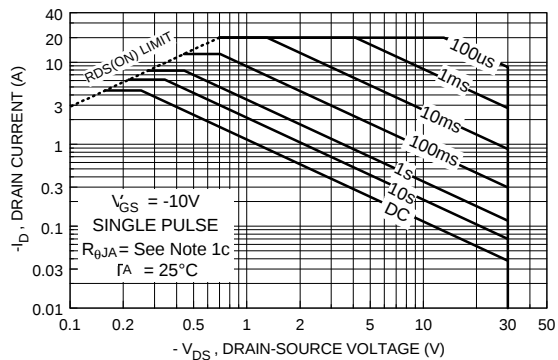


Figure 16. Maximum Safe Operating Area.

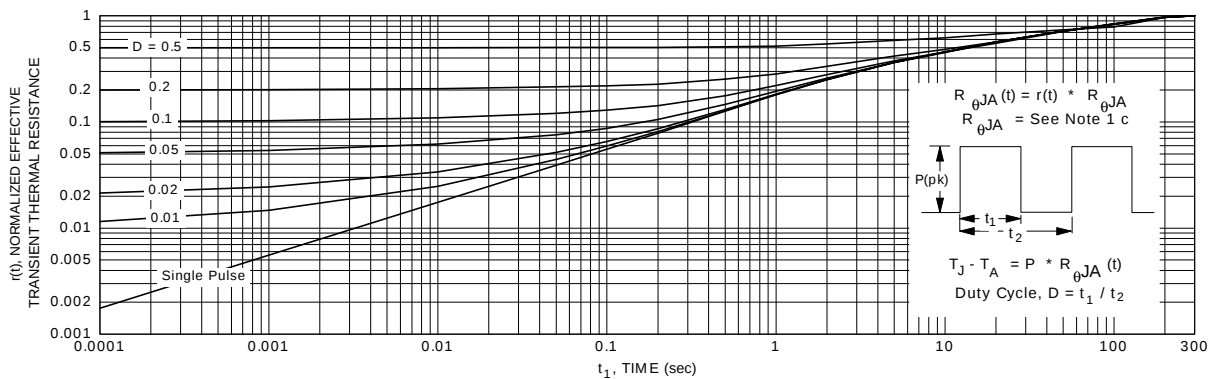


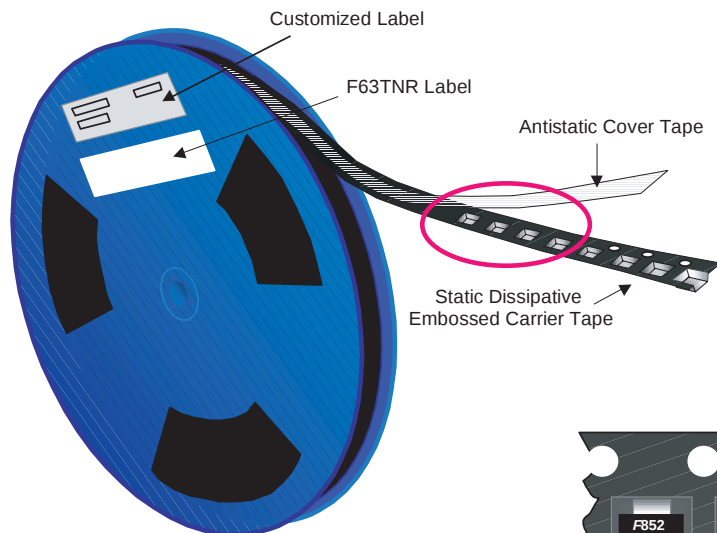
Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

# SOT-223 Tape and Reel Data and Package Dimensions



## SOT-223 Packaging Configuration: Figure 1.0

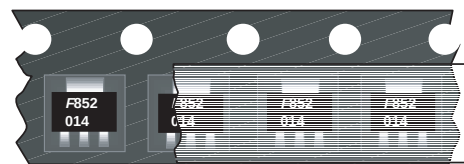


### Packaging Description:

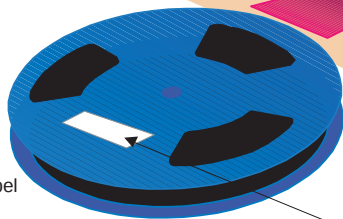
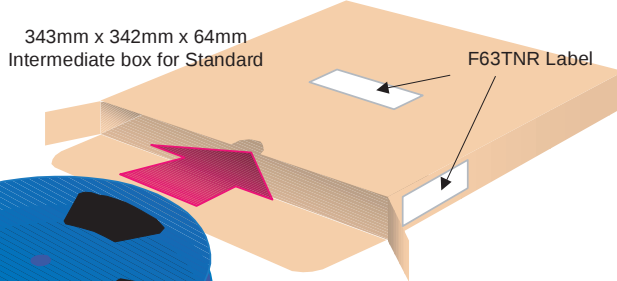
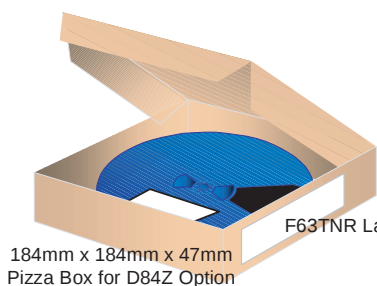
SOT-223 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

| SOT-223 Packaging Information |                         |            |
|-------------------------------|-------------------------|------------|
| Packaging Option              | Standard (no flow code) | D84Z       |
| Packaging type                | TNR                     | TNR        |
| Qty per Reel/Tube/Bag         | 2,500                   | 500        |
| Reel Size                     | 13" Dia                 | 7" Dia     |
| Box Dimension (mm)            | 343x64x343              | 184x187x47 |
| Max qty per Box               | 5,000                   | 1,000      |
| Weight per unit (gm)          | 0.1246                  | 0.1246     |
| Weight per Reel (kg)          | 0.7250                  | 0.1532     |
| Note/Comments                 |                         |            |



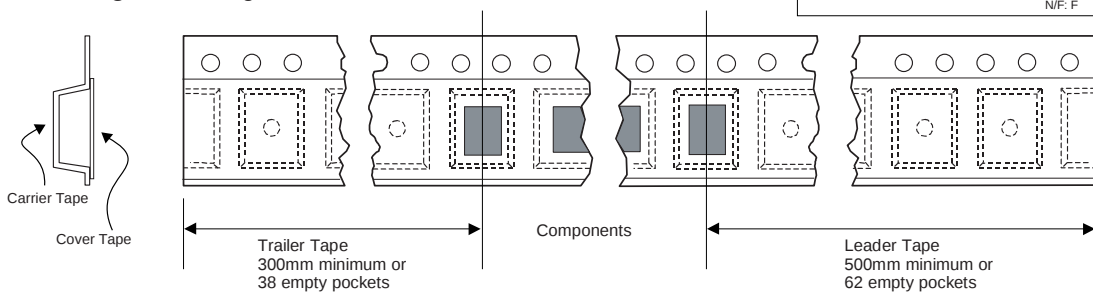
### SOT-223 Unit Orientation



### F63TNR Label sample



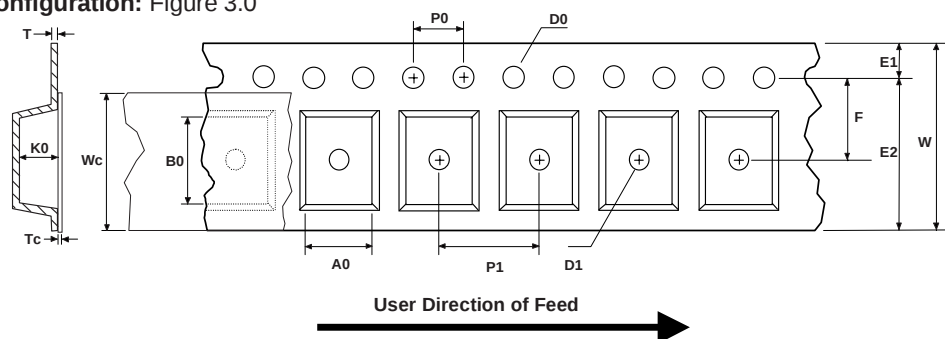
## SOT-223 Tape Leader and Trailer Configuration: Figure 2.0



## SOT-223 Tape and Reel Data and Package Dimensions, continued

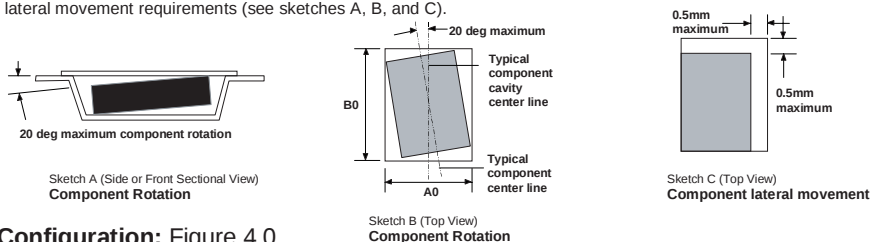
### SOT-223 Embossed Carrier Tape

Configuration: Figure 3.0

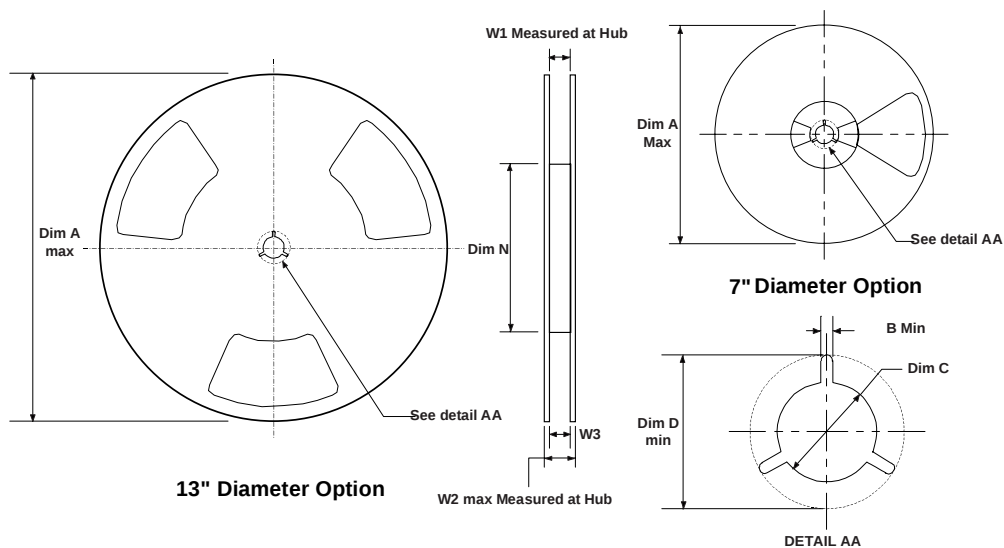


| Dimensions are in millimeter |                 |                 |                |                 |                 |                 |              |                 |               |               |                 |                        |                 |                 |
|------------------------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|--------------|-----------------|---------------|---------------|-----------------|------------------------|-----------------|-----------------|
| Pkg type                     | A0              | B0              | W              | D0              | D1              | E1              | E2           | F               | P1            | P0            | K0              | T                      | Wc              | Tc              |
| SOT-223<br>(12mm)            | 6.83<br>+/-0.10 | 7.42<br>+/-0.10 | 12.0<br>+/-0.3 | 1.55<br>+/-0.05 | 1.50<br>+/-0.10 | 1.75<br>+/-0.10 | 10.25<br>min | 5.50<br>+/-0.05 | 8.0<br>+/-0.1 | 4.0<br>+/-0.1 | 1.88<br>+/-0.10 | 0.292<br>+/-<br>0.0130 | 9.5<br>+/-0.025 | 0.06<br>+/-0.02 |

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



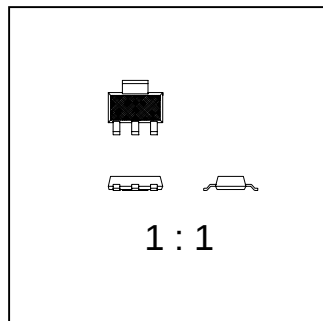
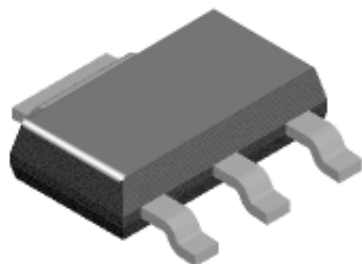
### SOT-223 Reel Configuration: Figure 4.0



| Dimensions are in inches and millimeters |             |               |              |                                   |               |              |                                  |               |                              |
|------------------------------------------|-------------|---------------|--------------|-----------------------------------|---------------|--------------|----------------------------------|---------------|------------------------------|
| Tape Size                                | Reel Option | Dim A         | Dim B        | Dim C                             | Dim D         | Dim N        | Dim W1                           | Dim W2        | Dim W3 (LSL-USL)             |
| 12mm                                     | 7" Dia      | 7.00<br>177.8 | 0.059<br>1.5 | 512 +0.020/-0.008<br>13 +0.5/-0.2 | 0.795<br>20.2 | 5.906<br>150 | 0.488 +0.078/-0.000<br>12.4 +2/0 | 0.724<br>18.4 | 0.469 – 0.606<br>11.9 – 15.4 |
| 12mm                                     | 13" Dia     | 13.00<br>330  | 0.059<br>1.5 | 512 +0.020/-0.008<br>13 +0.5/-0.2 | 0.795<br>20.2 | 7.00<br>178  | 0.488 +0.078/-0.000<br>12.4 +2/0 | 0.724<br>18.4 | 0.469 – 0.606<br>11.9 – 15.4 |

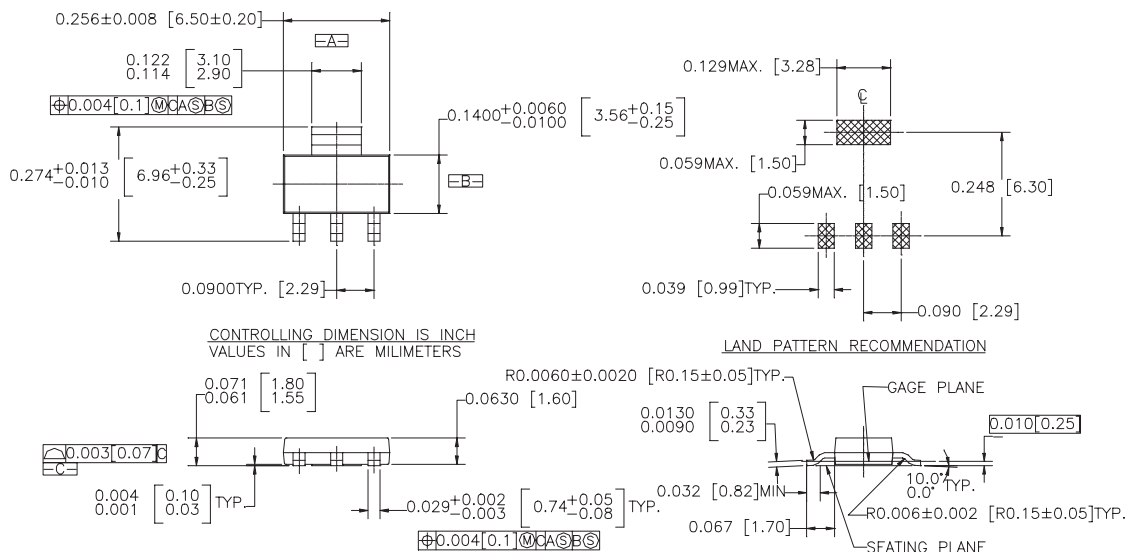
## SOT-223 Tape and Reel Data and Package Dimensions, continued

### SOT-223 (FS PKG Code 47)



Scale 1:1 on letter size paper

Part Weight per unit (gram): 0.1246



NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH TO BE 150 MICRONS/ 3.81 MICROMETERS

MINIMUM TIN/LEAD (SOLDER) ON COPPER.

2. REFERENCE JEDEC REGISTRATION TO-261, VARIATION AA, ISSUE A, DATED JAN 1990

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE<sup>x</sup><sup>TM</sup>  
CoolFET<sup>TM</sup>  
CROSSVOLT<sup>TM</sup>  
E<sup>2</sup>CMOS<sup>TM</sup>  
FACT<sup>TM</sup>  
FACT Quiet Series<sup>TM</sup>  
FAST<sup>®</sup>  
FAST<sup>r</sup><sup>TM</sup>  
GTO<sup>TM</sup>  
HiSeC<sup>TM</sup>

ISOPLANAR<sup>TM</sup>  
MICROWIRE<sup>TM</sup>  
POP<sup>TM</sup>  
PowerTrench<sup>TM</sup>  
QFET<sup>TM</sup>  
QS<sup>TM</sup>  
Quiet Series<sup>TM</sup>  
SuperSOT<sup>TM</sup>-3  
SuperSOT<sup>TM</sup>-6  
SuperSOT<sup>TM</sup>-8

TinyLogic<sup>TM</sup>  
UHC<sup>TM</sup>  
VCX<sup>TM</sup>

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status         | Definition                                                                                                                                                                                                            |
|--------------------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Advance Information      | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.                                                                                    |
| Preliminary              | First Production       | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production        | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.                                                       |
| Obsolete                 | Not In Production      | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.                                                   |