

## STEPPER MOTOR CONTROLLER

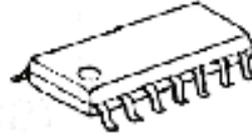
### ■ GENERAL DESCRIPTION

NJU7380 is a controller with transrator which convert from input step and direction pulse to driver's phase signal for full and half step.

NJU7380 translates from pulse input signal (Serial interface) to phase signal input, so NJM3700 series dual channel bipolar drivers or NJM2672 dual H-bridge driver can be easily controlled by a micro processor .

NJU7380 is also including Auto Current Down (ACD) circuit which is suitable for reducing power dissipation of power devices and motor.

### ■ PACKAGE OUTLINE

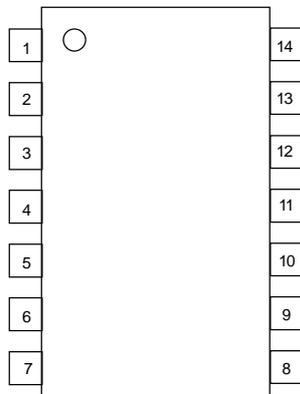


NJU7380E

### ■ FEATURES

- Operating Voltage  $V_{DD}=4.75 \sim 5.25V$
- Absolute Maximum Voltage 7V
- Half -step and Full - step Operation
- Internal Phase Logic
- Phase Logic Reset Terminal(RESET)
- Internal Auto Current Down Function
- Specially matched to NJM3775,NJM3777 and NJM2672.
- C-MOS Technology
- Package Outline EMP14

### ■ PIN CONFIGURATIONS



- |          |              |
|----------|--------------|
| 1. DIR   | 8. PGND      |
| 2. STEP  | 9. ACD       |
| 3. HSM   | 10. Dis2     |
| 4. RESET | 11. Dis1     |
| 5. MO    | 12. P2       |
| 6. Ct    | 13. P1       |
| 7. SGND  | 14. $V_{DD}$ |

Fig. 1 Pin Configurations

# NJU7380

## ■ BLOCK DIAGLAM

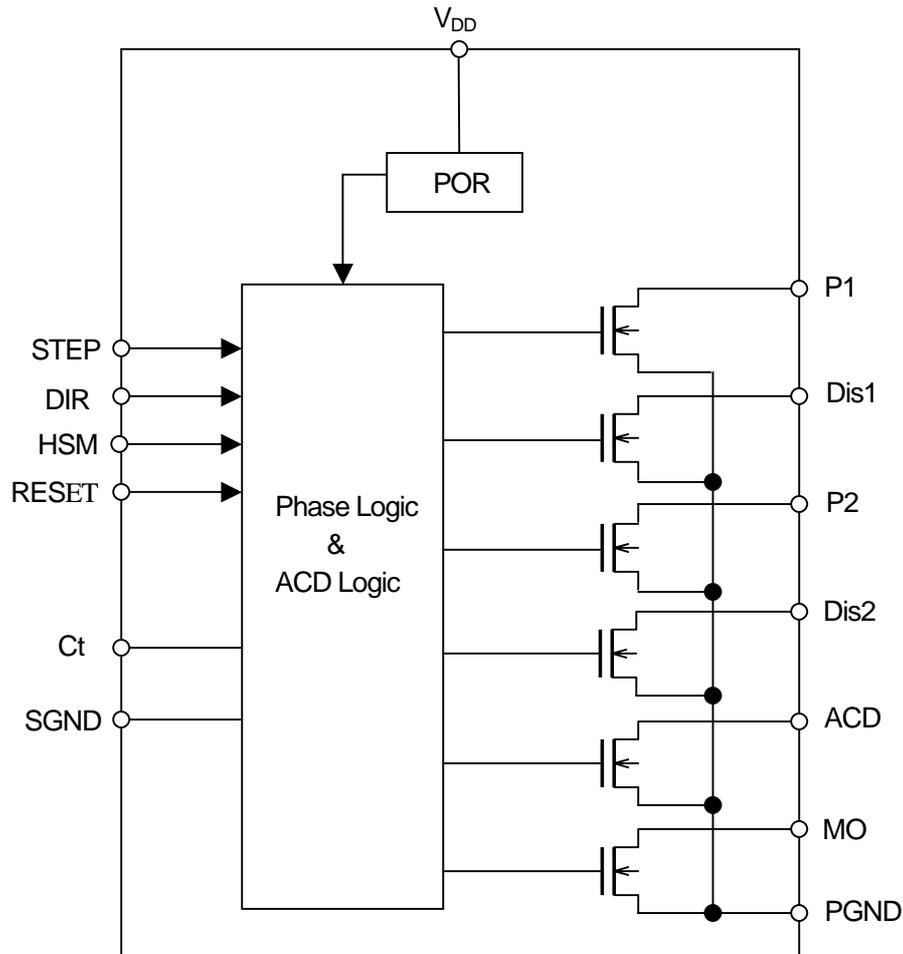


Fig.2 Block Diagram

## ■ PIN DESCRIPTION

Pin	Pin name	Description
1	DIR	Direction command input for determining motor turning direction
2	STEP	Motor stepping pulse input, phase logic operation triggered by negative edge of STEP signal
3	HSM	Half/Full step mode switching input H level in full step mode and L level in half step mode
4	RESET	Phase logic initial input
5	MO	Phase output initial status detection output
6	Ct	A value of connected capacitor determines lock detection time (Ton) and auto resume time (Toff)
7	SGND	SGND (Logic GND) and PGND (Analog GND) is not connect in the IC
8	PGND	SGND and PGND pins should be connected ground respectively.
9	ACD	Auto Current Down output terminal L level in active
10	DIS2	Step sequence output terminals
11	DIS1	P1/DIS1(P2/DIS2) determine a sequence output on Phase1(2) for driver IC
12	P2	P1(P2) determine a motor current direction on Phase1(2) for driver IC
13	P1	DIS1(DIS2) determine a phase current OFF mode at the half-step
14	V <sub>DD</sub>	Logic power supply voltage terminal

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	RATINGS	SYMBOL [unit]	NOTE
Supply Voltage	+7.0	V <sub>DD</sub> [V]	
Input Voltage	-0.3 ~ V <sub>DD</sub> +0.3	V <sub>ID</sub> [V]	
Output Current	10	I <sub>O</sub> [mA]	
Operating Temperature Range	-40 ~ 85	T <sub>OPR</sub> [°C]	
Storage Temperature Range	-40 ~ +125	T <sub>STG</sub> [°C]	
Power Dissipation	300	P <sub>D</sub> [mW]	Device itself

## ■ RECOMMENDED OPERATING CONDITIONS

V<sub>DD</sub>=4.75V~5.25V

## ■ ELECTRICAL CHARACTERISTICS

(V<sup>+</sup>=5V, Ta=25°C)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I <sub>DD</sub>	No Signal	-	0.2	0.3	mA
H Level Input Voltage	V <sub>IH</sub>	-	3.5	-	-	V
L Level Input Voltage	V <sub>IL</sub>	-	-	-	1.5	V
H Level Input Current	I <sub>IH</sub>	-	-	0.1	1.0	μA
L Level Input Current	I <sub>IL</sub>	-	-	-50	-100	μA
Phase Output Saturation Voltage	V <sub>P</sub>	I <sub>P</sub> =5mA	-	-	0.5	V
DIS Output Saturation Voltage	V <sub>DIS</sub>	I <sub>DIS</sub> =5mA	-	-	0.5	V
VR Detection Voltage	V <sub>VR</sub>	I <sub>MO</sub> =5mA	-	-	0.5	V
MO Output Saturation Voltage	V <sub>MO</sub>	I <sub>MO</sub> =5mA	-	-	0.5	V
Output Leak Current	I <sub>LEAK</sub>	V <sub>DD</sub> =7V	-	-	1	μA
Power Down ON Time	T <sub>ON</sub>	C <sub>T</sub> =0.1μF	-	200	-	ms
Turn ON Time	T <sub>DON</sub>	-	-	-	3	μs
Set-up Time	T <sub>S</sub>	-	400	-	-	ns
Step-pulse Continuation Time	V <sub>SPC</sub>	-	800	-	-	ns

# NJU7380

## APPLICATION INFORMATION

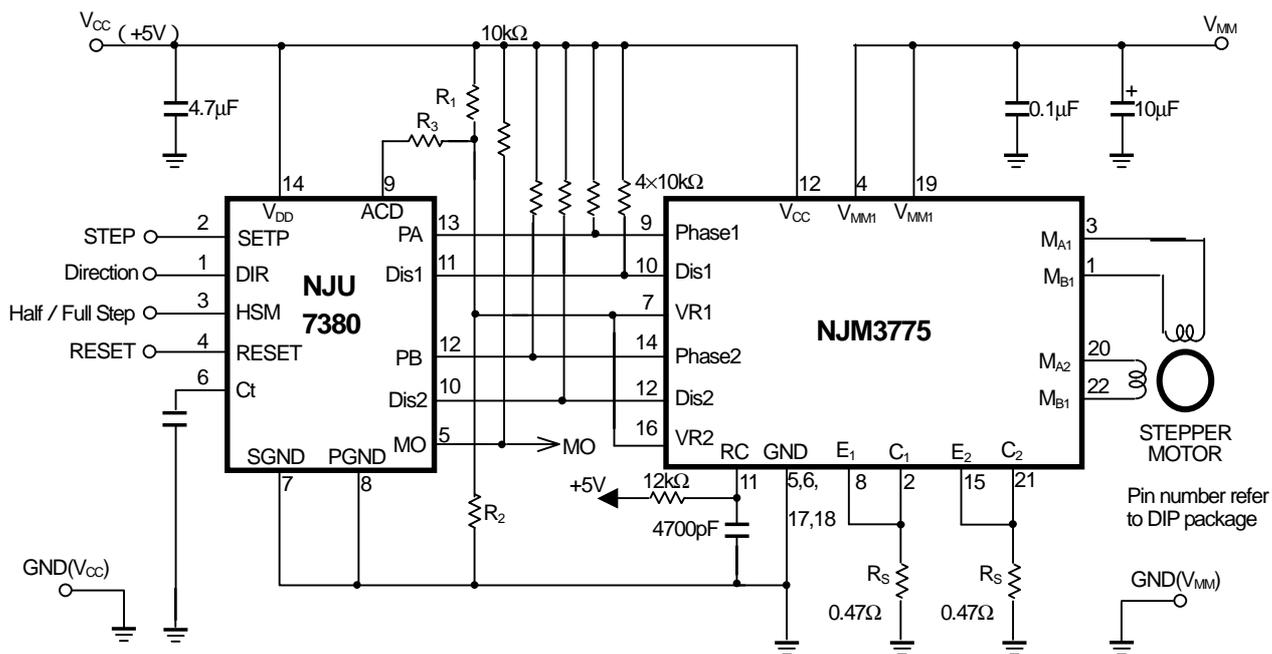


Fig.3 Typical stepper motor driver application with NJM3775.

## FUNCTIONAL DESCRIPTION

NJU7380 is a transrator, intended to convert from input step and direction pulse to driver's phase signal for 2-phase stepper motor driver. Motor control is simply attained only by the pulse generator because you use it by NJM3775 and the set.

## LOGIC INPUT

NJU7380 contains all phase logic necessary to control the motor in a proper way. If any of the logic inputs are left open, the circuit will accept it as a HIGH level. In order to make noise-proof nature into the maximum, it is necessary to connect an idle input terminal to V<sub>DD</sub> level.

### STEP – Stepping pulse

The built-in phase logic sequencer goes UP on every negative edge of the STEP signal (pulse). In full step mode, the pulse turns the stepping motor at the basic step angle. In half step mode, two pulses are required to turn the motor at the basic step angle.

The DIR (direction) signal and HSM (half/full mode) are latched to the STEP negative edge and must therefore be established before the start of the negative edge. Note the setup time t<sub>s</sub> in Figure 4.

### DIR – direction

The DIR signal determines the step direction. The direction of the stepping motor depends on how the NJU7380 and NJM3775 are connected to the motor. Although DIR can be modified this should be avoided since a misstep of 1 pulse increment may occur if it is set simultaneous with the negative edge. See the timing chart in Figure 4.

- HSM – half/full step mode switching

This signal determines whether the stepping motor turns at half step or full step mode. The built-in phase logic is set to the half step mode when HSM is low level. Although HSM can be modified this should be avoided since a misstep of 1 pulse increment may occur if it is set simultaneous with the negative edge. See the timing chart in Figure 4.

- RESET

A two-phase stepping motor repeats the same winding energizing sequence every angle that is a multiple of four of the basic step. The phase logic sequence is repeated every four pulses in the full step mode and every eight pulses in the half step mode.

RESET forces to initialize the phase logic to sequence start mode.

When RESET is at L level, the phase logic is initialized and the energizing pattern of phase logic at sequence start is output. At this time, the STEP input of phase logic will be ignored during the RESET is at L level.

- POR – power on and reset function

The internal power-on and reset circuit, which is connected to Vcc, resets the phase logic and turns off phase output when the power is supplied to prevent missteps.

Each time the power is turned on, the energizing pattern of phase logic at sequence start is output.

- MO – origin monitor

At sequence start of the phase logic or after POR or external RESET, an L level output is made to indicate to external devices that the energizing sequence is in initial status.

In a system using a stepping motor, the device sensor and the MO AND function enable a higher resolution detection of motor origin.

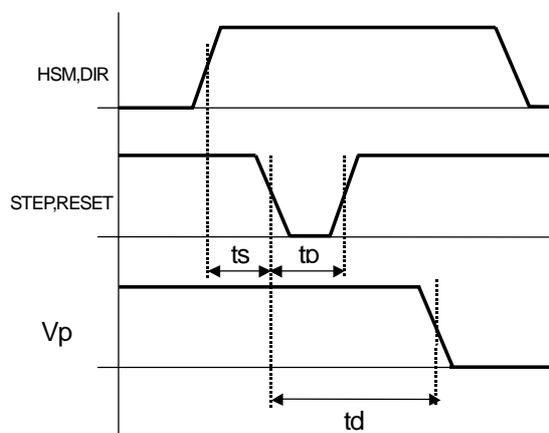


Fig.4 Timing chart

## ■ TIMING CHART

Fig.5-1 Full-step mode,forward  
4-step sequence

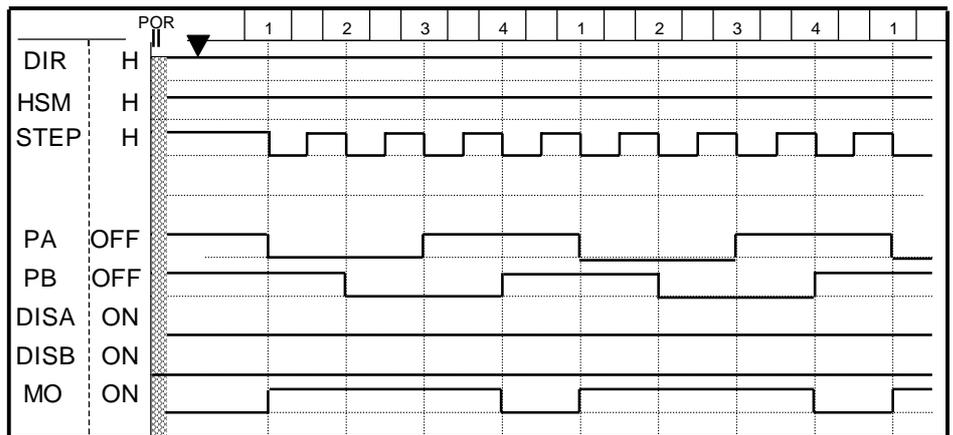


Fig.5-2 Full-step mode,reverse  
4-step sequence

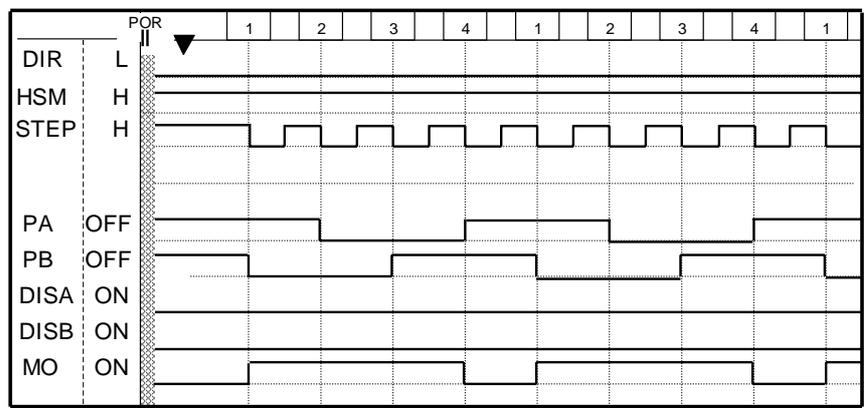


Fig.5-3 Half-step mode,forward  
8-step sequence

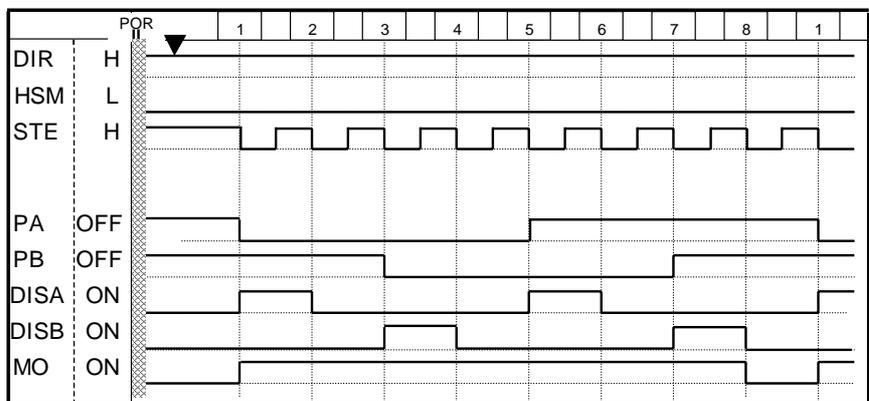
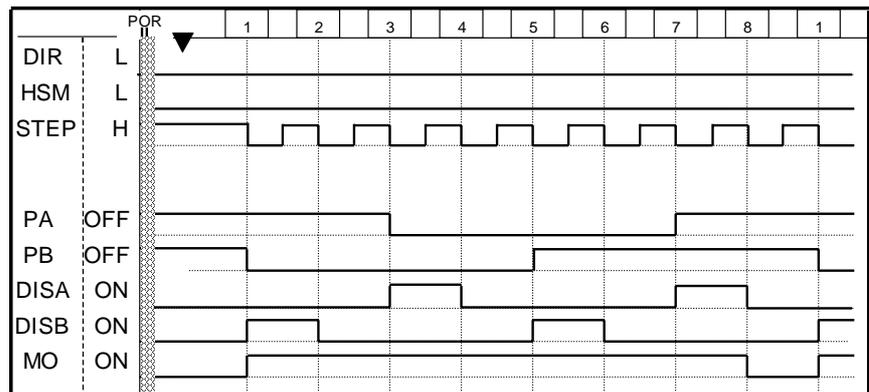


Fig.5-4 Half-step mode,reverse  
8-step sequence



## ■ ACD – auto current down function

The ACD feature monitors step signals and sets the ACD pin output to H when the negative edge of a STEP signal is input. It then sets the ACD output to L after a time ( $T_{ON}$ ) that is fixed by the capacitor that is connected to the Ct pin.

By combining this pin with the VR pin that determines motor current for the NJM3775 motor, it is possible to reduce current when stopping the motor.

If the next negative edge of a STEP is input during the time  $T_{ON}$ , an internal retrigger will operate, maintaining the ACD pin's H output.

That is, after the final negative edge of a STEP is input, ACD H output is maintained during the time  $T_{ON}$ , after which it is set to L.

The time  $T_{ON}$  must be long enough to securely stop the stepping motor.

Approximately 100mS is usually sufficient for normal applications.

The following expression determines the time  $T_{ON}$ .

$$T_{on}[ms]=3 \times 10^9 \times C_t[F]$$

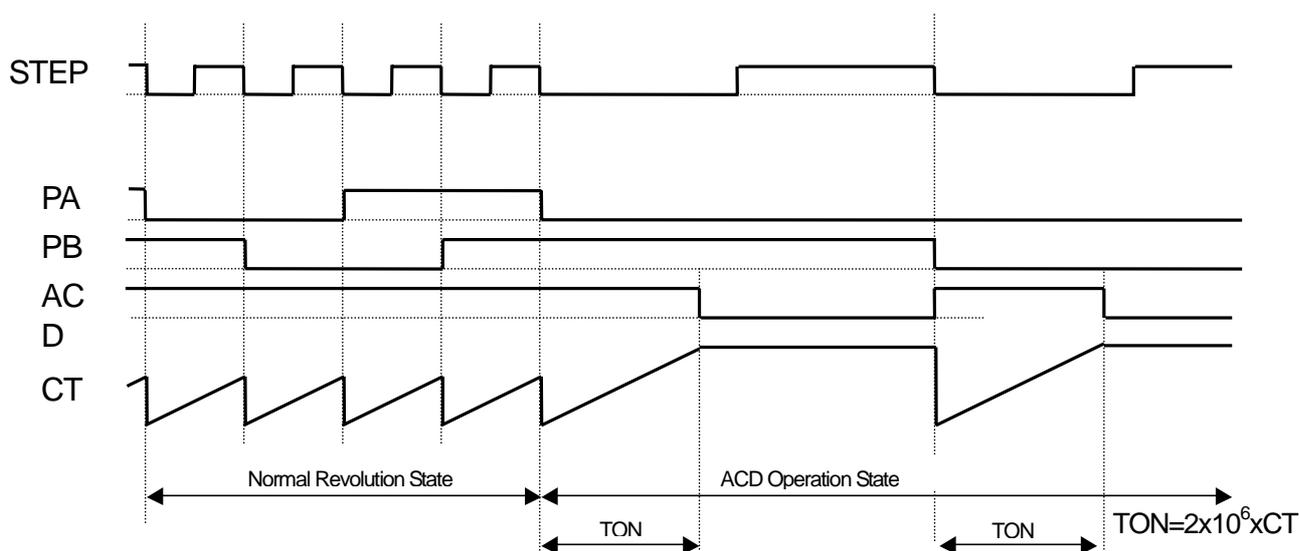


Fig.6 ACD Operation Timing Diagram

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