CY7C1021CV33

64K x 16 Static RAM

Features

- **Pin- and function-compatible with CY7C1021BV33**
- **High speed**
  - **t_{AA} = 8, 10, 12, and 15 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **360 mW (max.)**
- **Data retention at 2.0V**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in 44-pin TSOP II, 400-mil SOJ, 48-ball FBGA**

Functional Description

The CY7C1021CV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

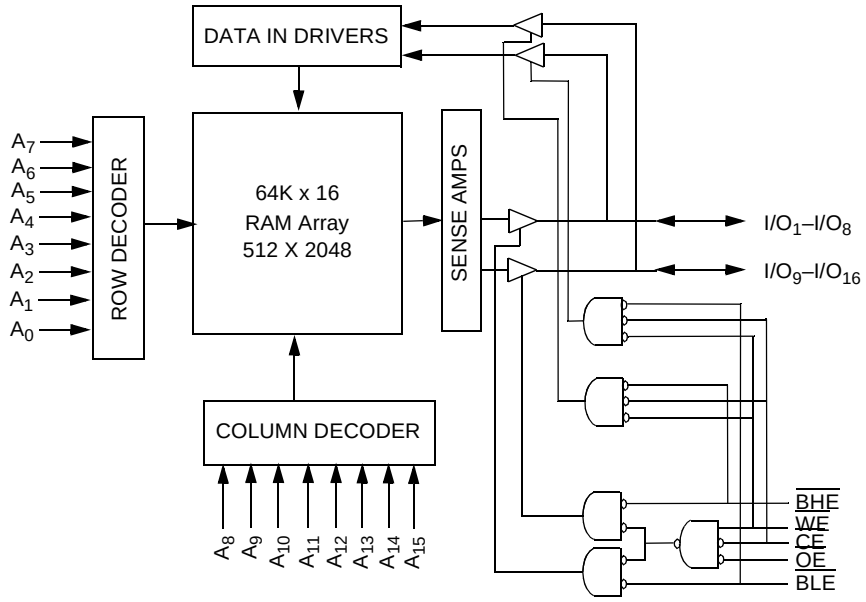
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_9 to I/O_{16}. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

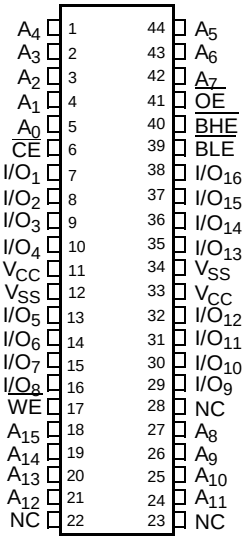
The CY7C1021CV33 is available in standard 44-pin TSOP Type II 400-mil-wide SOJ packages, as well as a 48-ball FBGA.

Logic Block Diagram



Pin Configuration

SOJ / TSOP II
Top View



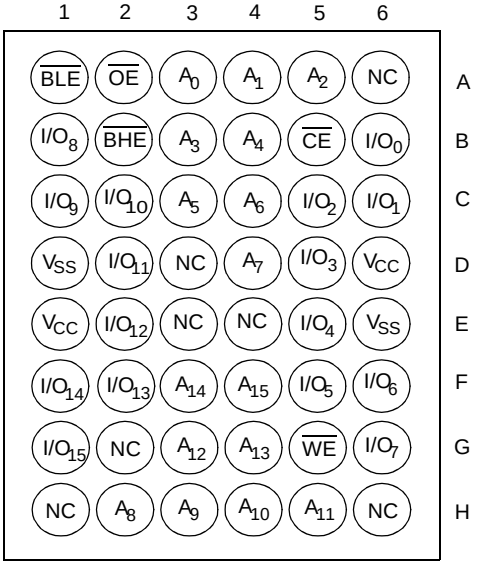
Selection Guide

	CY7C1021CV33-8	CY7C1021CV33-10	CY7C1021CV33-12	CY7C1021CV33-15	Unit
Maximum Access Time	8	10	12	15	ns
Maximum Operating Current	95	90	85	80	mA
Maximum CMOS Standby Current	5	5	5	5	mA

Pin Configuration

48-ball FBGA

(Top View)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[1] .....–0.5V to V_{CC}+0.5V

DC Input Voltage[1].....–0.5V to V_{CC}+0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1021CV33-8		1021CV33-10		1021CV33-12		1021CV33-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	+1	–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–1	+1	–1	+1	–1	+1	–1	+1	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		-300		–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		95		90		85		80	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		15		15		15		15	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0		5		5		5		5	mA

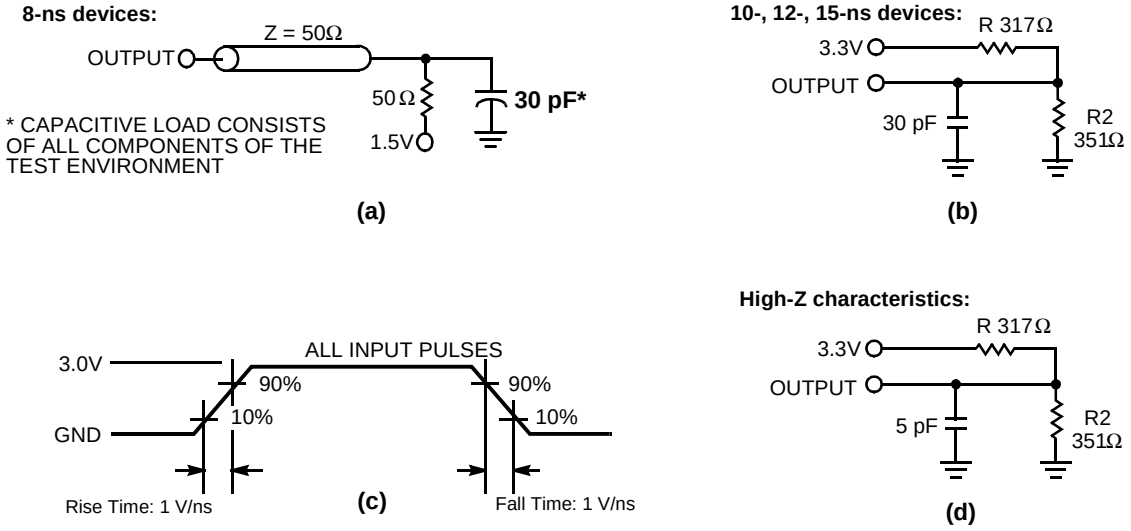
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[4]



Note:

4. AC characteristics (except High-Z) for all 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

Switching Characteristics Over the Operating Range[5]

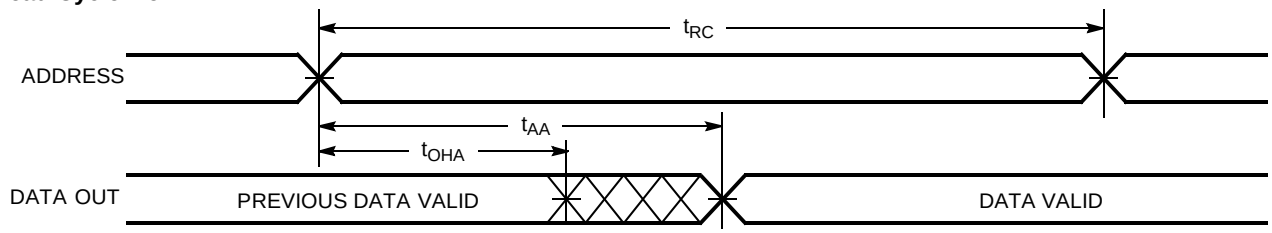
Parameter	Description	1021CV33-8		1021CV33-10		1021CV33-12		1021CV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[6]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6, 7]		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[6]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[6, 7]		4		5		6		7	ns
t_{PU}[8]	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}[8]	$\overline{CE}$ HIGH to Power-Down		8		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		5		6		7	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		0		0		ns
t_{HZBE}	Byte Disable to High-Z		4		5		6		7	ns
Write Cycle[9]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		9		10		ns
t_{AW}	Address Set-Up to Write End	7		8		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		7		8		10		ns
t_{SD}	Data Set-Up to Write End	5		5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[6]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6, 7]		4		5		6		7	ns
t_{BW}	Byte Enable to End of Write	6		7		8		9		ns

Notes:

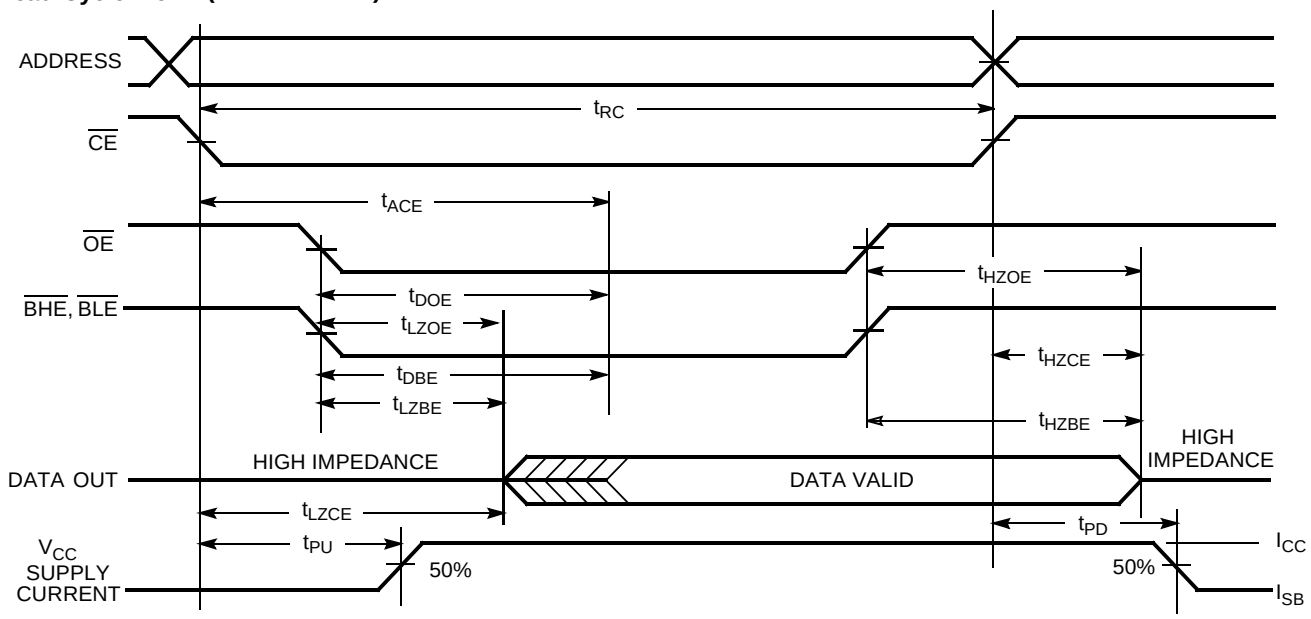
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. This parameter is guaranteed by design and is not tested.
9. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle No. 1[10, 11]



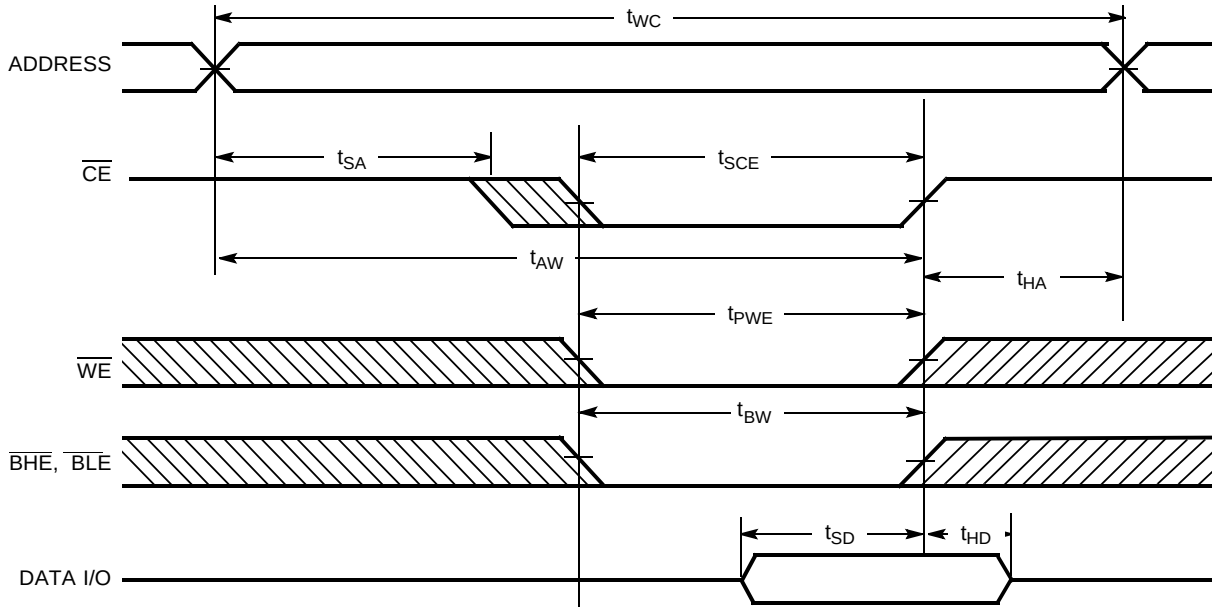
Read Cycle No. 2 ($\overline{OE}$ Controlled)[11, 12]



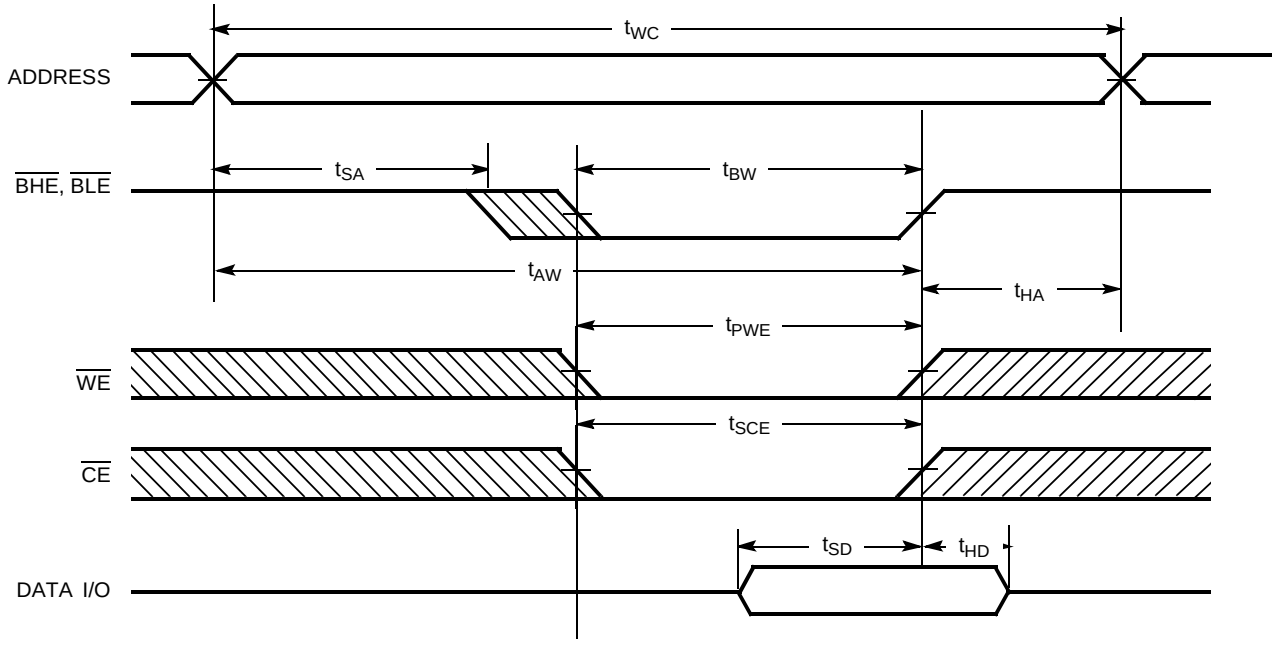
Notes:
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for Read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled) [13, 14]



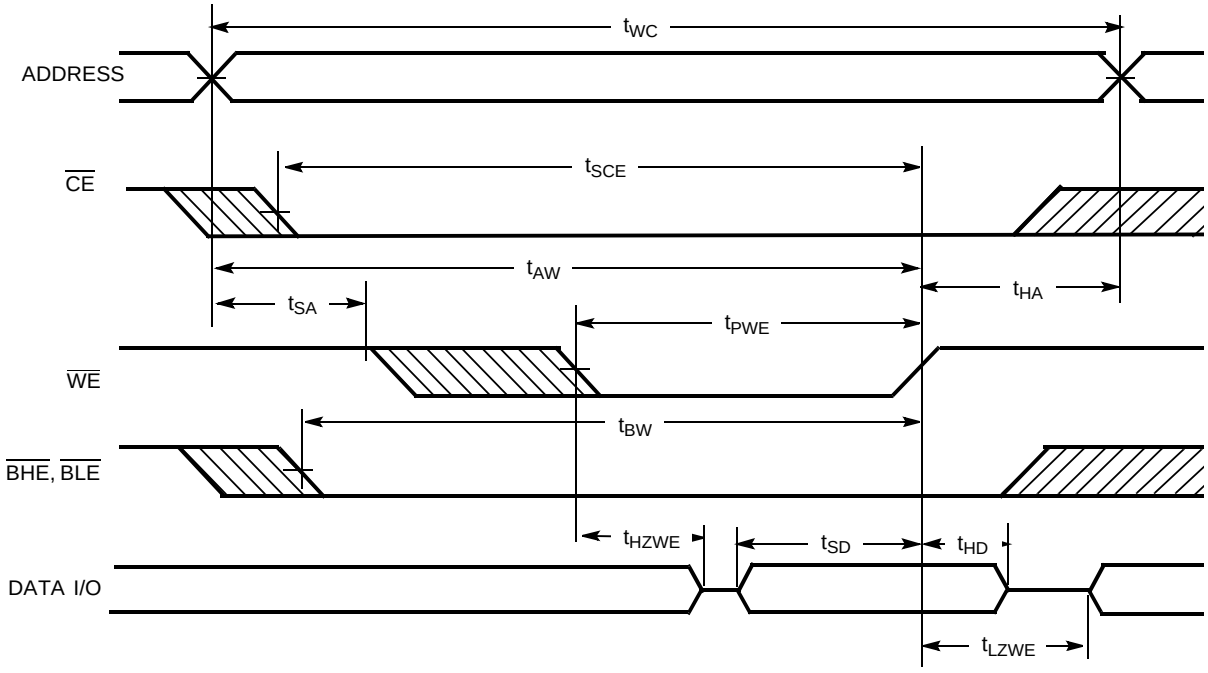
Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes:
13. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)



Truth Table

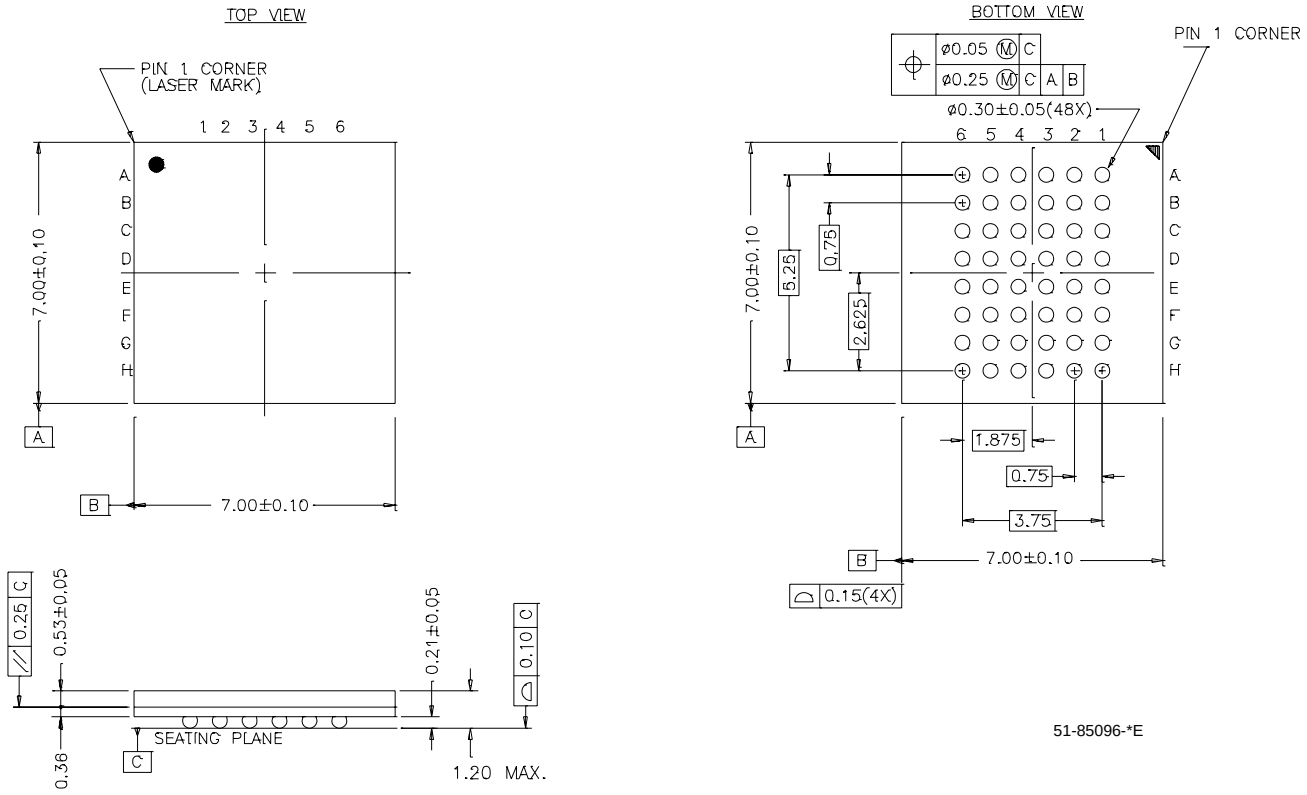
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High-Z	Read – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High-Z	Write – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1021CV33-8VC	V34	44-lead (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-8ZC	Z44	44-lead TSOP Type II	
	CY7C1021CV33-8BAC	BA48A	48-ball FBGA	
10	CY7C1021CV33-10VC	V34	44-lead (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-10VI			Industrial
	CY7C1021CV33-10ZC	Z44	44-lead TSOP Type II	Commercial
	CY7C1021CV33-10ZI			Industrial
	CY7C1021CV33-10BAC	BA48A	48-ball FBGA	Commercial
	CY7C1021CV33-10BAI			Industrial
12	CY7C1021CV33-12VC	V34	44-lead (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-12VI			Industrial
	CY7C1021CV33-12ZC	Z44	44-lead TSOP Type II	Commercial
	CY7C1021CV33-12ZI			Industrial
	CY7C1021CV33-12BAC	BA48A	48-ball FBGA	Commercial
	CY7C1021CV33-12BAI			Industrial
15	CY7C1021CV33-15VC	V34	44-lead (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-15VI			Industrial
	CY7C1021CV33-15ZC	Z44	44-lead TSOP Type II	Commercial
	CY7C1021CV33-15ZI			Industrial
	CY7C1021CV33-15BAC	BA48A	48-ball FBGA	Commercial
	CY7C1021CV33-15BAI			Industrial

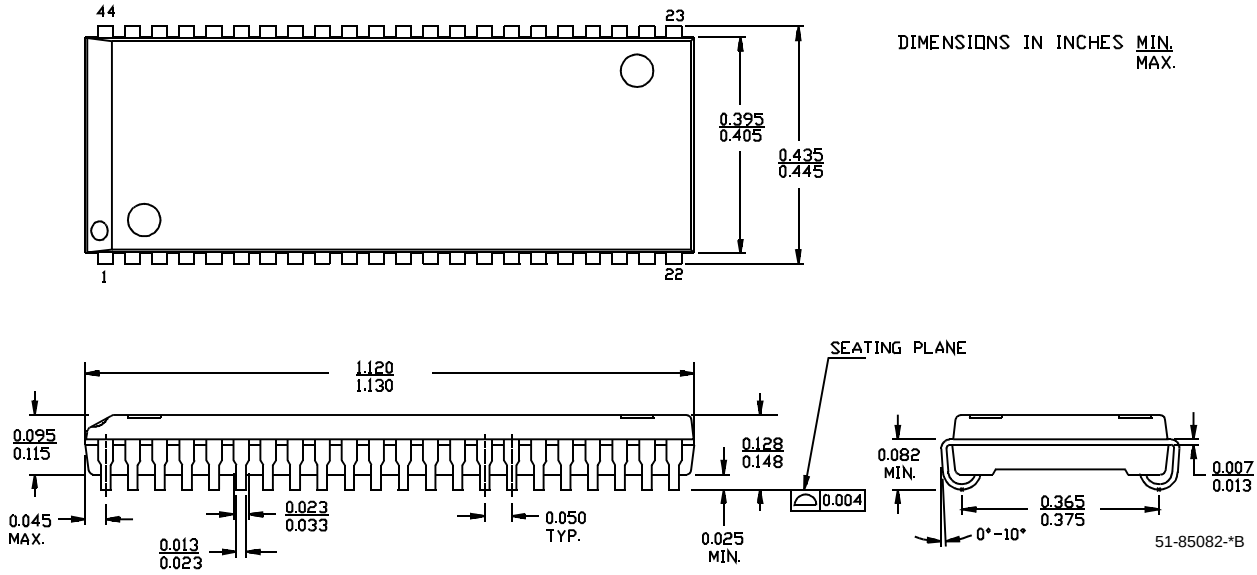
Package Diagrams

48-Ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A

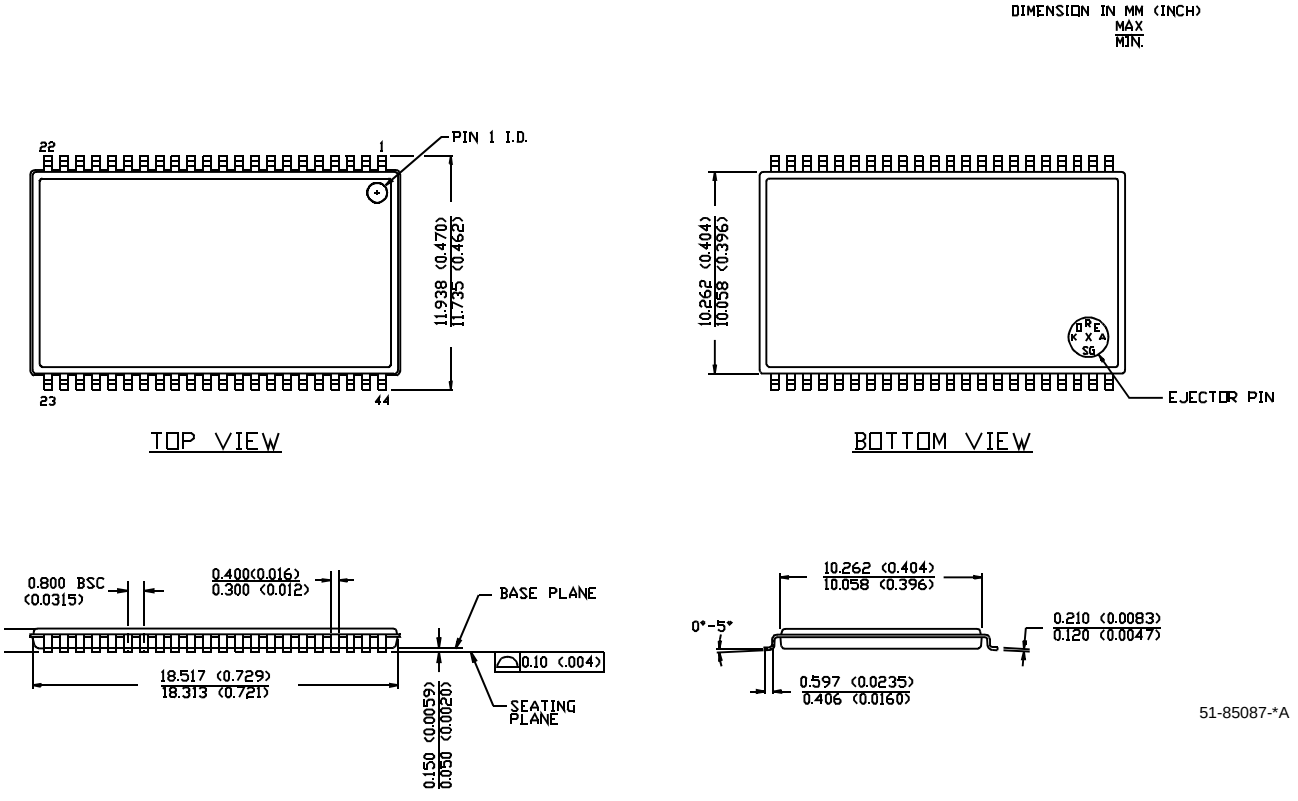


Package Diagrams (continued)

44-Lead (400-Mil) Molded SOJ V34



44-pin TSOP II Z44



Document History Page

Document Title: CY7C1021CV33 64K x 16 Static RAM Document Number: 38-05132				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109472	12/06/01	HGK	New Data Sheet
*A	115044	05/08/02	HGK	Ram7 version C4K x 16 Async. Remove “Preliminary”
*B	115808	06/25/02	HGK	I_{SB1} and I_{CC} values changed
*C	120413	10/31/02	DFP	Updated BGA pin E4 to NC.