Single 12-/10-/8-Bit I²C V_{OUT} DACs with 10ppm/°C Reference

FEATURES

- **Integrated Precision Reference**
  2.5V Full-Scale 10ppm/°C (LTC2631-L)
  4.096V Full-Scale 10ppm/°C (LTC2631-H)
- **Maximum INL Error: 1LSB (LTC2631A-12)**
- **Bidirectional Reference: Input or 10ppm/°C Output**
- **400kHz I²C™ Interface**
- Nine Selectable Addresses (LTC2631-Z)
- Low Noise (0.7mV$_{P-P}$, 0.1Hz to 200kHz)
- Guaranteed Monotonic Over Temperature
- 2.7V to 5.5V Supply Range (LTC2631-L)
- Low Power Operation: 180µA at 3V
- Power Down to 1.8µA Maximum (C and I Grades)
- Power-On Reset to Zero or Mid-Scale Options
- Double-Buffered Data Latches
- Guaranteed Operation From –40°C to 125°C (H-Grade)
- 8-Lead TSOT-23 (ThinSOT™) Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Automatic Test Equipment
- Portable Equipment
- Automotive
- Optical Networking

DESCRIPTION

The LTC®2631 is a family of 12-, 10-, and 8-bit voltage-output DACs with an integrated, high accuracy, low-drift reference in an 8-lead TSOT-23 package. It has a rail-to-rail output buffer that is guaranteed monotonic.

The LTC2631-L has a full-scale output of 2.5V, and operates from a single 2.7V to 5.5V supply. The LTC2631-H has a full-scale output of 4.096V, and operates from a 4.5V to 5.5V supply. A 10ppm/°C reference output is available at the REF pin.

Each DAC can also operate in External Reference mode, in which a voltage supplied to the REF pin sets the full-scale output.

The LTC2631 DACs use a 2-wire, I²C-compatible serial interface. The LTC2631 operates in both the standard mode (clock rate of 100kHz) and the fast mode (clock rate of 400kHz).

The LTC2631 incorporates a power-on reset circuit. Op-tions are available for reset to zero-scale or reset to mid-scale after power-up.

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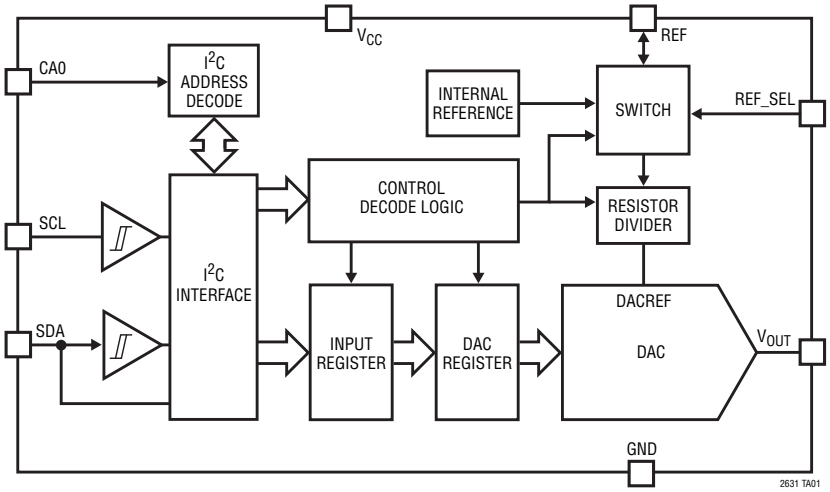
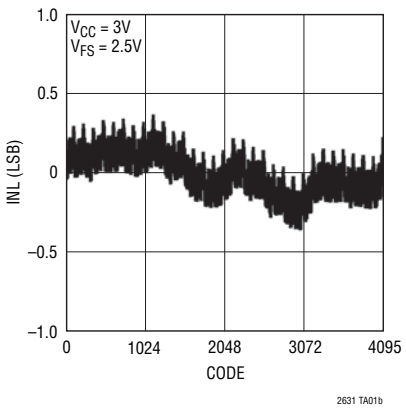
BLOCK DIAGRAM (LTC2631-M)



Integral Nonlinearity (LTC2631A-LM12)



ABSOLUTE MAXIMUM RATINGS

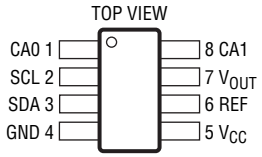
(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 6V
REF_SEL, SCL, SDA ..... –0.3V to 6V
V_{OUT}, CA0, CA1, REF ..... –0.3V to Min(V_{CC} + 0.3V, 6V)
Operating Temperature Range
  LTC2631C ..... 0°C to 70°C
  LTC2631I ..... –40°C to 85°C
  LTC2631H (Note 3) ..... –40°C to 125°C

Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

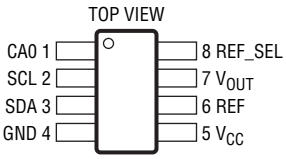
PIN CONFIGURATION

LTC2631-Z



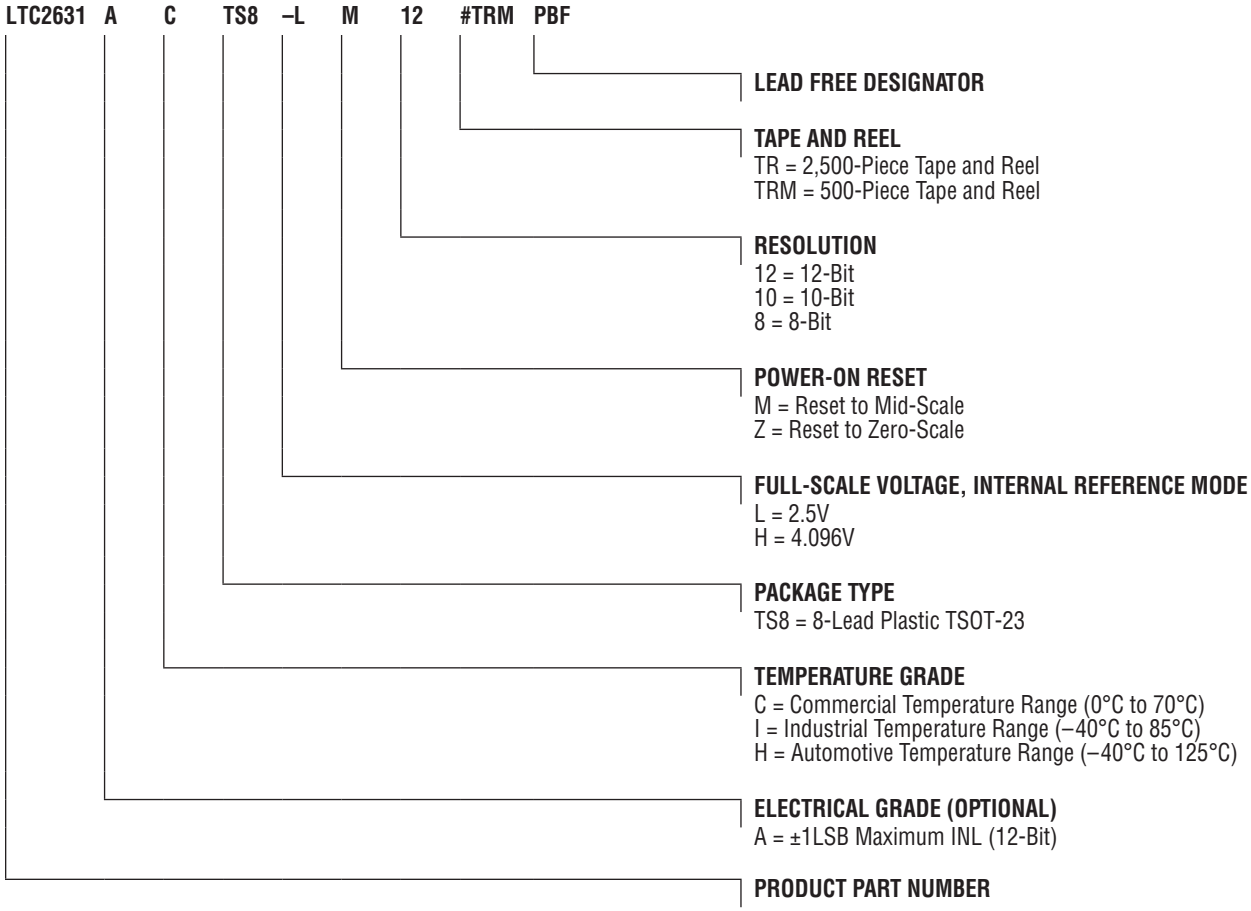
TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C (NOTE 6), θ_{JA} = 195°C/W

LTC2631-M



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C (NOTE 6), θ_{JA} = 195°C/W

ORDER INFORMATION



Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

PRODUCT SELECTION GUIDE

PART NUMBER	PART MARKING*	V_{FS} WITH INTERNAL REFERENCE	POWER-ON RESET TO CODE	PIN 8	RESOLUTION	V_{CC}	MAXIMUM INL
LTC2631A-LM12	LTDHF	2.5V • (4095/4096)	Mid-Scale	REF_SEL	12-Bit	2.7V – 5.5V	±1LSB
LTC2631A-LZ12	LTDHG	2.5V • (4095/4096)	Zero	CA1	12-Bit	2.7V – 5.5V	±1LSB
LTC2631A-HM12	LTDHH	4.096V • (4095/4096)	Mid-Scale	REF_SEL	12-Bit	4.5V – 5.5V	±1LSB
LTC2631A-HZ12	LTDHJ	4.096V • (4095/4096)	Zero	CA1	12-Bit	4.5V – 5.5V	±1LSB
LTC2631-LM12	LTDHF	2.5V • (4095/4096)	Mid-Scale	REF_SEL	12-Bit	2.7V – 5.5V	±2.5LSB
LTC2631-LM10	LTDHK	2.5V • (1023/1024)	Mid-Scale	REF_SEL	10-Bit	2.7V – 5.5V	±1LSB
LTC2631-LM8	LTDHQ	2.5V • (255/256)	Mid-Scale	REF_SEL	8-Bit	2.7V – 5.5V	±0.5LSB
LTC2631-LZ12	LTDHG	2.5V • (4095/4096)	Zero	CA1	12-Bit	2.7V – 5.5V	±2.5LSB
LTC2631-LZ10	LTDHM	2.5V • (1023/1024)	Zero	CA1	10-Bit	2.7V – 5.5V	±1LSB
LTC2631-LZ8	LTDHR	2.5V • (255/256)	Zero	CA1	8-Bit	2.7V – 5.5V	±0.5LSB
LTC2631-HM12	LTDHH	4.096V • (4095/4096)	Mid-Scale	REF_SEL	12-Bit	4.5V – 5.5V	±2.5LSB
LTC2631-HM10	LTDHN	4.096V • (1023/1024)	Mid-Scale	REF_SEL	10-Bit	4.5V – 5.5V	±1LSB
LTC2631-HM8	LTDHS	4.096V • (255/256)	Mid-Scale	REF_SEL	8-Bit	4.5V – 5.5V	±0.5LSB
LTC2631-HZ12	LTDHJ	4.096V • (4095/4096)	Zero	CA1	12-Bit	4.5V – 5.5V	±2.5LSB
LTC2631-HZ10	LTDHP	4.096V • (1023/1024)	Zero	CA1	10-Bit	4.5V – 5.5V	±1LSB
LTC2631-HZ8	LTDHT	4.096V • (255/256)	Zero	CA1	8-Bit	4.5V – 5.5V	±0.5LSB

*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2631-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2631A-LM12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		LTC2631-8 MIN	LTC2631-8 TYP	LTC2631-8 MAX	LTC2631-10 MIN	LTC2631-10 TYP	LTC2631-10 MAX	LTC2631-12 MIN	LTC2631-12 TYP	LTC2631-12 MAX	LTC2631A-12 MIN	LTC2631A-12 TYP	LTC2631A-12 MAX	UNITS
DC Performance																
	Resolution		●	8			10			12			12			Bits
	Monotonicity	V_{CC} = 3V, Internal Ref. (Note 4)	●	8			10			12			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 4)	●			±0.5			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 4)	●		±0.05	±0.5		±0.2	±1		±1	±2.5		±0.5	±1	LSB
ZSE	Zero-Scale Error	V_{CC} = 3V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 3V, Internal Ref. (Note 5)	●		±0.5	±5		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 3V, Internal Ref. (Note 5)			±10			±10			±10			±10		µV/°C
FSE	Full-Scale Error	V_{CC} = 3V, Internal Ref. (Note 15)	●		±0.08	±0.4		±0.08	±0.4		±0.08	±0.4		±0.08	±0.4	%FSR
V_{FSTC}	Full-Scale Voltage Temperature Coefficient	V_{CC} = 3V, Internal Ref. (Note 10) C-Grade I-Grade H-Grade			 ±10 ±10 ±10			 ±10 ±10 ±10			 ±10 ±10 ±10			 ±10 ±10 ±10		 ppm/°C ppm/°C ppm/°C
	Load Regulation	Internal Ref., Mid-Scale, V_{CC} = 3V ±10%, –5mA ≤ I_{OUT} ≤ 5mA, V_{CC} = 5V ±10%, –10mA ≤ I_{OUT} ≤ 10mA	 ● ●		 0.009 0.009	 0.016 0.016		 0.035 0.035	 0.064 0.064		 0.14 0.14	 0.256 0.256		 0.14 0.14	 0.256 0.256	 LSB/mA LSB/mA
R_{OUT}	DC Output Impedance	Internal Ref., Mid-Scale, V_{CC} = 3V ±10%, –5mA ≤ I_{OUT} ≤ 5mA, V_{CC} = 5V ±10%, –10mA ≤ I_{OUT} ≤ 10mA	 ● ●		 0.09 0.09	 0.156 0.156		 0.09 0.09	 0.156 0.156		 0.09 0.09	 0.156 0.156		 0.09 0.09	 0.156 0.156	 Ω Ω

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	External Reference Internal Reference			0 to V_{REF} 0 to 2.5		V V
PSR	Power Supply Rejection	V_{CC} = 3V ±10% or 5V ±10%			–80		dB
I_{SC}	Short-Circuit Output Current (Note 6) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero-Scale; V_{OUT} shorted to V_{CC} Full-Scale; V_{OUT} shorted to GND	 ● ●		 27 –28	 48 –48	 mA mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current (Note 7)	V_{CC} = 3V, V_{REF} = 2.5V, External Reference V_{CC} = 3V, Internal Reference V_{CC} = 5V, V_{REF} = 2.5V, External Reference V_{CC} = 5V, Internal Reference	● ● ● ●		150 180 160 190	200 240 210 260	µA µA µA µA
I_{SD}	Supply Current in Power-Down Mode (Note 7)	V_{CC} = 5V, C-Grade, I-Grade V_{CC} = 5V, H-Grade	● ●		0.6 0.6	1.8 4	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2631-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2631A-LM12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance		●	160	190	220	kΩ
	Capacitance				7.5		pF
I_{REF}	Reference Current, Power-Down Mode	DAC Powered Down	●		0.005	0.1	µA
Reference Output							
	Output Voltage		●	1.240	1.250	1.260	V
	Reference Temperature Coefficient				±10		ppm/°C
	Output Impedance				0.5		kΩ
	Capacitive Load Driving				10		µF
	Short-Circuit Current	V_{CC} = 5.5V; REF Shorted to GND			2.5		mA
Digital I/O							
V_{IL}	Low Level Input Voltage (SDA and SCL)	(Note 14)	●	–0.5		$0.3V_{CC}$	V
V_{IH}	High Level Input Voltage (SDA and SCL)	(Note 11)	●	$0.7V_{CC}$			V
$V_{IL(CAn)}$	Low Level Input Voltage on CA*n* (n = 0, 1)	See Test Circuit 1	●			$0.15V_{CC}$	V
$V_{IH(CAn)}$	High Level Input Voltage on CA*n* (n = 0, 1)	See Test Circuit 1	●	$0.85V_{CC}$			V
R_{INH}	Resistance from CA*n* (n = 0, 1) to V_{CC} to Set CA*n* = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CA*n* (n = 0, 1) to GND to Set CA*n* = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA*n* (n = 0, 1) to V_{CC} or GND to Set CA*n* = Float	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current = 3mA	●	0		0.4	V
t_{OF}	Output Fall Time	$V_O = V_{IH(MIN)}$ to $V_O = V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 12)	●	$20 + 0.1C_B$		250	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	$0.1V_{CC} \le V_{IN} \le 0.9V_{CC}$	●			±1	µA
C_{IN}	I/O Pin Capacitance	(Note 8)	●			10	pF
C_B	Capacitive Load for Each Bus Line		●			400	pF
C_{CAn}	External Capacitive Load on Address Pin CA*n* (n = 0, 1)		●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2631-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2631A-LM12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
t_S	Settling Time	V_{CC} = 3V (Note 9) ±0.39% (±1LSB at 8-Bits) ±0.098% (±1LSB at 10-Bits) ±0.024% (±1LSB at 12-Bits)			 3.2 3.8 4.1		 µs µs µs
	Voltage-Output Slew Rate				1		V/µs
	Capacitance Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			2.1		nV•s
	Multiplying Bandwidth	External Reference			300		kHz
e_n	Output Voltage Noise Density	At f = 1kHz, External Reference At f = 10kHz, External Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			140 130 160 150		$nV\sqrt{Hz}$ $nV\sqrt{Hz}$ $nV\sqrt{Hz}$ $nV\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz, External Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, External Reference 0.1Hz to 200kHz, Internal Reference, C_{REF} = 0.33µF			20 20 650 670		μV_{P-P} μV_{P-P} μV_{P-P} μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V. (See Figure 1) (Note 13).

LTC2631-LM12/-LM10/-LM8/-LZ12/-LZ10/-LZ8, LTC2631A-LM12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time of Both SDA and SCL Signals	(Note 12)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time of Both SDA and SCL Signals	(Note 12)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2631-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2631A-HM12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		LTC2631-8 MIN	LTC2631-8 TYP	LTC2631-8 MAX	LTC2631-10 MIN	LTC2631-10 TYP	LTC2631-10 MAX	LTC2631-12 MIN	LTC2631-12 TYP	LTC2631-12 MAX	LTC2631A-12 MIN	LTC2631A-12 TYP	LTC2631A-12 MAX	UNITS
DC Performance																
	Resolution		●	8			10			12			12			Bits
	Monotonicity	V_{CC} = 5V, Internal Ref. (Note 4)	●	8			10			12			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 5V, Internal Ref. (Note 4)	●			±0.5			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 5V, Internal Ref. (Note 4)	●		±0.05	±0.5		±0.2	±1		±1	±2.5		±0.5	±1	LSB
ZSE	Zero-Scale Error	V_{CC} = 5V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 5V, Internal Ref. (Note 5)	●		±0.5	±5		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 5V, Internal Ref. (Note 5)			±10			±10			±10			±10		µV/°C
FSE	Full-Scale Error	V_{CC} = 5V, Internal Ref. (Note 15)	●		±0.08	±0.4		±0.08	±0.4		±0.08	±0.4		±0.08	±0.4	%FSR
V_{FSTC}	Full-Scale Voltage Temperature Coefficient	V_{CC} = 5V, Internal Ref. (Note 10) C-Grade I-Grade H-Grade			 ±10 ±10 ±10			 ±10 ±10 ±10			 ±10 ±10 ±10			 ±10 ±10 ±10		 ppm/°C ppm/°C ppm/°C
	Load Regulation	V_{CC} = 5V ±10%, Internal Ref. Mid-Scale, –10mA ≤ I_{OUT} ≤ 10mA	●		0.006	0.01		0.022	0.04		0.09	0.16		0.09	0.16	LSB/mA
R_{OUT}	DC Output Impedance	V_{CC} = 5V ±10%, Internal Ref. Mid-Scale, –10mA ≤ I_{OUT} ≤ 10mA	●		0.09	0.156		0.09	0.156		0.09	0.156		0.09	0.156	Ω

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	External Reference Internal Reference			0 to V_{REF} 0 to 4.096		V V
PSR	Power Supply Rejection	V_{CC} = 5V ±10%			–80		dB
I_{SC}	Short-Circuit Output Current (Note 6) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero-Scale; V_{OUT} shorted to V_{CC} Full-Scale; V_{OUT} shorted to GND	 ● ●		 27 –28	 48 –48	 mA mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.5		5.5	V
I_{CC}	Supply Current (Note 7)	V_{CC} = 5V, V_{REF} = 4.096V, External Reference V_{CC} = 5V, Internal Reference	● ●		160 200	220 270	µA µA
I_{SD}	Supply Current in Power-Down Mode (Note 7)	V_{CC} = 5V, C-Grade, I-Grade V_{CC} = 5V, H-Grade	● ●		0.6 0.6	1.8 4	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2631-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2631A-HM12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance		●	160	190	220	kΩ
	Capacitance				7.5		pF
I_{REF}	Reference Current, Power-Down Mode	DAC Powered Down	●		0.005	0.1	µA
Reference Output							
	Output Voltage		●	2.032	2.048	2.064	V
	Reference Temperature Coefficient				±10		ppm/°C
	Output Impedance				0.5		kΩ
	Capacitive Load Driving				10		µF
	Short-Circuit Current	V_{CC} = 5.5V; REF Shorted to GND			4.3		mA
Digital I/O							
V_{IL}	Low Level Input Voltage (SDA and SCL)	(Note 14)	●	–0.5		$0.3V_{CC}$	V
V_{IH}	High Level Input Voltage (SDA and SCL)	(Note 11)	●	$0.7V_{CC}$			V
$V_{IL(CAn)}$	Low Level Input Voltage on CA*n* (n = 0, 1)	See Test Circuit 1	●			$0.15V_{CC}$	V
$V_{IH(CAn)}$	High Level Input Voltage on CA*n* (n = 0, 1)	See Test Circuit 1	●	$0.85V_{CC}$			V
R_{INH}	Resistance from CA*n* (n = 0, 1) to V_{CC} to Set CA*n* = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CA*n* (n = 0, 1) to GND to Set CA*n* = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA*n* (n = 0, 1) to V_{CC} or GND to Set CA*n* = Float	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current = 3mA	●	0		0.4	V
t_{OF}	Output Fall Time	$V_O = V_{IH(MIN)}$ to $V_O = V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 12)	●	$20 + 0.1C_B$		250	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	$0.1V_{CC} \le V_{IN} \le 0.9V_{CC}$	●			±1	µA
C_{IN}	I/O Pin Capacitance	(Note 8)	●			10	pF
C_B	Capacitive Load for Each Bus Line		●			400	pF
C_{CAn}	External Capacitive Load on Address Pin CA*n* (n = 0, 1)		●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2631-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2631A-HM12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
t_S	Settling Time	V_{CC} = 5V (Note 9) ±0.39% (±1LSB at 8-Bits) ±0.098% (±1LSB at 10-Bits) ±0.024% (±1LSB at 12-Bits)			 3.7 4.2 4.6		 µs µs µs
	Voltage-Output Slew Rate				1		V/µs
	Capacitance Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			3.0		nV•s
	Multiplying Bandwidth	External Reference			300		kHz
e_n	Output Voltage Noise Density	At f = 1kHz, External Reference At f = 10kHz, External Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			140 130 210 200		$nV\sqrt{Hz}$ $nV\sqrt{Hz}$ $nV\sqrt{Hz}$ $nV\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz, External Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, External Reference 0.1Hz to 200kHz, Internal Reference, C_{REF} = 0.33µF			20 20 650 670		μV_{P-P} μV_{P-P} μV_{P-P} μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V. (See Figure 1) (Note 13).

LTC2631-HM12/-HM10/-HM8/-HZ12/-HZ10/-HZ8, LTC2631A-HM12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time of Both SDA and SCL Signals	(Note 12)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time of Both SDA and SCL Signals	(Note 12)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND.

Note 3: High temperatures degrade operating lifetimes. Operating lifetime is derated at temperatures greater than 105°C.

Note 4: Linearity and monotonicity are defined from code k_L to code $2^N - 1$, where N is the resolution and k_L is given by $k_L = 0.016 \bullet (2^N / V_{FS})$, rounded to the nearest whole code. For V_{FS} = 2.5V and N = 12, k_L = 26 and linearity is defined from code 26 to code 4,095. For V_{FS} = 4.096V and N = 12, k_L = 16 and linearity is defined from code 16 to code 4,095.

Note 5: Inferred from measurement at code 16 (LTC2631-12), code 4 (LTC2631-10) or code 1 (LTC2631-8), and at full-scale.

Note 6: This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: Digital inputs at 0V or V_{CC}.

Note 8: Guaranteed by design and not production tested.

Note 9: Internal Reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 100pF to GND.

Note 10: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 11: Maximum $V_{IH} = V_{CC(MAX)} + 0.5V$

Note 12: C_B = capacitance of one bus line in pF

Note 13: All values refer to $V_{IH} = V_{IH(MIN)}$ and $V_{IL} = V_{IL(MAX)}$ levels.

Note 14: Minimum V_{IL} exceeds the Absolute Maximum rating. This condition won't damage the IC, but could degrade performance.

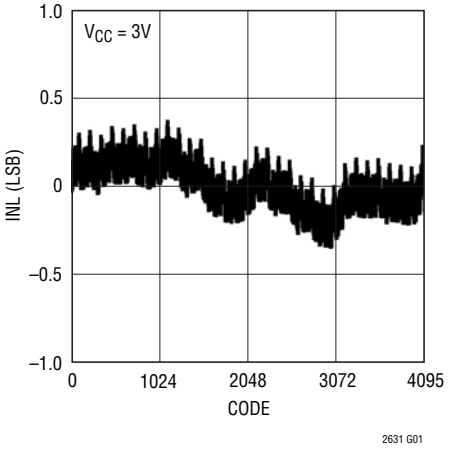
Note 15: Full-scale error is determined using the reference voltage measured at the REF pin.

TYPICAL PERFORMANCE CHARACTERISTICS

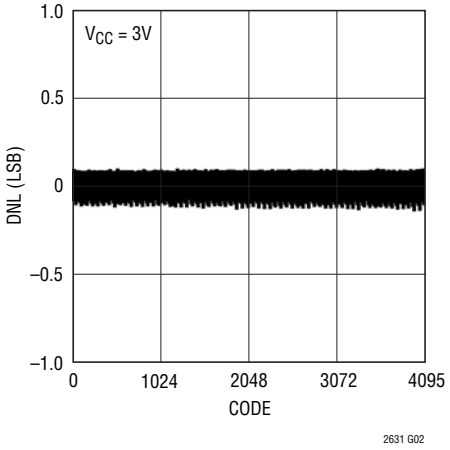
T_A = 25°C, unless otherwise noted.

LTC2631-L12 (Internal Reference, V_{FS} = 2.5V)

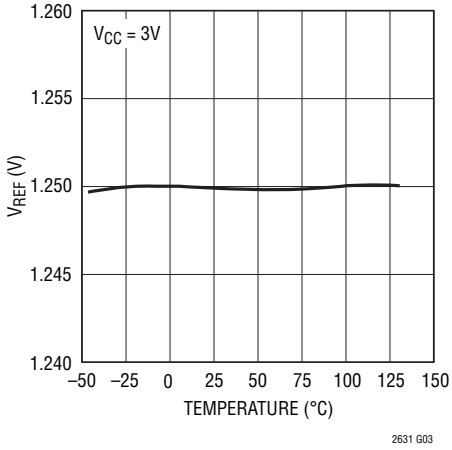
Integral Nonlinearity (INL)



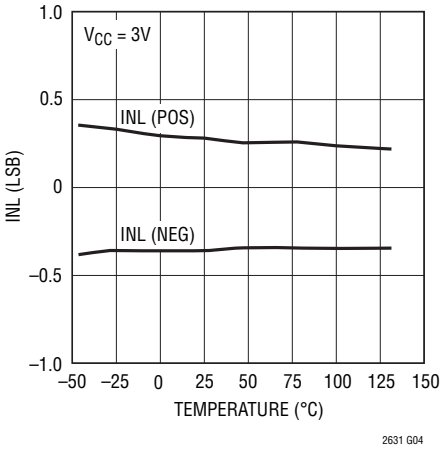
Differential Nonlinearity (DNL)



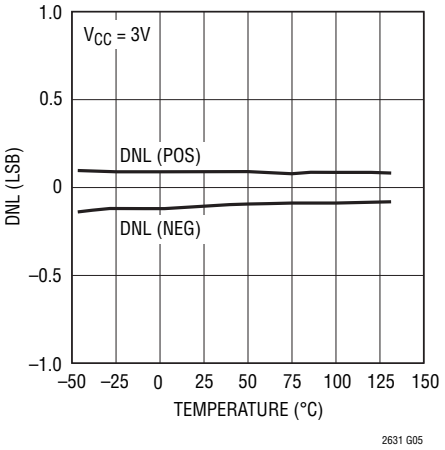
Reference Output Voltage vs Temperature



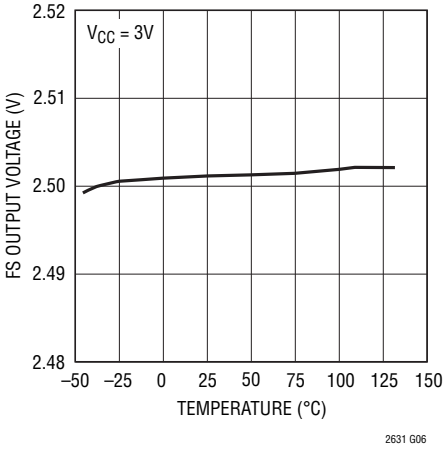
INL vs Temperature



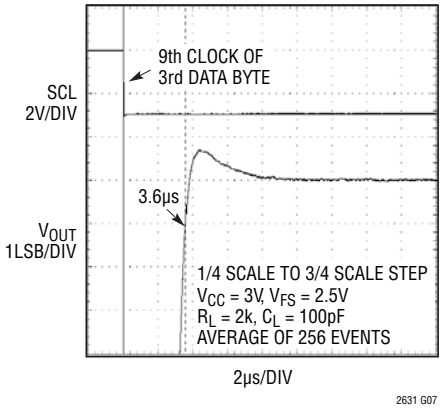
DNL vs Temperature



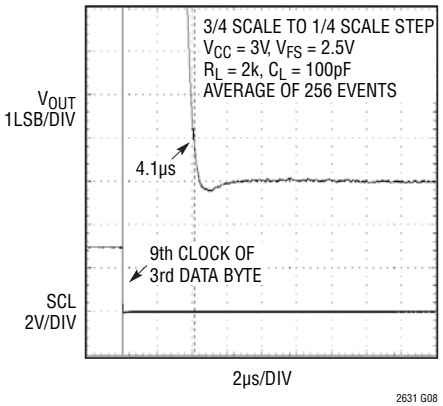
Full-Scale Output Voltage vs Temperature



Settling to ±1LSB



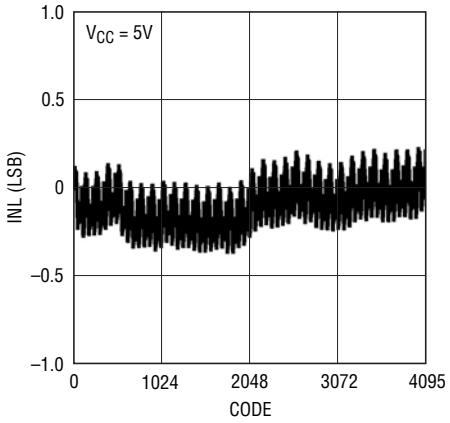
Settling to ±1LSB



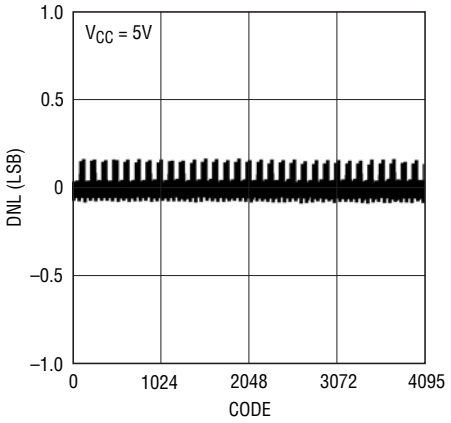
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LTC2631-H12 (Internal Reference, V_{FS} = 4.096V)

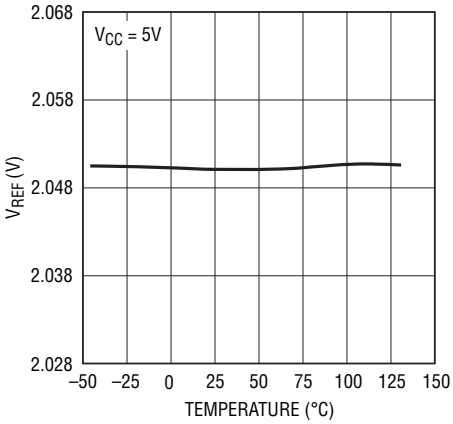
Integral Nonlinearity (INL)



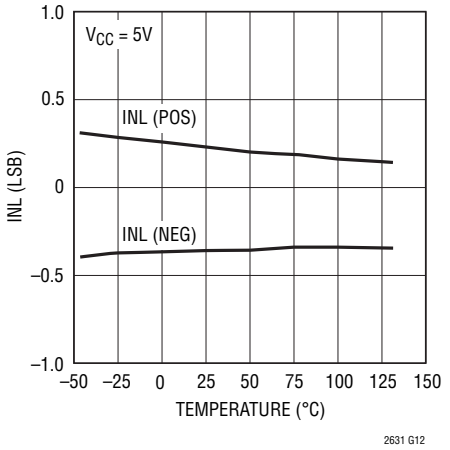
Differential Nonlinearity (DNL)



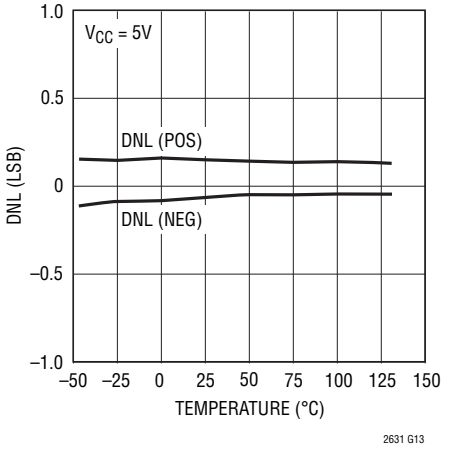
Reference Output Voltage vs Temperature



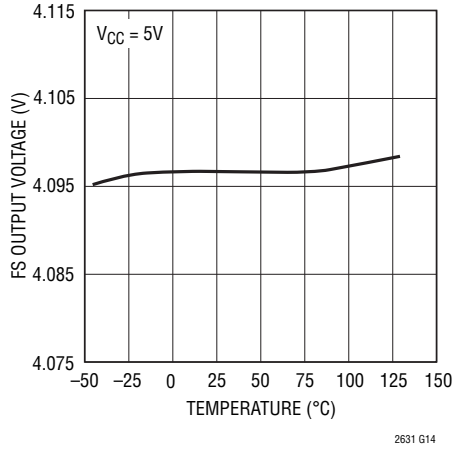
INL vs Temperature



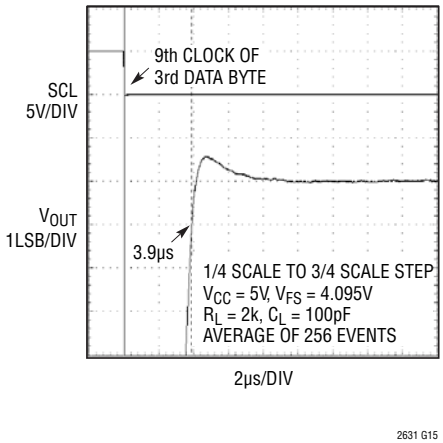
DNL vs Temperature



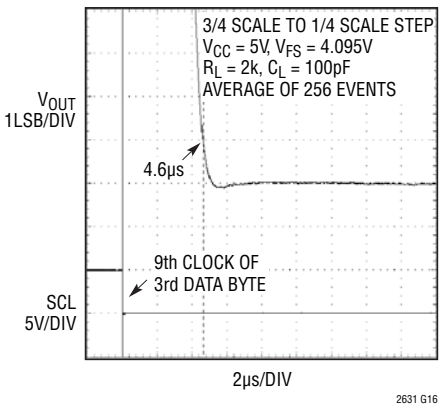
Full-Scale Output Voltage vs Temperature



Settling to ±1LSB



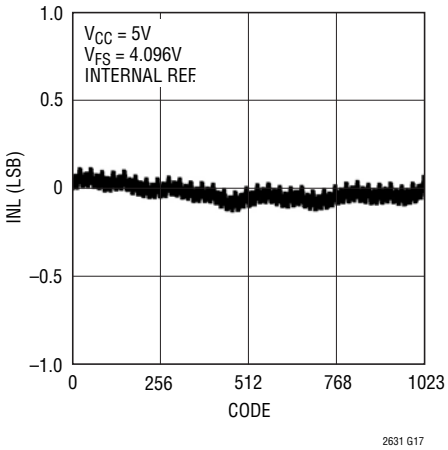
Settling to ±1LSB



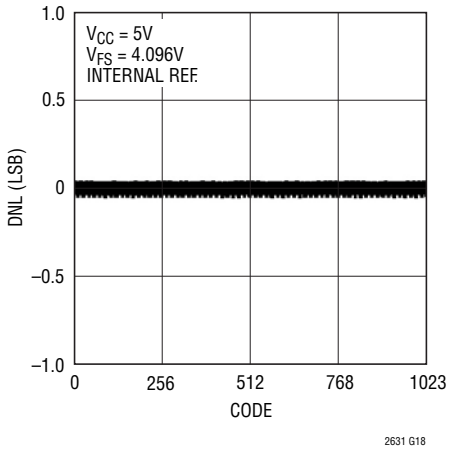
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LTC2631-10

Integral Nonlinearity (INL)

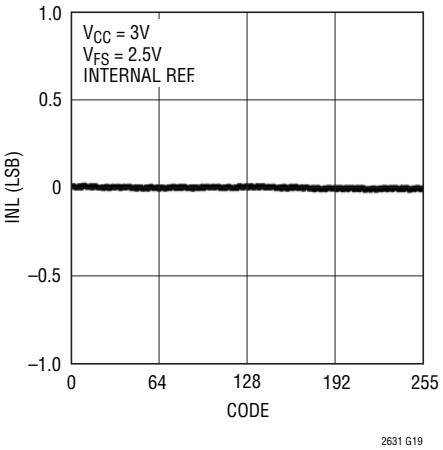


Differential Nonlinearity (DNL)

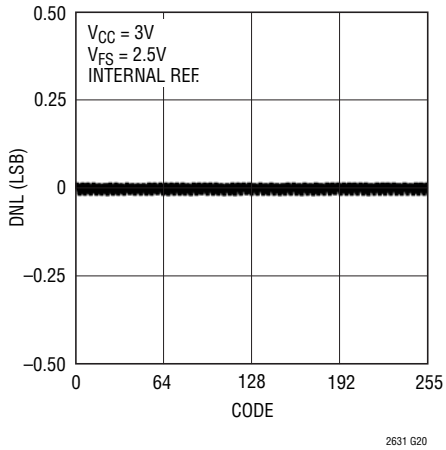


LTC2631-8

Integral Nonlinearity (INL)

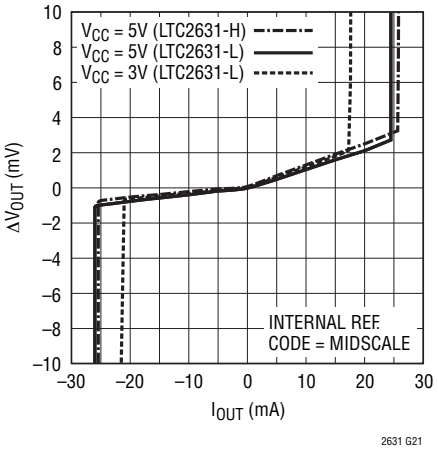


Differential Nonlinearity (DNL)

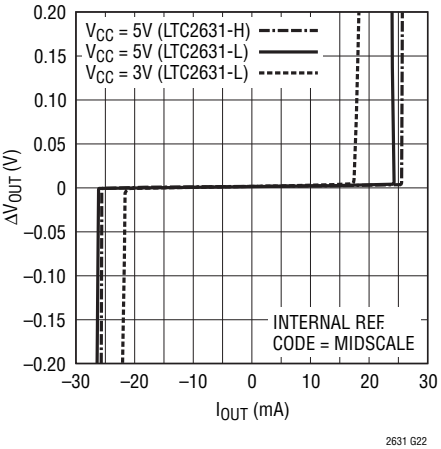


LTC2631

Load Regulation



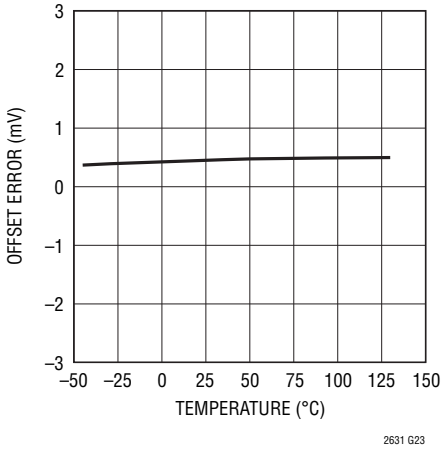
Current Limiting



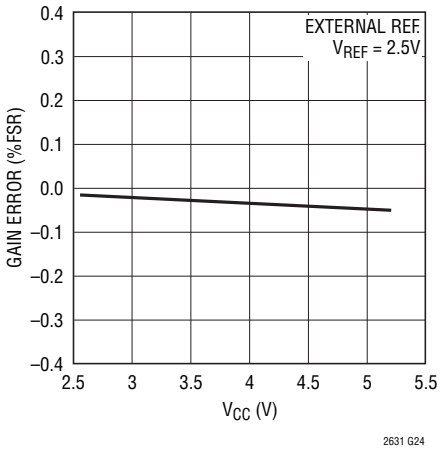
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LTC2631

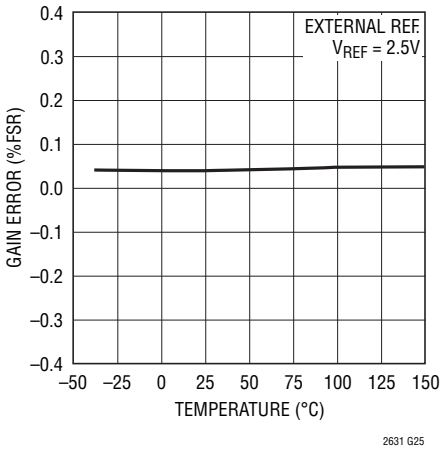
Offset Error vs Temperature



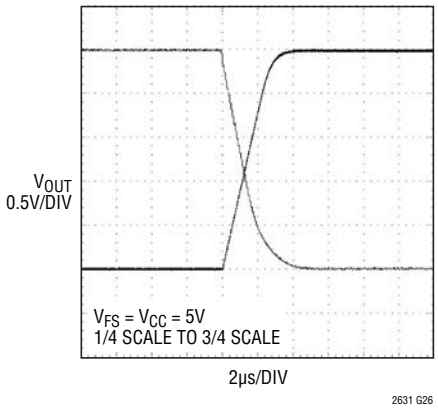
Gain Error vs V_{CC}



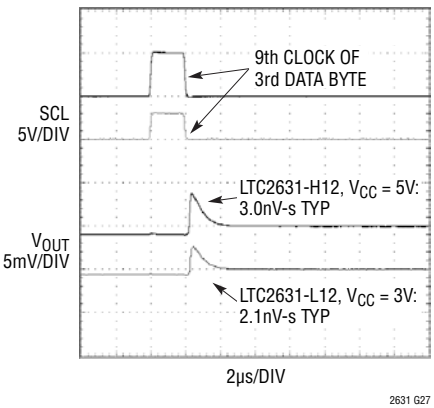
Gain Error vs Temperature



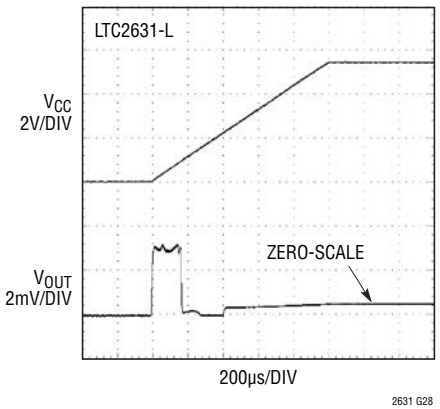
Large-Signal Response



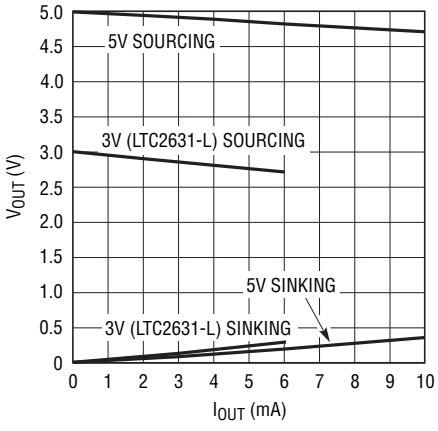
Mid-Scale-Glitch Impulse



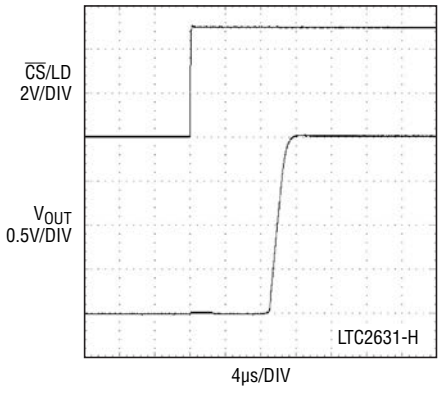
Power-On Reset Glitch



Headroom at Rails vs Output Current



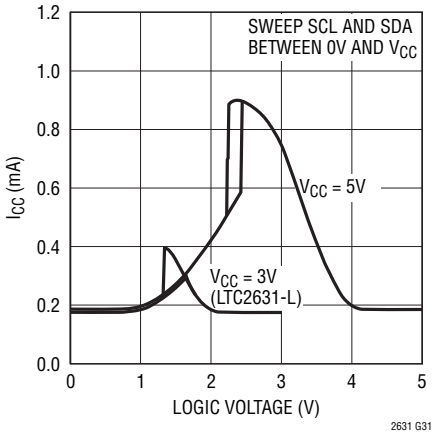
Exiting Power-Down to Mid-Scale



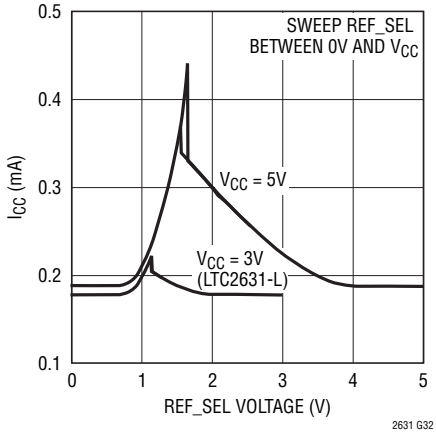
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LTC2631

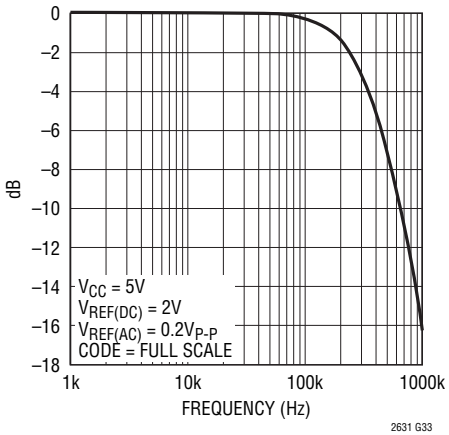
Supply Current vs Logic Voltage



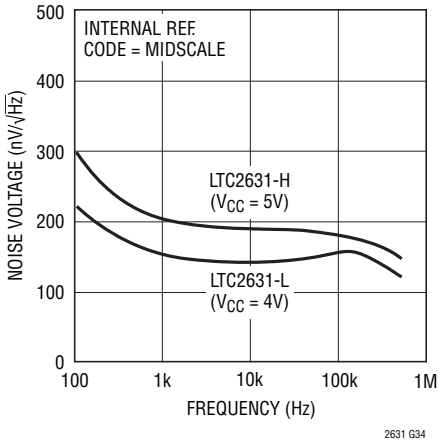
Supply Current vs REF_SEL Voltage



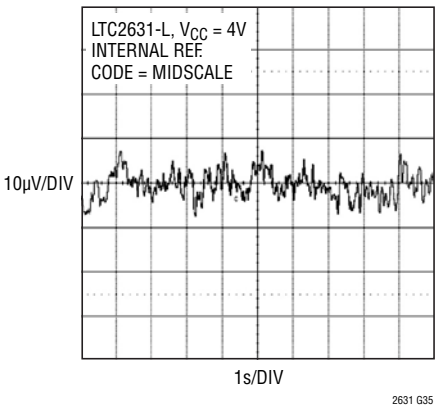
Multiplying Bandwidth



Noise Voltage vs Frequency



0.1Hz to 10Hz Voltage Noise



PIN FUNCTIONS

CA0 (Pin 1): Chip Address Bit 0. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (see Tables 1 and 2).

SCL (Pin 2): Serial Clock Input Pin. Data is shifted into the SDA pin at the rising edges of the clock. This high impedance pin requires a pull-up resistor or current source to V_{CC}.

SDA (Pin 3): Serial Data Bidirectional Pin. Data is shifted into the SDA pin and acknowledged by the SDA pin. This pin is high impedance while data is shifted in. Open-drain N-channel output during acknowledgment. SDA requires a pull-up resistor or current source to V_{CC}.

GND (Pin 4): Ground.

V_{CC} (Pin 5): Supply Voltage Input. 2.7V ≤ V_{CC} ≤ 5.5V (LTC2631-L) or 4.5V ≤ V_{CC} ≤ 5.5V (LTC2631-H). Bypass to GND with a 0.1µF capacitor.

REF (Pin 6): Reference Voltage Input or Output. When External Reference mode is selected, REF is an input (0V ≤ V_{REF} ≤ V_{CC}) where the voltage supplied sets the full-scale voltage. When Internal Reference is selected, the 10ppm/°C 1.25V (LTC2631-L) or 2.048V (LTC2631-H) internal reference is available at the pin. This output may be bypassed to GND with up to 10µF (0.33µF is recommended), and must be buffered when driving external DC load current.

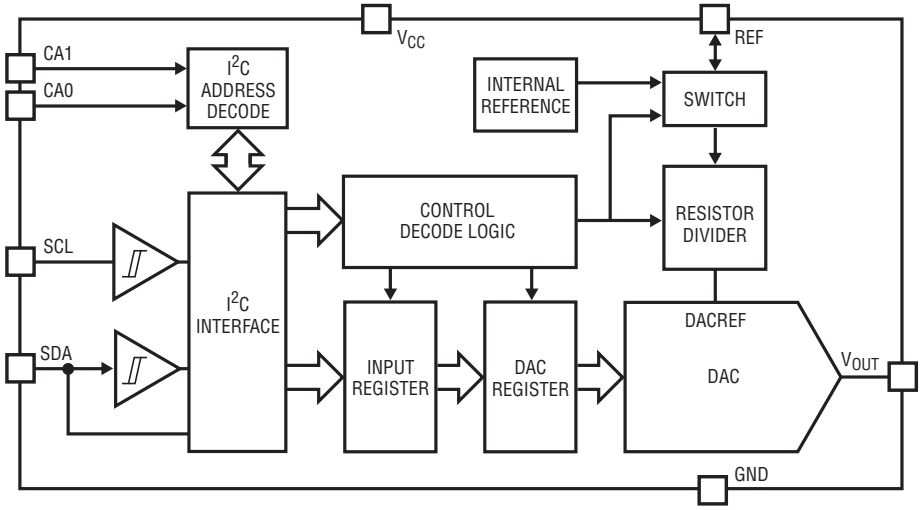
V_{OUT} (Pin 7): DAC Analog Voltage Output.

CA1 (Pin 8, LTC2631-Z): Chip Address Bit 1. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (see Table 1).

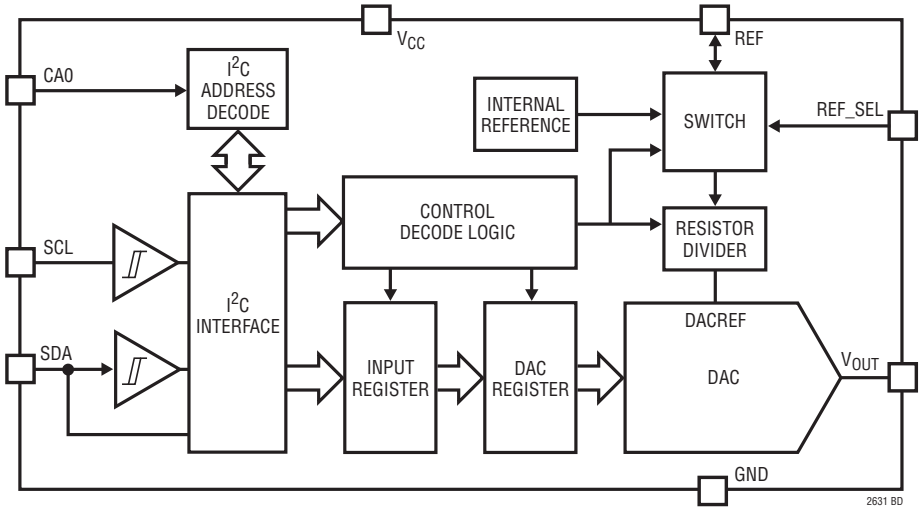
REF_SEL (Pin 8, LTC2631-M): Selects default Reference at power up. Tie to V_{CC} to select the Internal Reference, or GND to select an External Reference. After power-up, the logic state at this pin is ignored and the reference may be changed only by software command.

BLOCK DIAGRAMS

LTC2631-Z



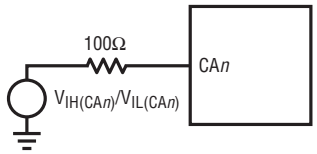
LTC2631-M



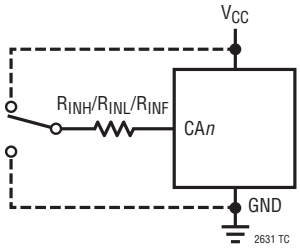
TEST CIRCUITS

Test Circuits for I²C Digital I/O (See Electrical Characteristics)

Test Circuit 1



Test Circuit 2



TIMING DIAGRAMS

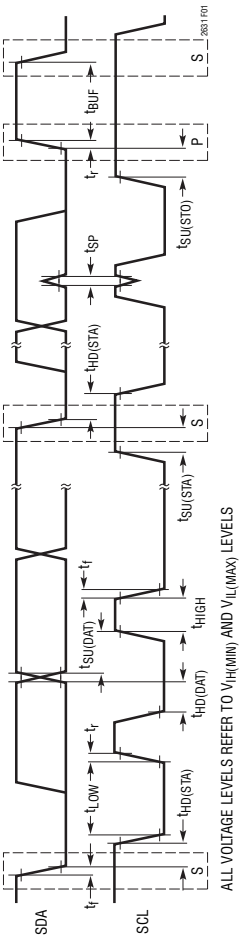


Figure 1. Serial Interface Timing

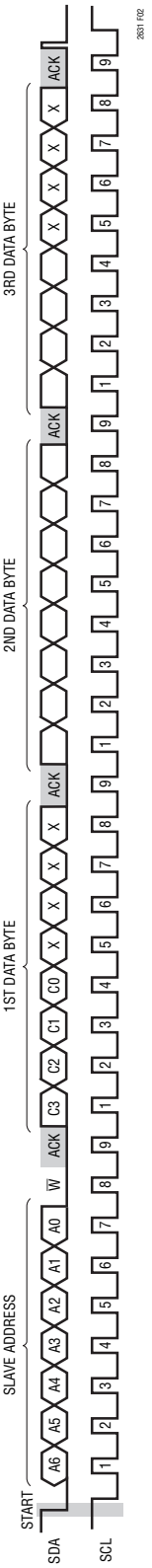


Figure 2. Typical LTC2631 Write Transaction

OPERATION

The LTC2631 is a family of single voltage-output DACs in 8-lead ThinSOT packages. Each DAC can operate rail-to-rail using an external reference, or with its full-scale voltage set by an integrated reference. Twelve combinations of accuracy (12-, 10-, and 8-bit), power-on reset value (zero or mid-scale), and full-scale voltage (2.5V or 4.096V) are available. The LTC2631 is controlled using a 2-wire I^2C interface.

Power-On Reset

The LTC2631-HZ/LTC2631-LZ clear the output to zero-scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2631 contains circuitry to reduce the power-on glitch: the analog output typically rises less than 5mV above zero-scale during power on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased. See "Power-On Reset Glitch" in the Typical Performance Characteristics section.

The LTC2631-HM/LTC2631-LM provide an alternative reset, setting the output to mid-scale when power is first applied.

Default reference mode selection is described in the Reference Modes section.

Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 5) is in transition.

Transfer Function

The digital-to-analog transfer function is

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right) V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution, and V_{REF} is either 2.5V (LTC2631-LM/LTC2631-LZ) or 4.096V (LTC2631-HM/LTC2631-HZ) when in Internal Reference mode, and the voltage at REF (Pin 6) when in External Reference mode.

I^2C Serial Interface

The LTC2631 communicates with a host using the standard 2-wire I^2C interface. The Timing Diagrams (Figures 1 and 2) show the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The value of these pull-up resistors is dependent on the power supply and can be obtained from the I^2C specifications. For an I^2C bus operating in the fast mode, an active pull-up will be necessary if the bus capacitance is greater than 200pF.

The LTC2631 is a receive-only (slave) device. The master can write to the LTC2631. The LTC2631 does not respond to a read from the master.

START (S) and STOP (P) Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a communication to a slave device by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high.

When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave lets the master know that the latest byte of information was properly received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock pulse. The slave-receiver must pull down the SDA bus line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse. The LTC2631 responds to a write by a master

OPERATION

in this manner but does not acknowledge a read operation; in that case, SDA is retained HIGH during the period of the Acknowledge clock pulse.

Chip Address

The state of pins CA0 and CA1 (LTC2631-HZ/LTC2631-LZ) determines the slave address of the part. These pins can each be set to any one of three states: V_{CC}, GND or float. This results in nine (LTC2631-HZ/LTC2631-LZ) or three (LTC2631-HM/LTC2631-LM) selectable addresses for the part. The slave address assignments are shown in Tables 1 and 2.

Table 1. Slave Address Map (LTC2631-Z)

CA1	CA0	A6	A5	A4	A3	A2	A1	A0
GND	GND	0	0	1	0	0	0	0
GND	FLOAT	0	0	1	0	0	0	1
GND	V_{CC}	0	0	1	0	0	1	0
FLOAT	GND	0	0	1	0	0	1	1
FLOAT	FLOAT	0	1	0	0	0	0	0
FLOAT	V_{CC}	0	1	0	0	0	0	1
V_{CC}	GND	0	1	0	0	0	1	0
V_{CC}	FLOAT	0	1	0	0	0	1	1
V_{CC}	V_{CC}	0	1	1	0	0	0	0
GLOBAL ADDRESS		1	1	1	0	0	1	1

Table 2. Slave Address Map (LTC2631-M)

CA0	A6	A5	A4	A3	A2	A1	A0
GND	0	0	1	0	0	0	0
FLOAT	0	0	1	0	0	0	1
V_{CC}	0	0	1	0	0	1	0
GLOBAL ADDRESS	1	1	1	0	0	1	1

In addition to the address selected by the address pins, the part also responds to a global address. This address allows a common write to all LTC2631 parts to be accomplished using one 3-byte write transaction on the I^2C bus. The global address, listed at the end of Tables 1 and 2, is a 7-bit hardwired address not selectable by CA0/CA1. If another address is required, please consult the factory.

The maximum capacitive load allowed on the CA0/CA1 address pins is 10pF, as these pins are driven during address detection to determine if they are floating.

Write Word Protocol

The master initiates communication with the LTC2631 with a START condition and a 7-bit slave address followed by the Write bit ($\overline{W}$) = 0. The LTC2631 acknowledges by pulling the SDA pin low at the ninth clock if the 7-bit slave address matches the address of the part (set by CA0/CA1) or the global address. The master then transmits 3-bytes of data. The LTC2631 acknowledges each byte of data by pulling the SDA line low at the ninth clock of each data byte transmission. After receiving three complete bytes of data, the LTC2631 executes the command specified in the 24-bit input word.

If more than three data bytes are transmitted after a valid 7-bit slave address, the LTC2631 does not acknowledge the extra bytes of data (SDA is high during the 9th clock).

The format of the three data bytes is shown in Figure 3. The first byte of the input word consists of the 4-bit command, followed by four don't-cares bits. The next two bytes contain the 16-bit data word, which consists of the 12-, 10- or 8-bit input code, MSB to LSB, followed by 4, 6 or 8 don't-cares bits (LTC2631-12, LTC2631-10 and LTC2631-8 respectively). A typical LTC2631 write transaction is shown in Figure 4.

The command bit assignments (C3-C0) are shown in Table 3. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register. In an update operation, the data word is copied from the input register to the DAC register and converted to an analog voltage at the DAC output. The update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

OPERATION

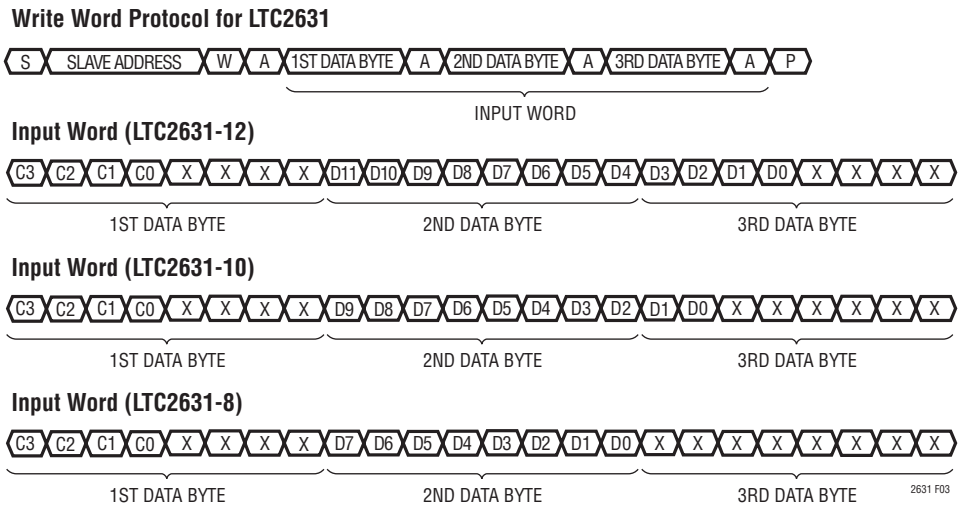


Figure 3. Command and Data Input Format

Table 3. Command Codes

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register
0	0	0	1	Update (Power Up) DAC Register
0	0	1	1	Write to and Update (Power Up) DAC Register
0	1	0	0	Power Down
0	1	1	0	Select Internal Reference
0	1	1	1	Select External Reference

*Command codes not shown are reserved and should not be used.

Reference Modes

For applications where an accurate external reference is not available, the LTC2631 has a user-selectable, integrated reference. The LTC2631-LM/LTC2631-LZ provide a full-scale output of 2.5V. The LTC2631-HM/LTC2631-HZ provide a full-scale output of 4.096V. The internal reference can be useful in applications where the supply voltage is poorly regulated. Internal Reference mode can be selected by using command 0110, and is the power-on default for LTC2631-HZ/LTC2631-LZ, as well as for LTC2631-HM/LTC2631-LM when REF_SEL is tied high.

The 10ppm/°C, 1.25V (LTC2631-LM/LTC2631-LZ) or 2.048V (LTC2631-HM/LTC2631-HZ) internal reference is available at the REF pin. Adding bypass capacitance to the REF pin will improve noise performance; 0.33µF is recommended, and up to 10µF can be driven without oscillation. This output must be buffered when driving external DC load current.

Alternatively, the DAC can operate in External Reference mode using command 0111. In this mode, an input voltage supplied externally to the REF pin provides the reference ($0V \le V_{REF} \le V_{CC}$) and the supply current is reduced. External Reference mode is the power-on default for LTC2631-HM/LTC2631-LM when REF_SEL is tied low.

The reference mode of LTC2631-HZ/LTC2631-LZ can be changed only by software command. The same is true for LTC2631-HM/LTC2631-LM after power-on, after which the logic state on REF_SEL is ignored.

Power-Down Mode

For power-constrained applications, the LTC2631's power-down mode can be used to reduce the supply current whenever the DAC output is not needed. When in power down, the buffer amplifier, bias circuit, and reference circuit are disabled and draw essentially zero current. The DAC output is put into a high-impedance state, and the output pin is passively pulled to ground through a 200kΩ resistor. Input and DAC register contents are not disturbed during power down.

OPERATION

The DAC can be put into power-down mode by using command 0100. The supply current is reduced to 1.8µA maximum (C and I grades) and the REF pin becomes high impedance (typically > 1GΩ).

Normal operation resumes after executing any command that includes a DAC update, as shown in Table 3. The DAC is powered up and its voltage output is updated. Normal settling is delayed while the bias, reference, and amplifier circuits are re-enabled. When the REF pin output is bypassed to GND with 1nF or less, the power-up delay time is 20µs for settling to 12-bits. This delay increases to 200µs for 0.33µF, and 10ms for 10µF.

Voltage Output

The LTC2631's integrated rail-to-rail amplifier has guaranteed load regulation when sourcing or sinking up to 10mA at 5V, and 5mA at 3V.

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load current. The measured change in output voltage per change in forced load current is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to ohms. The amplifier's DC output impedance is 0.1Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 50Ω typical channel resistance of the output devices (e.g., when sinking 1mA, the minimum output voltage is 50Ω • 1mA, or 50mV). See the graph "Headroom at Rails vs. Output Current" in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 500pF.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage-output device, the output is limited to voltages within the supply range.

Since the analog output of the DAC cannot go below ground, it may limit the lowest codes, as shown in Figure 5b. Similarly, limiting can occur near full-scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC}, as shown in Figure 5c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

Board Layout

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane. The resistance from the LTC2631 GND pin to the ground plane should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.1Ω). Note that the LTC2631 is no more susceptible to this effect than any other parts of this type; on the contrary, it allows layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Another technique for minimizing errors is to use a separate power ground return trace on another board layer. The trace should run between the point where the power supply is connected to the board and the DAC ground pin. Thus the DAC ground pin becomes the common point for analog ground, digital ground, and power ground. When the LTC2631 is sinking large currents, this current flows out the ground pin and directly to the power ground trace without affecting the analog ground plane voltage.

It is sometimes necessary to interrupt the ground plane to confine digital ground currents to the digital portion of the plane. When doing this, make the gap in the plane only as long as it needs to be to serve its purpose and ensure that no traces cross over the gap.

OPERATION

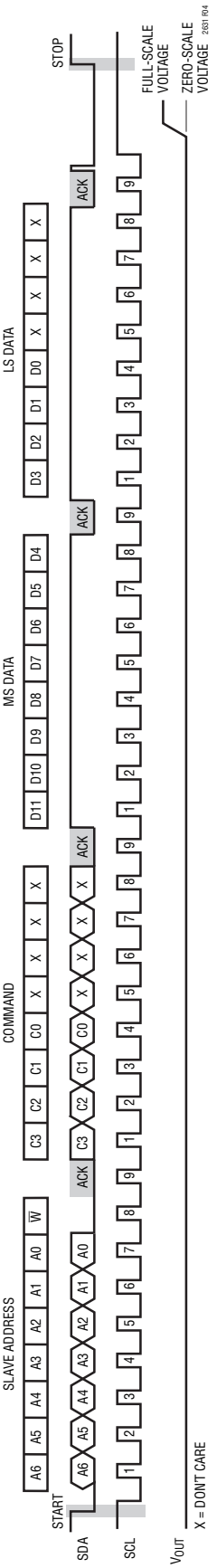


Figure 4. Typical LTC2631 Input Waveform—Programming 12-Bit DAC Output for Full-Scale

OPERATION

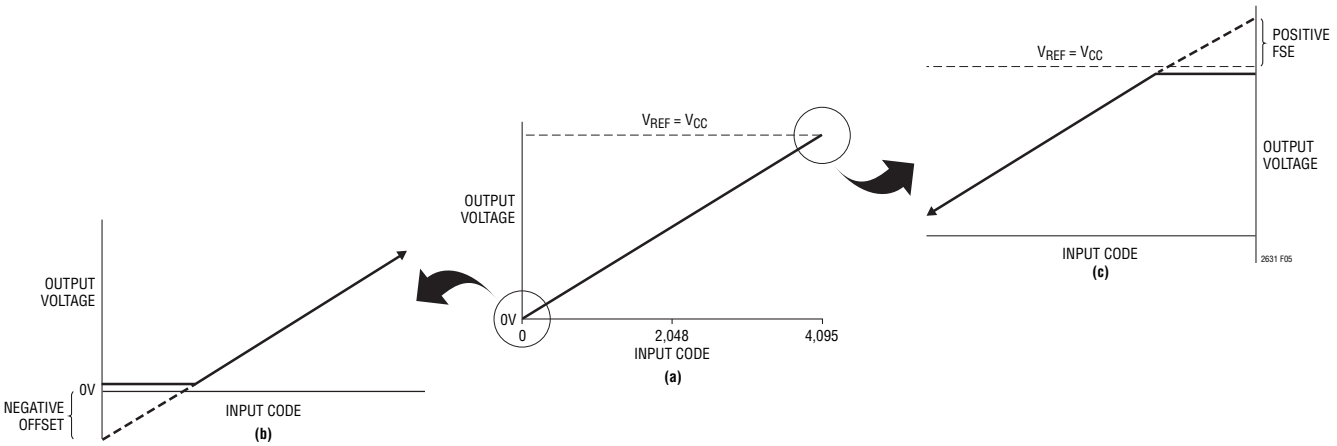
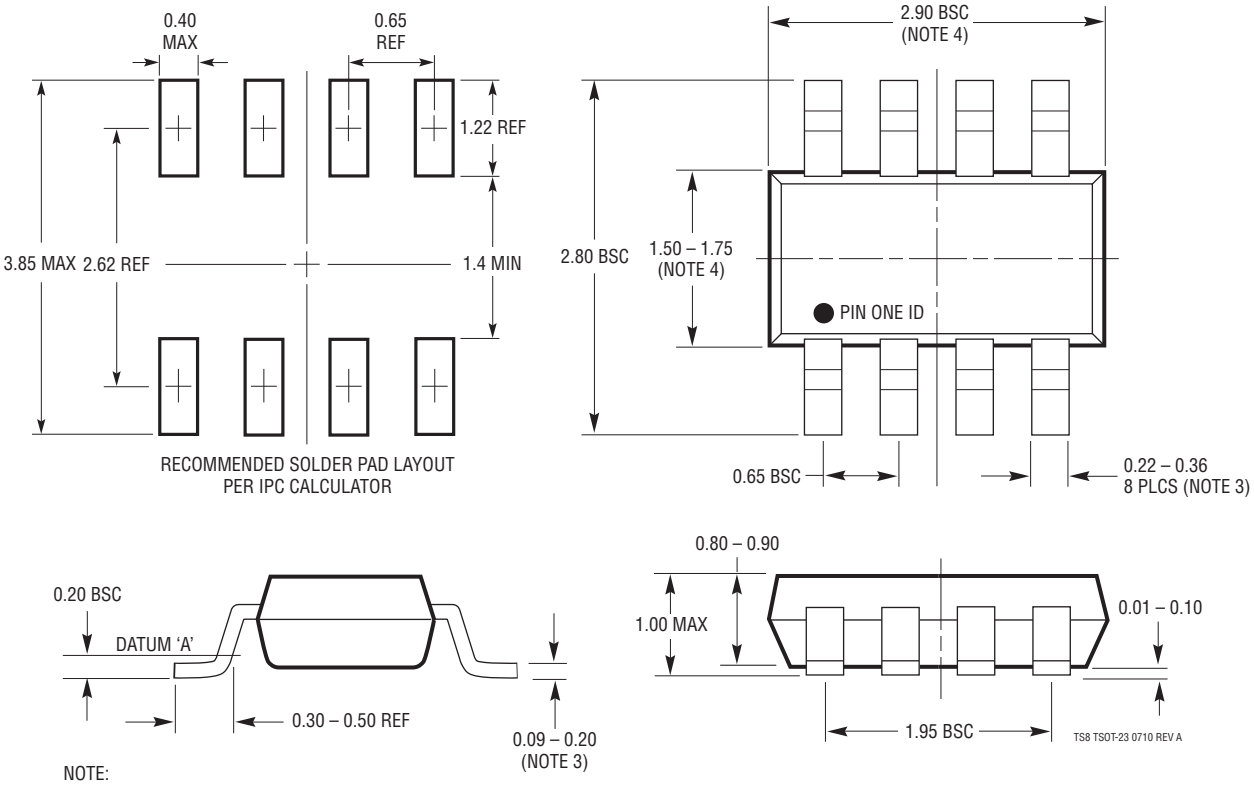


Figure 5. Effects of Rail-to-Rail Operation on a DAC Transfer Curve (Shown for 12-Bits)
(a) Overall Transfer Function
(b) Effect of Negative Offset for Codes Near Zero
(c) Effect of Positive Full-Scale Error for Codes Near Full-Scale

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

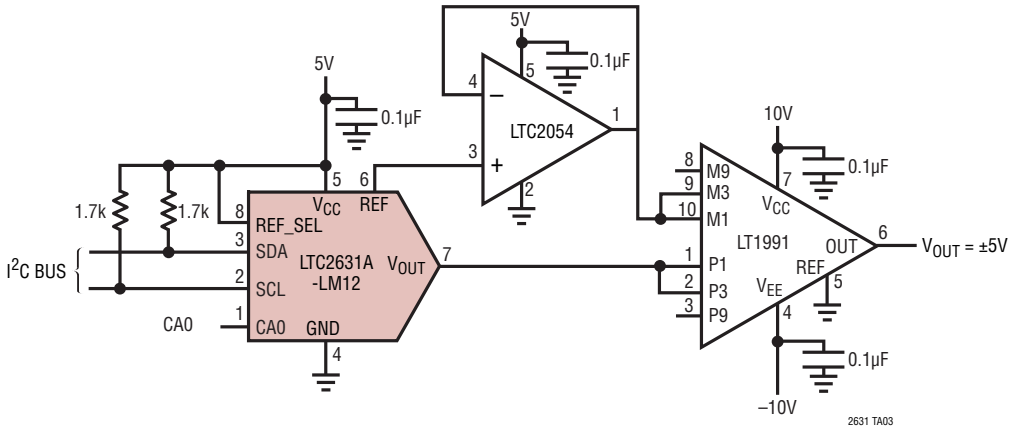
REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	11/13	Updated TS8 package drawing to Rev A	26

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Programmable ±5V Output



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1663	Single 10-Bit V_{OUT} DAC in SOT-23	V_{CC} = 2.7V to 5.5V, 60µA, Internal Reference, SMBus Interface
LTC1669	Single 10-Bit V_{OUT} DAC in SOT-23	V_{CC} = 2.7V to 5.5V, 60µA, Internal Reference, I^2C Interface
LTC2360/LT2362/ LTC2365/LTC2366	12-Bit SAR ADCs in TSOT23-6/TSOT23-8 Packages	100ksps/250ksps/500ksps/1Msps/3Msps Output Rates
LTC2450/LTC2452	16-Bit Single-Ended/Differential Delta Sigma ADCs	SPI Interface, Tiny DFN Packages, 60Hz Output Rate
LTC2451/LTC2453	16-Bit Single-Ended/Differential Delta Sigma ADCs	I^2C Interface, Tiny DFN and TSOT23-8 Packages, 60Hz Output Rate
LTC2600/LTC2610/LTC2620	Octal 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2601/LTC2611/LTC2621	Single 16-/14-/12-Bit V_{OUT} DACs in 10-Lead DFN	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2602/LTC2612/LTC2622	Dual 16-/14-/12-Bit V_{OUT} DACs in 8-Lead MSOP	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2604/LTC2614/LTC2624	Quad 16-/14-/12-Bit V_{OUT} DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2605/LTC2615/LTC2625	Octal 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, I^2C Interface
LTC2606/LTC2616/LTC2626	Single 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	270µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, I^2C Interface
LTC2609/LTC2619/LTC2629	Quad 16-/14-/12-Bit V_{OUT} DACs with I^2C Interface	250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output with Separate V_{REF} Pins for Each DAC
LTC2630	Single 12-/10-/8-Bit V_{OUT} DACs with 10ppm/°C Reference in SC70	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Rail-to-Rail Output, SPI Interface
LTC2640	Single 12-/10-/8-Bit SPI V_{OUT} DACs with 10ppm/°C Reference in ThinSOT	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Selectable External Reference Mode, Rail-to-Rail Output, SPI Interface

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