# M54122L

EARTH LEAKAGE CURRENT DETECTOR

## DESCRIPTION

The M54122L is a semiconductor integrated circuit with amplifier for a high-speed earth leakage circuit breaker.

## FEATURES

- Suitable for JIS C 8371
- Good temperature characteristics of input sensitivity current
- High input sensitivity ($V_T$ = 13.5mV Typ.)
- Low external component count
- High noise and surge-proof
- Low power dissipation ($P_d$ = 5mW Typ.) and may be used both as 100V and 200V.
- High mounting density by SIL package with 8 pins
- Wide temperature range (Ta = -20 – +80°C)

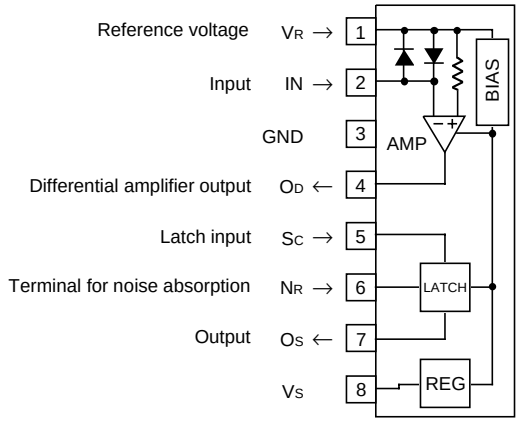
## APPLICATION

High speed earth leakage circuit breaker

## FUNCTION

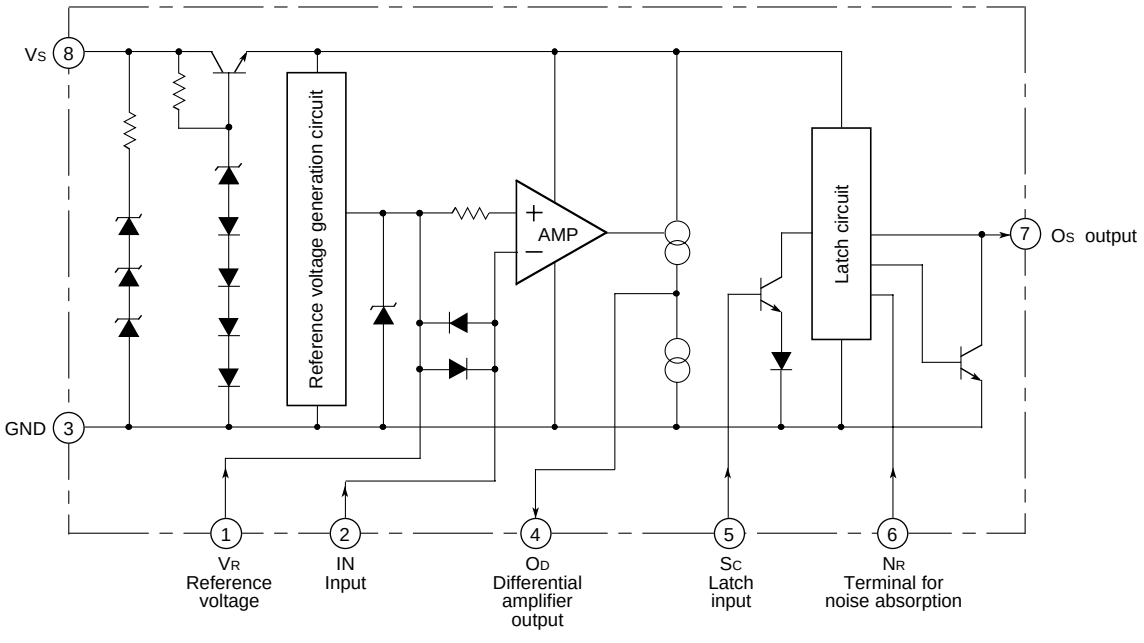
The M54122L circuit for the amplifying parts of earth leakage circuit breaker consists of differential amplifier, latch circuit and voltage regulator. It is connected to the secondary side of the zero-current transformer (ZCT) which detects leakage current in the both input of the differential amplifier. Signals amplified by differential amplifier are integrated by an external capacitor, and connects to the input terminal of latch circuit with output suitable for the characteristics of high-speed earth leakage circuit breaker. Latch circuit keeps low in the output till the input voltage reaches the fixed level, and output becomes high when the leakage current more than fixed flows. It drives a thyristor connected to the output terminal of latch circuit.

## PIN CONFIGURATION (TOP VIEW)




Outline 8P5

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (Ta = -20 – 80°C unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $I_S$ | Supply current | | 8 | mA |
| $I_{VR}$ | $V_R$ terminal current | Between $V_R$-IN (Note 1) | 250 | mA |
| | | Between $V_R$-GND | 30 | |
| | | Between IN-$V_R$ (Note 1) | -250 | |
| $I_{IN}$ | IN terminal current | Between IN-$V_R$ (Note 1) | 250 | mA |
| | | Between IN-GND | 30 | |
| | | Between $V_R$-IN (Note 1) | -250 | |
| $I_{SC}$ | Sc terminal current | | 5 | mA |
| $P_d$ | Power dissipation | | 200 | mW |
| $T_{opr}$ | Operating temperature | | -20 – 80 | °C |
| $T_{stg}$ | Storage temperature | | -55 – 125 | °C |

Note 1: Current value between $V_R$ and IN, and between IN and $V_R$ is less than 1ms in the pulse width, and duty cycle is less than 12%. In applying AC current continuously, it is 100mArms in the off-state.

Remarks: GND terminal (pin ③) of the circuit is a basis of all the voltages except differential input clamp voltage of DC electrical characteristics, and direction of current is plus (no signal) in flowing into the circuit and is minus (– signal) in flowing out of it. Maximum value and minimum one are shown as absolute value. Please don't apply voltage whose standard is GND terminal in $V_R$ and IN pin.

## RECOMMENDED OPERATING CONDITIONS (Ta = -20 – 80°C unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $V_S$ | Supply voltage when latch circuit is off-state. | 12 | | | V |
| $C_{VS}$ | External capacitor between $V_S$ and GND | 1 | | | μF |
| $C_{OS}$ | External capacitor between $O_S$ and GND | | | 1 | μF |

## ELECTRICAL CHARACTERISTICS (Ta = -20 – 80°C unless otherwise noted)

| Symbol | Parameter | Test conditions | | Tempera-ture(°C) | Test circuit | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Typ.* | Max. | |
| $I_{S1}$ | Supply current | $V_S$ = 12V, $V_R$-$V_I$ = 30mV | | -20 | 1 | | | 580 | μA |
| | | | | 25 | 1 | | 400 | 530 | |
| | | | | 80 | 1 | | | 480 | |
| $V_T$ | Trip voltage | $V_S$ = 16V, $V_R$-$V_I$ (Note 2) | | -20 – +80 | 2 | 10 | 13.5 | 17 | $mV_{rms}$ |
| $I_{TD1}$ | Timed current 1 | $V_S$ = 16V, $V_R$-$V_I$ = 30mV<br>$V_{OD}$ = 1.2V | | 25 | 3 | -12 | | -30 | μA |
| $I_{TD2}$ | Timed current 2 | $V_S$ = 16V, short circuit between $V_R$ and $V_I$, $V_{OD}$ = 0.8V | | 25 | 4 | 17 | | 37 | μA |
| $I_O$ | Output current | $V_{SC}$ = 1.4V<br>$V_{OS}$ = 0.8V | $I_{S1}$ = 580μA | -20 | 5 | -200 | | | μA |
| | | | $I_{S1}$ = 530μA | 25 | 5 | -100 | | | |
| | | | $I_{S1}$ = 480μA | 80 | 5 | -75 | | | |
| $V_{SC}$ "ON" | Sc ON voltage (Note 3) | $V_S$ = 16V | | 25 | 6 | 0.7 | | 1.4 | V |
| $I_{SC}$ "ON" | Sc input current | $V_S$ = 12V | | 25 | 7 | | | 5 | μA |
| $I_{OSL}$ | Output low-level current | $V_S$ = 12V, $V_{OSL}$ = 0.2V | | -20 – +80 | 8 | 200 | | | μA |
| $V_{IC}$ | Input clamp voltage | $V_S$ = 12V, $I_{IC}$ = 20mA | | -20 – +80 | 9 | 4.3 | | 6.7 | V |
| $V_{IDC}$ | Differential input clamp voltage | $I_{IDC}$ = 100mA | | -20 – +80 | 10 | 0.4 | | 2 | V |
| $V_{SM}$ | Maximum current voltage | $I_{SM}$ = 7mA | | 25 | 11 | 20 | | 28 | V |
| $I_{S2}$ | Supply current 2 (Note 4) | $V_R$-$V_I$ $V_{OS}$ = 0.6V (Note 5) | | -20 – +80 | 12 | | | 900 | μA |
| $V_S$ "OFF" | Latch circuit off-state supply voltage (Note 6) | | | 25 | 13 | 0.5 | | | V |
| $T_{ON}$ | Operating time (Note 7) | $V_S$ = 16V, $V_R$-$V_I$ = 0.3V | | 25 | 14 | 2 | | 4 | ms |

*: Typical values are at Ta = 25°C.

Note 2: When standard value of voltage (60Hz) between $V_R$ and $V_I$ is minimum, and output $O_S$ is low-level, or when standard value of voltage (60Hz) between $V_R$ and $V_I$ is maximum, and output $O_S$ is high-level, it is considered as a good one.

3: When standard value of voltage $V_{SC}$ "ON" is minimum, and output $O_S$ is low-level, or when standard value of voltage $V_{SC}$ "ON" is maximum, and output $O_S$ is high-level, it is considered as a good one.

4: Supply current 2 is necessary to keep high in output $O_S$.

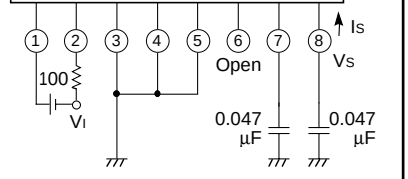
5: After applying 30mV between $V_R$ and $V_I$ and shorting between them, it is considered as a good one if standard value of $I_{GT}$ flows out of output $O_S$.

6: After supply voltage applies 12V and output $O_S$ is high-level, it is considered as a good one in the standard value of supply voltage and in the low-level of output $O_S$.

7: Operating time is a time from applying fixed input till operating latch circuit in 0.047μF between $O_D$ and GND.

## TEST CIRCUIT

1

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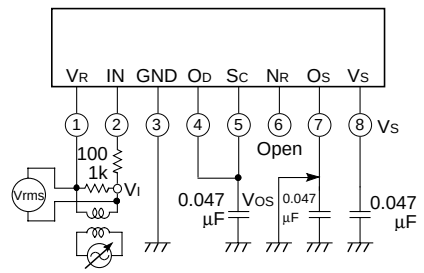


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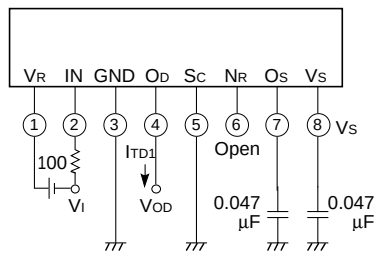


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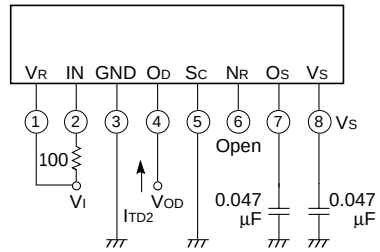


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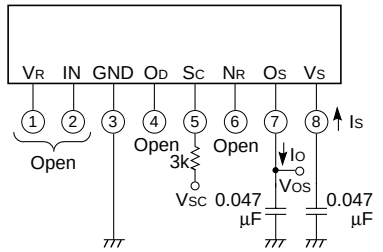


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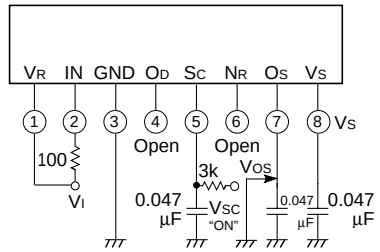


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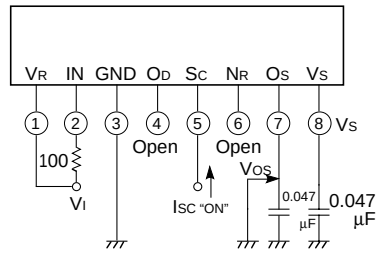


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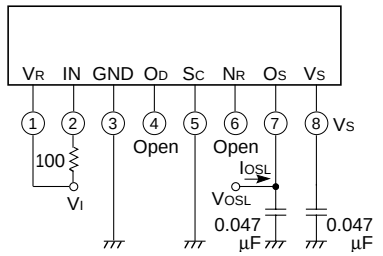


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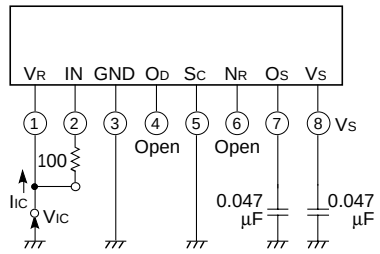


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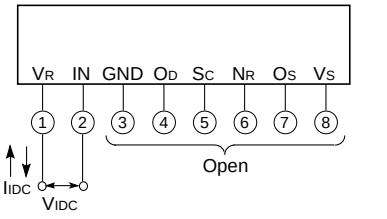


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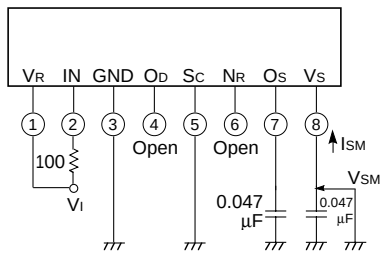


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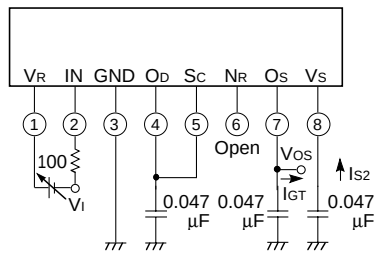


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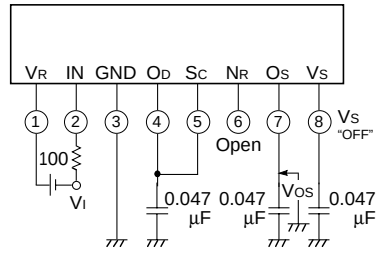


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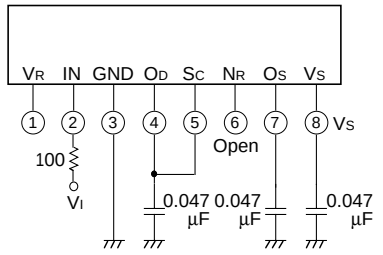
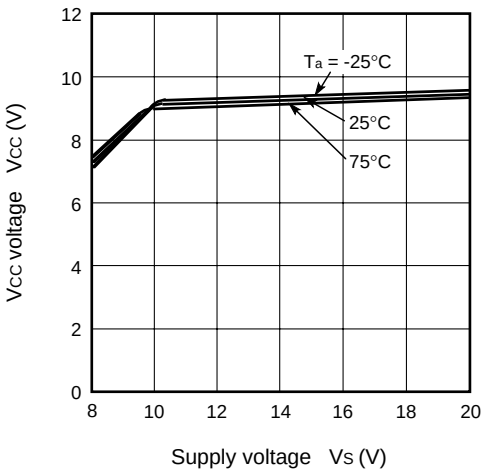


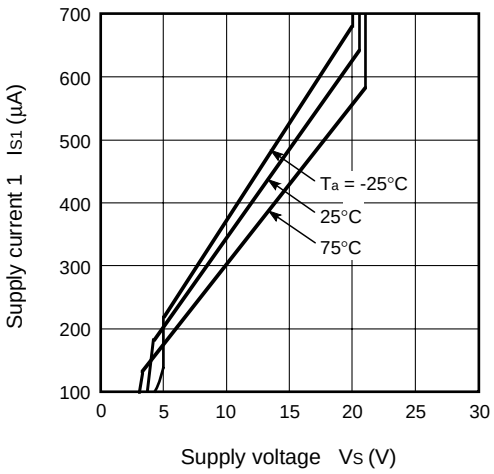

Note: The unit of resistance is ohm.
Please insurt 0.01μF between pin ① and pin ③ in test.

## TYPICAL CHARACTERISTICS

$V_{CC}$ voltage vs. supply voltage

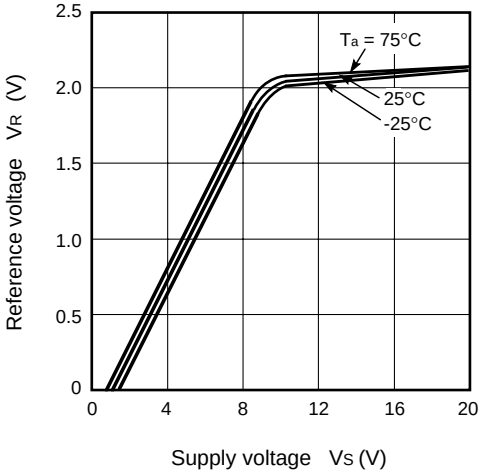



Supply current 1 vs. supply voltage

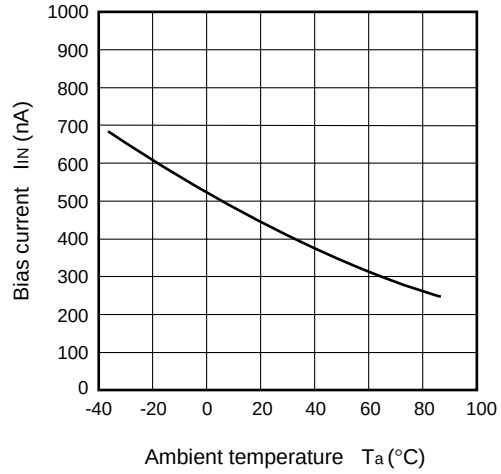



$V_{CC}$ voltage generates by the constant voltage circuit in IC.
This is measured not by M54122L but by a special element.

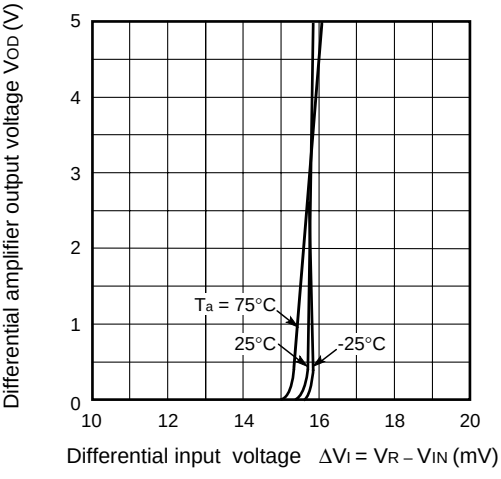
Reference voltage vs. supply voltage



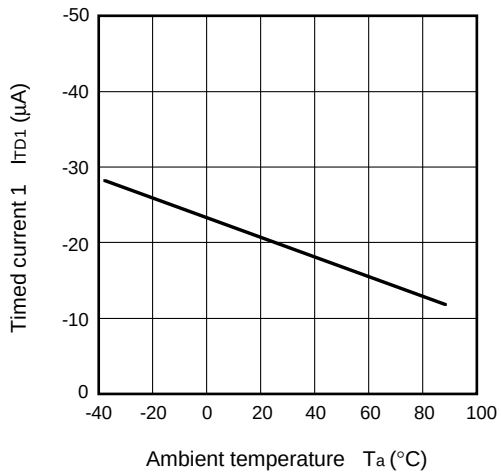

Bias current vs. ambient temperature



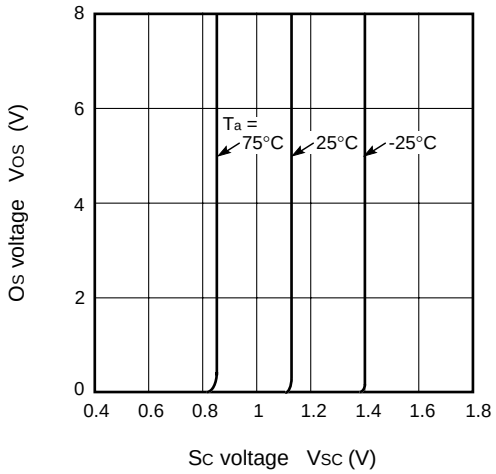

Differential amplifier output voltage
vs. differential input voltage



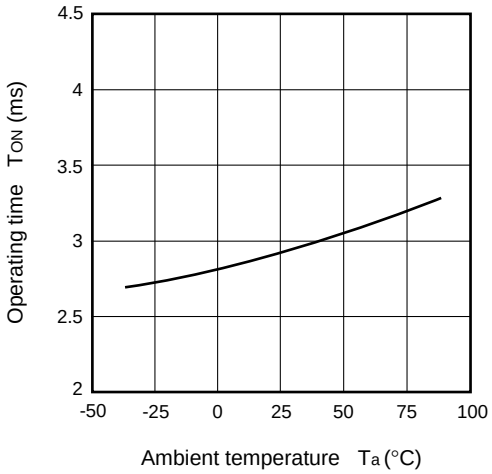

Timed current 1 vs. ambient temperature



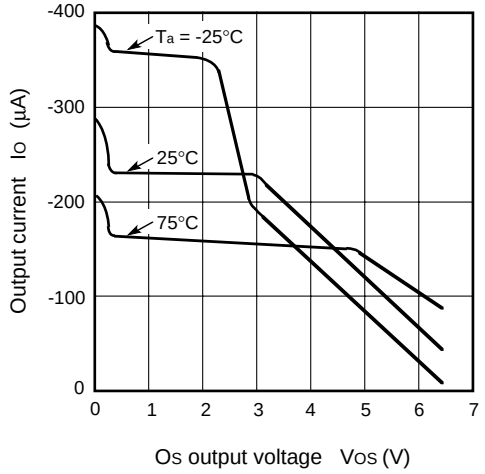
Os voltage vs. Sc voltage



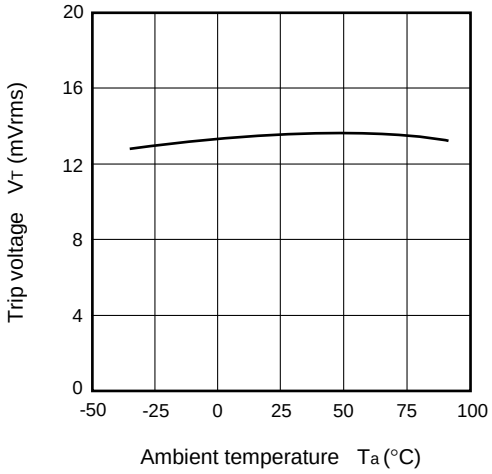

Operating time vs. ambient temperature




Output current vs. Os output voltage

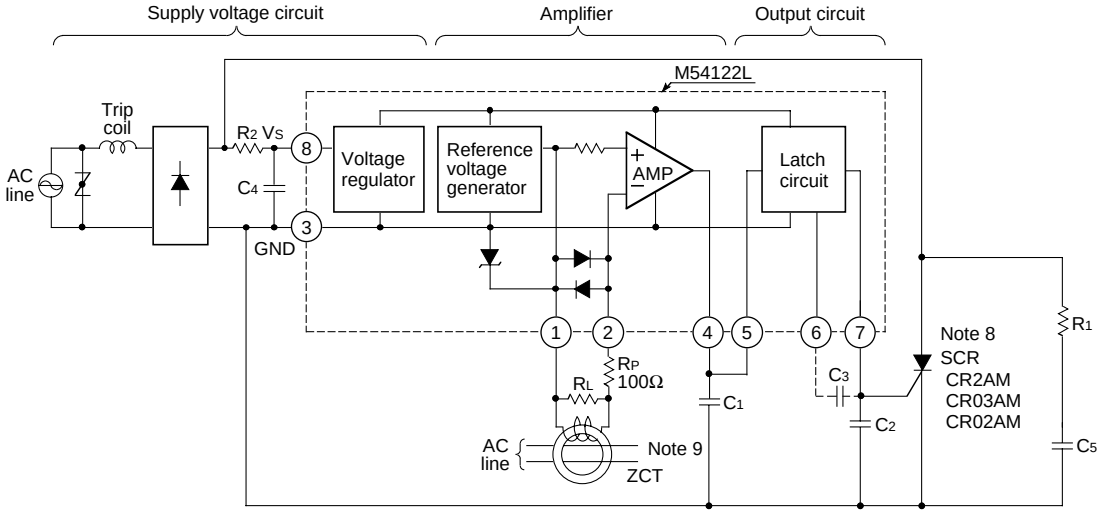



Trip voltage vs. ambient temperature



## APPLICATION EXAMPLE

• HIGH-SPEED LEAKAGE CIRCUIT BREAKER WITH M54122L




Note 8 : Gate current must be selected.
Please select voltage resistance by AC supply voltage.
9 : MZ Core Series by Soryo Denshi Kagaku Co., Ltd (Mitsubishi Subsidiary)
Tel. +81-427-74-7813

Supply voltage circuit is connected as a previous diagram. Please decide constants $R_1$, $R_2$, $C_4$, and $C_5$ of a filter in order to keep at least 12V in $V_S$, when normal supply current flows.
In this case, please connect $C_4$ (more than 1μF) and $C_2$ (less than 1μF). ZCT and load resistance $R_L$ of ZCT are connected between input pin ① and ②. In this case protective resistance ($R_P$ = 100Ω) must be insurted. Sensitivity current is regulated by $R_L$, and output of amplifier shows in pin ④. External capacitor $C_1$ between pin ④ and GND is used for noise removal.
When large current is grounded in the primary side (AC line) of ZCT, the wave form in the secondary side of ZCT is distorted and some signals doesn't appear in the output of amplifier. So please connect a varistor or a diode (2 pcs.) to ZCT in parallel.
Latch circuit is used to inspect the output level of amplifier and to supply gate current on the external SCR. When input pin becomes more than 1.1V (Typ.), latch circuit operates and supply gate current in the gate of SCR connected to the output pin ⑦.
Pin ⑥ can be used in the open state, but please connect capacitor (about 0.047μF) between pin ⑥ and pin ⑦.

Operating time vs. input voltage