CMOS 4-BIT MICROCONTROLLER

TMP47C834N
TMP47C834F

The 47C834 are based on the TLCS-470 CMOS series. The 47C834 have on-screen display circuit to display characters and marks which indicate channel or time on TV screen, A/D converter input, and D/A converter output.

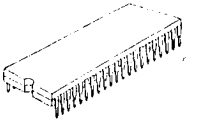
PART No.	ROM	RAM	PACKAGE	OTP version
TMP47C834N	8192 x 8-bit	512 x 4-bit	SDIP42	* TMP47P834N
TMP47C834F			QFP44	* TMP47P834F

*: Under Development

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2 MHz)
- ◆92 basic instructions
- ◆Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (30 pins)
  - Input 2 ports 5 pins
  - I/O 7ports 25 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Watchdog timer
- ◆Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - External/internal clock, leading/trailing edge shift, 4/8-bit
- ◆On-screen display circuit
  - Character patterns : 62 characters
  - Characters displayed : 16 columns x 2 lines
  - Composition : 8 x 8 dots (smoothing function)
  - Size of character : 2 kinds (line by line)
  - Color of character : 7 kinds (character by character)
  - Variable display position : horizontal 64 / vertical 64 steps
  - Double scan mode switching function
- ◆D/A converter (Pulse width modulation) outputs
  - 14-bit resolution 1 channel
  - 6-bit resolution 4 channels
- ◆3-bit A/D converter input
  Auto frequency control signal (S-shaped curve) detection
- ◆Pulse output (clock for PLL IC)
- ◆Horizontal synchronous signal is detected by timer/counter
- ◆Remote control signal preprocessing capability
- ◆High current outputs
  LED direct drive capability (typ. 20mA x 4 bits)
- ◆HOLD function : Battery/Capacitor back-up
- ◆Real Time Emulator : BM47C834B (Under development)

SDIP42



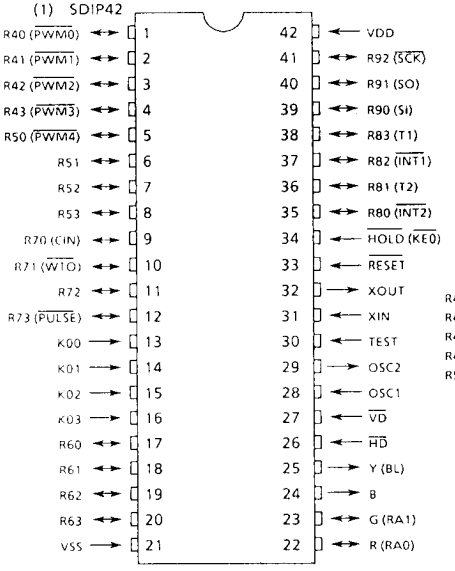
TMP47C834N
TMP47P834N

QFP44

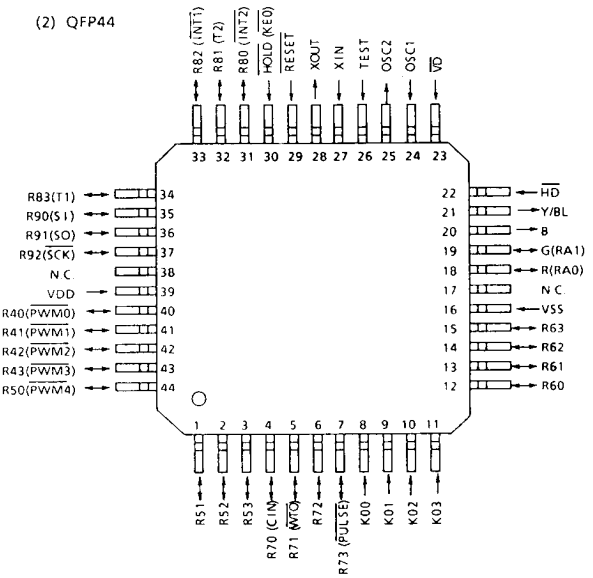
TMP47C834F
TMP47P834F

PIN ASSIGNMENT (TOP VIEW)

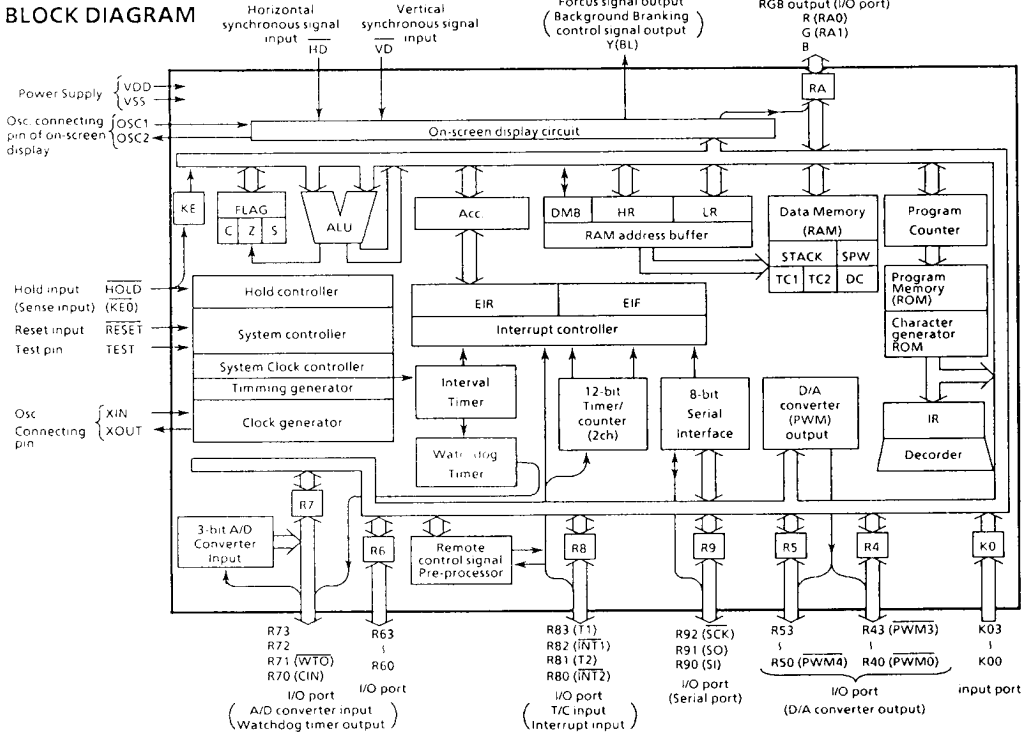
(1) SDIP42



(2) QFP44



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	input	4-bit input port	
R43 ($\overline{PWM3}$)	I/O (output)	4-bit I/O port with latch. When used as input port or D/A converter outputs pins, the latch must be set to "1".	6-bit D/A converter (PWM) output
-R41 ($\overline{PWM1}$)			
R40 ($\overline{PWM0}$)			14-bit D/A converter (PWM) output
R53 - R51	I/O		
R50 ($\overline{PWM4}$)	I/O (output)		6-bit D/A converter (PWM) output
R63 - R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R73 ($\overline{PULSE}$)	I/O (output)	4-bit I/O port with latch. When used as input port, watchdog timer output pin, or A/D converter input pin, the latch must be set to "1".	PULSE output
R72	I/O		
R71 ($\overline{WTO}$)	I/O (output)		Watchdog timer output
R70 (CIN)	I/O (input)		3-bit A/D converter input
R83 (T1)	I/O (input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (output)		Serial data output
R90 (SI)	I/O (input)		Serial data input
G (RA1)	Output (I/O)	RGB output	2-bit I/O port with latch. When used as input port, the latch must be set to "1".
R (RA0)			
B	Output		
Y (BL)	Output (output)	Focus signal output	Background blanking control signal output
$\overline{HD}$, $\overline{VD}$	Input	Horizontal synchronous signal input, Vertical synchronous signal input	
OSC1, OSC2	input, output	Resonator connecting pin of on-screen display circuit	
XIN, XOUT	input, output	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	input (input)	HOLD request/release signal input	Sense input
TEST	input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C834, the configuration and functions of hardwares are described.
As the description is provided with priority on those parts differing from the 47C434/634, the technical data sheets for the 47C434/634 and 47C660/860 shall also be referred to.

1. SYSTEM CONFIGURATION

(1) Program Memory (ROM)
(2) Data Memory (RAM)
(3) I/O Ports
(4) On-screen display (OSD) control circuit

2. INTERNAL CPU FUNCTION

2.1 Program Memory (ROM)

Programs are stored in address 0000 to $1FFF_H$ of 47C834. By the ROM data reference instruction [LDH A,@DC +, LDL A,@DC], the fixed data in address 1000_H to $1FFF_H$ can be loaded to the accumulator, respectively.

2.2 Data memory (RAM)

The 47C834 contains 256 × 4 bits data memory bank 0 (DMB0) and 256 × 4 bits data memory bank 1 (DMB1). The bank is controlled by DMB.

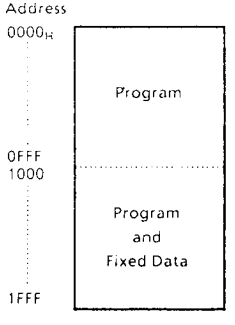


Figure 2-1. Program Memory

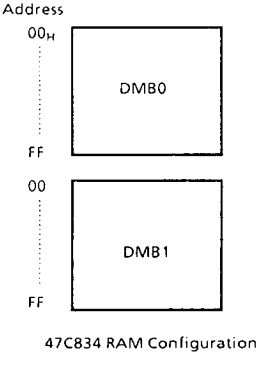


Figure 2-2. Data Memory (RAM)

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Ports

The 47C834 have 9 I/O ports (30 pins) each as follows.

① K0 ; 4-bit input
② R4, R5 ; 4-bit input/output (shared with pulse width modulation output)
③ R6 ; 4-bit input/output
④ R7 ; 4-bit input/output (shared with comparator input and watchdog timer output and pulse output)
⑤ R8 ; 4-bit input/output (shared with external interrupt input and timer/counter input)
⑥ R9 ; 3-bit input/output (shared with serial port)
⑦ RA ; 2-bit input/output (shared with on-screen display output)
⑧ KE ; 1-bit sense input (shared with hold request / release signal input)

This section describes ports of ④, which are changed from the 47C434/634.
Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port R7 (R73-R70)

The 4-bit I/O port with latch. When used as an input port, the latch should be set to "1". The latch is initialized to "1" during reset. R72 pins is I/O port usually.

Pin R70 (CIN) is shared with the digital input usual and the A/D converter (comparator) input for Auto Frequency Control signal detection. CIN input is comparator input and setting of 3-bit DIA convert for reference voltage are performed by the command register. R71 ($\overline{WTO}$), R73 ($\overline{PULSE}$) pins are shared with the watchdog timer output and pulse output. R70, R71, R73 pins latch is initialized to "1" during reset, and they are able to use I/O port usually.

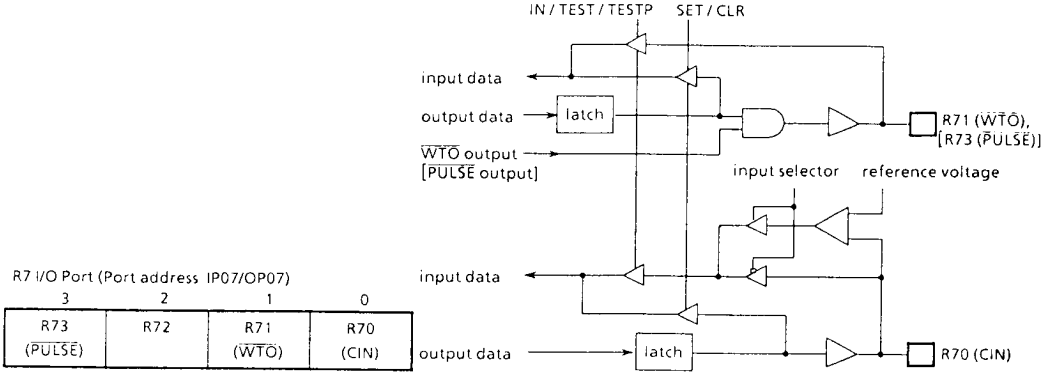


Figure 3-1. Port R7

Port address (**)	Port		I/O instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB@HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	Tri-state (R4 port) control	○	○	○	–	–	○	–
01	——	——	–	–	–	–	–	–	–
02	——	——	–	–	–	–	–	–	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RA input port	RA output port	○	○	○	–	○	○	–
0B	——	PULSE output control	–	○	○	–	–	–	–
0C	——	OSD command selector	–	○	○	–	–	–	–
0D	Remote control count value register	Remote control offset valve register	○	○	○	–	–	–	–
0E	status input (Note 2)	Remote control single preprocess circuit control	○	○	○	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	undefined	Hold operating mode control	–	○	–	–	–	–	–
11	undefined	——	–	–	–	–	–	–	–
12	undefined	A/D converter input control	–	○	–	–	–	–	–
13	undefined	Tri-state (R5 port) control	–	○	–	–	–	–	–
14	undefined	——	–	–	–	–	–	–	–
15	undefined	Watchdog timer control	–	○	–	–	–	–	–
16	undefined	——	–	–	–	–	–	–	–
17	undefined	PWM buffer selector	–	○	–	–	–	–	–
18	undefined	PWM data transfer buffer	–	○	–	–	–	–	–
19	undefined	Interval timer interrupt control	–	○	–	–	–	–	–
1A	undefined	OSD control	–	○	–	–	–	–	–
1B	undefined	——	–	–	–	–	–	–	–
1C	undefined	Timer/counter 1 control	–	○	–	–	–	–	–
1D	undefined	Timer/counter 2 control	–	○	–	–	–	–	–
1E	undefined	SIO control 1	–	○	–	–	–	–	–
1F	undefined	SIO control 2	–	○	–	–	–	–	–

Note 1: "——" means the reserved state. Unavailable for the user programs.

Note 2: The status input of serial interface, clock generator, and $\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$) pin.

Table 3-1. Port Address Assignments and Available I/O Instructions

3.2 On-screen display (OSD) circuit

An on-screen display (OSD) circuit used to display characters and symbols in built into the TV screen.
A maximum of 32 characters, as 16 columns x 2 lines, out of 62 character patterns can be displayed at a time.

3.2.1 OSD Circuit Function

①	Number of characters	62 kinds
②	Number of characters displayed	32 characters (16 columns x 2 lines)
③	Composition of a character	8 x 8 dots (with smoothing function)
④	Size of character	2 kinds (selectable line by line)
⑤	Color of character	7 kinds (selectable character by character)
⑥	Display position variable	horizontal 64 steps, vertical 64 steps
⑦	Double Scan mode switching function	

Only the OSD functions ① and ⑦, which are different from those of the 47C434/634, are explained here. Refer to the 47C434/634 technical data concerning all other OSD circuit functions, which are the same.

3.2.2 OSD Circuit Configuration

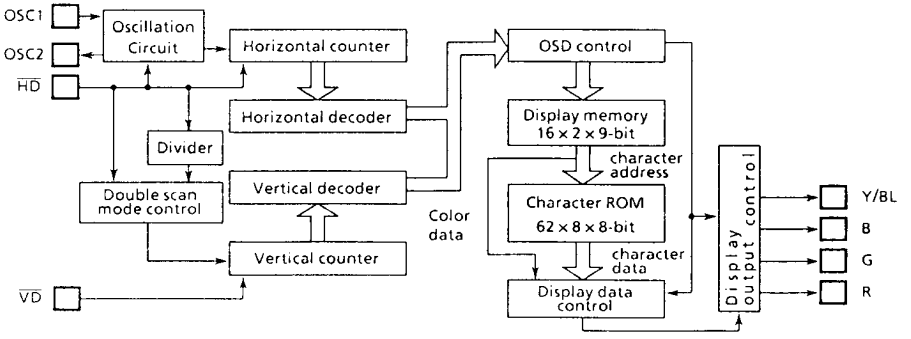


Figure 3-2. OSD Circuit

3.2.3 Character ROM

The 47C834 can display 62 different 8 x 8 dot characters (character ROM addresses 00_H - $3D_H$). Address $2F_H$ in the character ROM displays a blank, as with the 47C434/634, so set all ROM data to "0".
The first 48 characters of the 47C834 character ROM are the same as those of the 47C434/634; therefore, 47C434/634 programs can be used without change.

Figure 3-3. Character ROM Configuration

Note: Character ROM addresses $3E_H$ and $3F_H$ are used in shipping tests and cannot be specified.

3.2.4 Double Scan Mode Switching Function

The 47C834 has an Double scan mode switching function for selecting the interlace mode or the double scan (non-interlace) mode.

When the double scan mode is used, the number of scan lines on the screen is double that of the interlace mode; therefore, the $\overline{HD}$ signal is single-stage divided so that the vertical display start position and character size will be the same as with the interlace mode.

In the double scan mode, the horizontal scan line cycle is one-half that of the interlace mode; therefore, it is necessary to increase the OSD oscillation frequency.

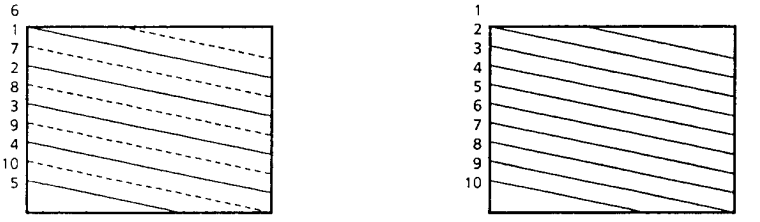


Figure 3-4. Double Scan Mode

3.2.5 Double Scan Mode Control

Double scan mode switching is controlled by WHD of the command register OP0B. Setting WHD to "0" selects the double scan mode and setting WHD to "1" selects the interlace mode. The initial setting selects the interlace mode.

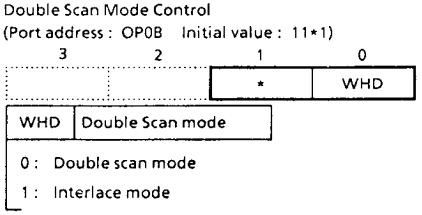


Figure 3-5. Double Scan Mode Command Register

3.3 Pulse Output Circuit

Pulse output circuit generates the pulse clock by dividing the clock frequency to R73 port. The pulse output is used for the basic clock for the PLL IC or peripheral ICs. The pulse output frequency can be set by accessing command register (OP0B). Command register is initialized to '11**' during reset. When R73 port is used as the pulse output, set R73 output latch to "1".

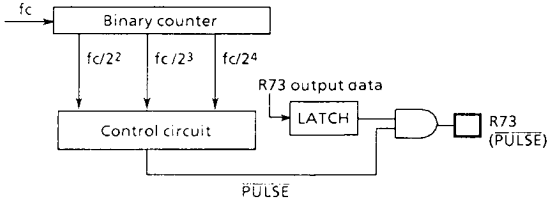


Figure 3-6. Pulse Output Circuit

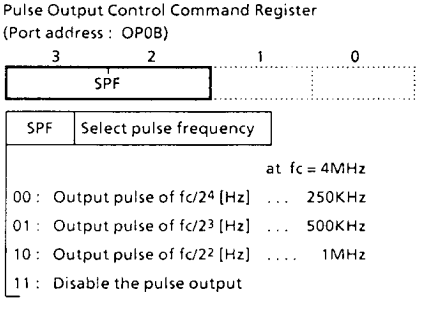


Figure 3-7. Pulse Output Command Register

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7 port	− 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	R6 port	30	mA
	I_{OUT2}	R7, R8, R9 port	3.2	
Output Current (Total)	ΣI_{OUT1}	R6 port	60	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	4.2	MHz
	f_{OSD}			−	6.0	

Note. Input Voltage V_{IH3}, V_{IL3}: in the HOLD mode.

D.C. CHARACTERISTICS

(V_{SS} = 0V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	K0 port, TEST, RESET, HOLD	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	–	–	± 2	μA
	I_{IN2}	R port (open drain)					
Input Low Current	I_{IL}	R port (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	–	–	– 2	mA
Input Resistance	R_{IN1}	K0 port with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	RESET		100	220	450	
Output leakage Current	I_{LO}	Tri-state R6, R8, R9 port (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	–	–	± 2	μA
Output High Voltage	V_{OH1}	R port (push-pull)	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	–	–	V
	V_{OH2}	R port (tri-state), OSD output	V_{DD} = 4.5V, I_{OH} = – 0.7mA	4.1	–	–	
Output Low Voltage	V_{OL1}	R7, R8, R9 port	V_{DD} = 4.5V, I_{OL} = 1.6mA	–	–	0.4	V
	V_{OL2}	R port (tri-state), OSD output	V_{DD} = 4.5V, I_{OL} = 0.7mA				
Output Low Current	I_{OL}	R6 port	V_{DD} = 4.5V, V_{OL} = 1.0V	–	20	–	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	–	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	–	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up /pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the pull-up / pull-down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

A / D CONVERTER CHARACTERISTICS

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V_{AIN}	CIN		V_{SS}	–	V_{DD}	V
A / D Conversion Error	–			–	–	$\pm\frac{1}{4}$	LSB

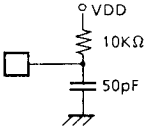
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

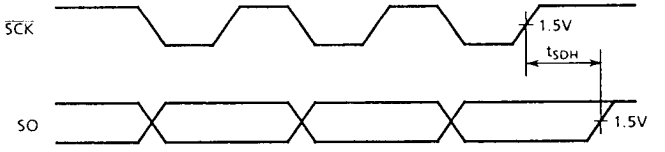
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	–	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns

Note. Shift data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin.



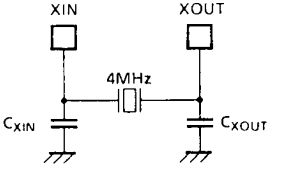
Serial port (Completion of transmission)



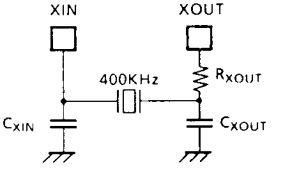
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, Topr = – 30 to 70°C)

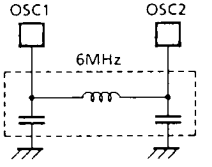
(1) 4MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF



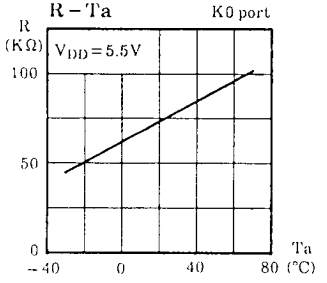
(2) 400KHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

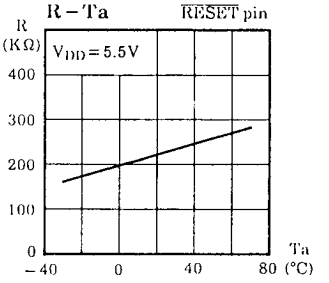


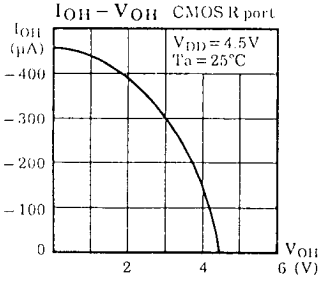
(3) 6MHz (for OSD)
LC Resonator
TBEKSES-30361FBY (TOUKOU)

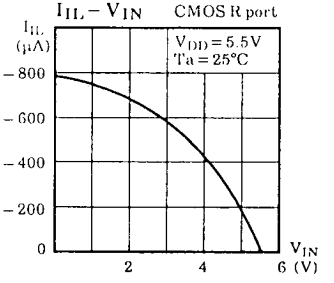


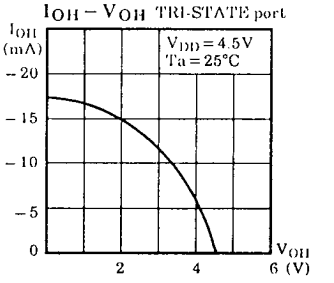
TYPICAL CHARACTERISTICS

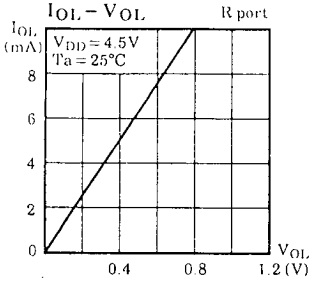


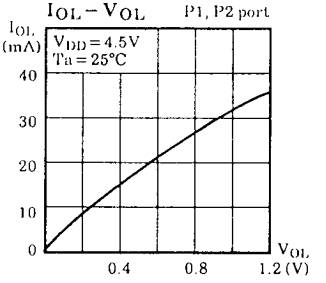


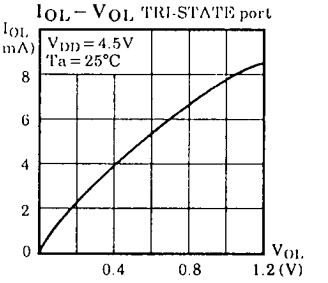


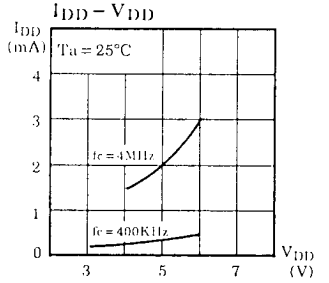


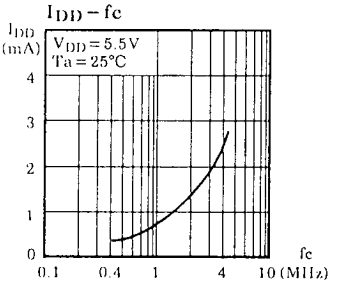








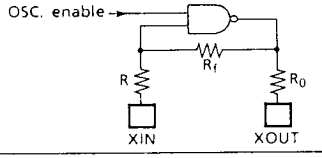
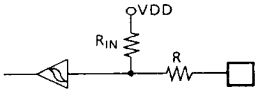
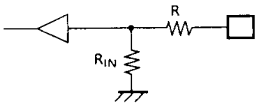
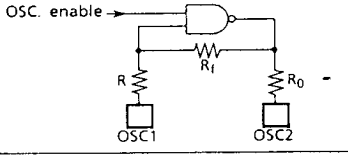
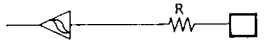




INPUT/OUTPUT CIRCUITRY

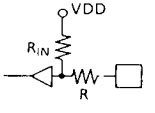
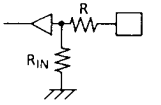
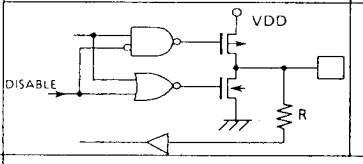
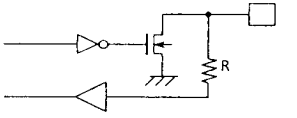
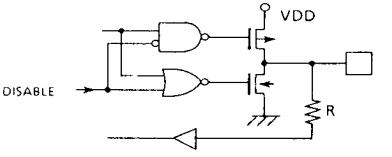
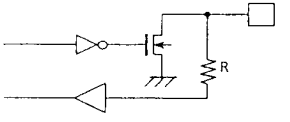
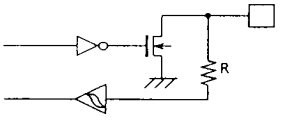
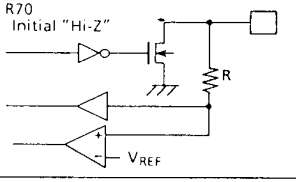
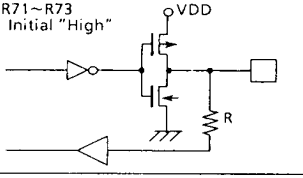
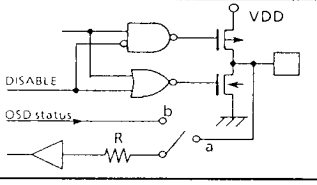
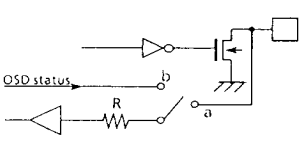
(1) Control Pins

Input/output circuitries of the 47C834 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1KΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2KΩ (typ.)
$\overline{RESET}$	Input		Hysteresis input Contained pull-up resistor R_{IN} = 220KΩ (typ.) R = 1KΩ (typ.)
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)		Hysteresis input (Sense input) R = 1KΩ (typ.)
TEST	Input		Contained pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
OSC1 OSC2	Input Output		Oscillation terminals for OSD R = 1KΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2KΩ (typ.)
$\overline{HD}$ $\overline{VD}$	Input		Synchronous signal input Hysteresis input R = 1KΩ (typ.)

(2) I/O Ports

The input/output circuitries of the 47C834 I/O ports are shown below, any one of the circuitries (PB, PC, PF, PU) can be chosen by a code as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	PB:  PC, PF, PU: 	Pull-up or pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
R4 R50	I/O	PB, PC:  PF, PU: 	Tri-state or Sink open drain Initial "Hi-Z" R = 1KΩ (typ.)
R51 R52 R53	I/O		Tri-state Initial "Hi-Z" R = 1KΩ (typ.)
R6 R8 R9	I/O	R6:  R8, R9: 	Sink open drain Initial "Hi-Z" Hysteresis input (R8, R9) R = 1KΩ (typ.)
R7	I/O	 	Sink open drain and push-pull Comparator input (R70 pin) R = 1KΩ (typ.)
R (RA0) G (RA1)	I/O	PB, PC, PF:  PU: 	Tri-state Initial "Hi-Z" R = 1KΩ (typ.) R, G : Side a B, Y : Side b
B Y (BL)	Output		