AN6592, AN6592S

Dual Low Power Operational Amplifiers

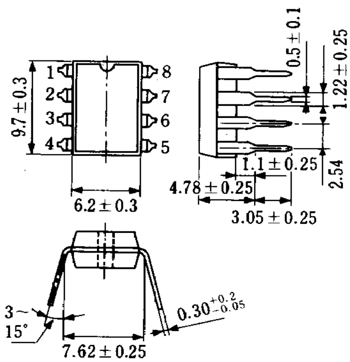
■ Outline

The AN6592 and the AN6592S are dual operational amplifiers allowing very low power consumption operation, with phase compensation circuits built-in and wide supply voltage range, so that they are very easy to use. They are suited for application to various electronic circuits such as portable equipment operated by the battery.

■ Features

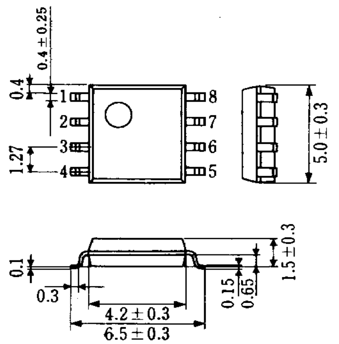
- Phase compensation circuit built-in
- Wide supply voltage range : $\pm 1 \sim 18$V
- Output short-circuit protection
- Low power consumption : $I_{CC} = 250\mu A$ max.
- High gain : $G_V = 100$dB typ.

AN6592 Unit : mm



8-Lead DIL Plastic Package

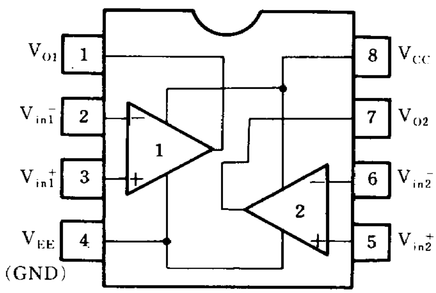
AN6592S Unit : mm



8-Lead PANAFLAT Package(SO-8D)

■ Block Diagram

AN6592
AN6592S



■ Pin

Pin No.	Pin Name
1	Ch. 1 Output
2	Ch. 1 Invert Input
3	Ch. 1 Non Invert Input
4	V_{EE} (GND)
5	Ch. 2 Non Invert Input
6	Ch. 2 Invert Input
7	Ch. 2 Output
8	Vcc

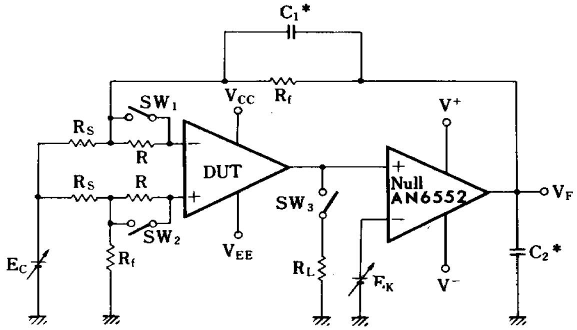
■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V_{CC}	±18	V
	Differential Input Voltage	V_{ID}	±30	V
	Common-Mode Input Voltage	V_{ICM}	±15	V
Power Dissipation	AN6592	P_D	500	mW
	AN6592S		360	
Operating Ambient Temperature		T_{opr}	−20～+75	℃
Storage Temperature	AN6592	T_{stg}	−55～+150	℃
	AN6592S		−55～+125	

■ Electrical Characteristics (V_{CC}=15V, V_{EE}=−15V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(offset)}$	1	$R_S \leqq 10k\Omega$		1	5	mV
Input Offset Current	I_{IO}	1			5	80	nA
Input Bias Current	I_{Bias}	1			50	250	nA
Voltage Gain	G_V	1	$R_L \geqq 10k\Omega$ $V_O = \pm 10V$	70	100		dB
Maximum Output Voltage	$V_{O(max.)}$	2	$R_L \geqq 10k\Omega$	±12	±13		V
Common-Mode Input Voltage Width	V_{CM}	3		±12	±13		V
Common-Mode Rejection Ratio	CMR	1		60	80		dB
Supply Voltage Rejection Ratio	SVR	1			30	200	μV/V
Supply Current	I_{CC}	4	$R_L = \infty$		130	250	μA
Slew Rate	SR	5	$R_L \geqq 10k\Omega$		0.5		V/μs
Noise Voltage Referred to Input	V_{ni}	6	$R_S = 1k\Omega$, DIN/AUDIO		4		μV_{rms}

Test Circuit 1 ($V_{I(offset)}$, I_{IO}, I_{Bias}, G_V, CMR, SVR)

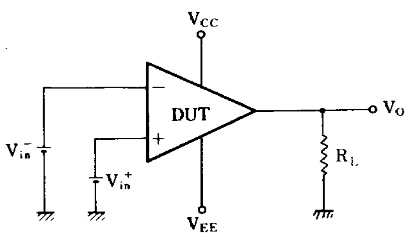


$R_S = 50\Omega$
$R = 10k\Omega$
$R_f = 20k\Omega$
$R_L = 10k\Omega$
$V_{CC} = 15V$
$V_{EE} = -15V$
$V^+ = 15V$
$V^- = -15V$

* C_1 and C_2 are capacitors for the prevention of oscillation.

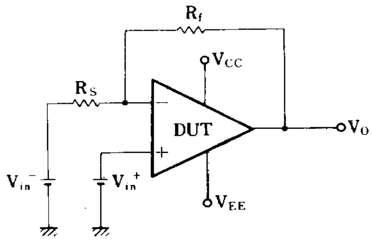
Item	Measurement Conditions
Input Offset Voltage	V_{F1} is measured with the SW_1, SW_2 and SW_3 set to OFF and $E_C = E_K = 0V$. Can be given by $V_{I(offset)} = \frac{V_{F1}}{400}$ (V)
Input Offset Current	V_{F2} is measured with the SW_1 and SW_2 set to ON, the SW_3 set to OFF and $E_C = E_K = 0V$. Can be given by $I_{IO} = \frac{\lvert V_{F2} - V_{F1} \rvert}{4 \times 10^6}$ (A)
Input Bias Current	V_{F3} is measured with the SW_1 set to ON, the SW_2 set to OFF, the SW_3 set to OFF and $E_C = E_K = 0V$. V_{F4} is measured with the SW_1 and SW_2 reversed. Can be given by $I_{Bias} = \frac{\lvert V_{F3} - V_{F4} \rvert}{8 \times 10^6}$ (A)
Voltage Gain	V_{F5} is measured with the SW_1 SW_2 and SW_3 set to ON, $E_C = 0V$ and $E_K = 10V$. V_{F5}' is measured with $E_K = -10V$. Can be given by $G_V = 20\log\left(\frac{8000}{\lvert V_{F5} - V_{F5}' \rvert}\right)$
Common-Mode Rejection Ratio	V_{F6} is measured with the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K = 0V$ and $E_C = 5V$. V_{F6}' is measured with $E_C = -5V$. Can be given by $CMR = 20\log\left(\left\lvert\frac{4000}{\lvert V_{F6} - V_{F6}' \rvert}\right\rvert\right)$
Supply Voltage Rejection Ratio I	V_{F7} is measured with the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K = E_C = 0V$ and $V_{CC} = 10V$. Can be given by $SVR(+) = \frac{\lvert V_{F7} - V_{F2} \rvert}{2 \times 10^3}$
Supply Voltage Rejection Ratio II	V_{F8} is measured with the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K = E_C = 0V$ and $V_{EE} = -10V$. Can be given by $SVR(-) = \frac{\lvert V_{F8} - V_{F2} \rvert}{2 \times 10^3}$

Test Circuit 2 ($V_{O(max.)}$)



$V_{CC} = 15V$
$V_{EE} = -15V$
$R_L = 10k\Omega$
$V_{in}^- = 0V$ or $1V$
$V_{in}^+ = 1V$ or $0V$

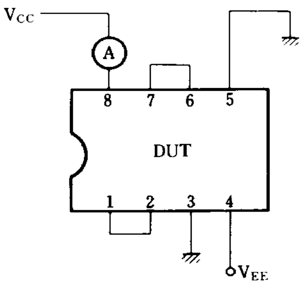
Test Circuit 3 (V_{CM})



$V_{CC} = 15V$
$V_{EE} = -15V$
$R_S = 1k\Omega$
$R_f = 10k\Omega$

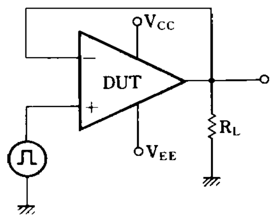
Note: Apply a voltage of $|V_{in}^+| > 12V$ and check $V_0 = V_{in}^+ + \frac{R_f}{R_s}(V_{in}^+ - V_{in}^-)$.

Test Circuit 4 (P_C)



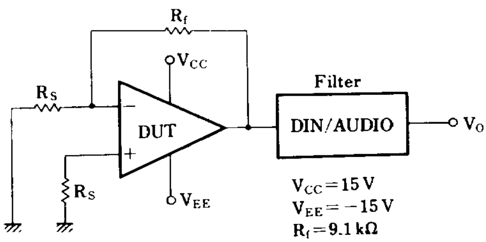
$V_{CC} = 15V$
$V_{EE} = -15V$

Test Circuit 5 (SR)



$V_{CC} = 15V$
$V_{EE} = -15V$
$R_L = 2k\Omega$

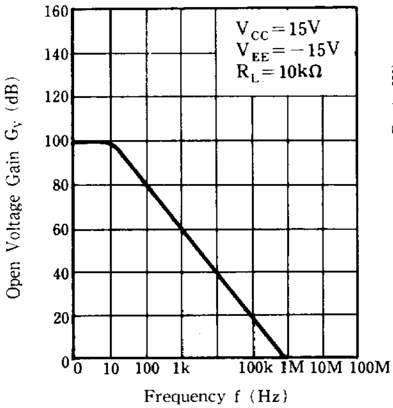
Test Circuit 6 (V_{ni})



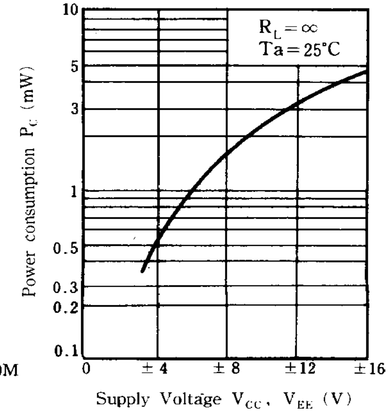
$V_{CC} = 15V$
$V_{EE} = -15V$
$R_f = 9.1k\Omega$
$R_S = 1k\Omega$

Note: A noise voltage referred to input, $V_{ni} = \frac{V_O}{(1 + R_f/R_s)}$ is given.

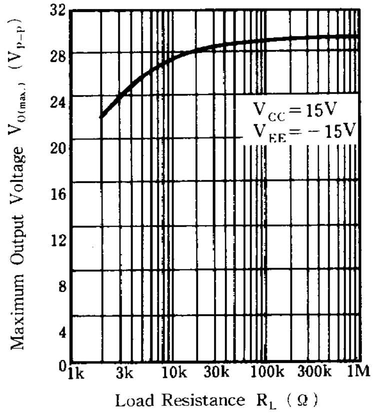
G_V—f



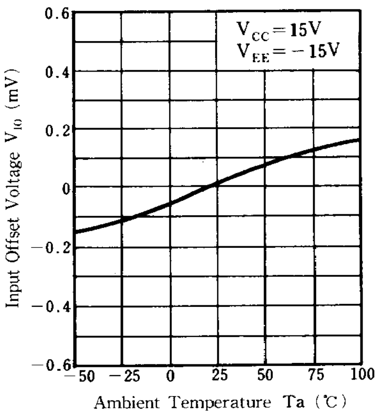
P_C—V_{CC}, V_{EE}



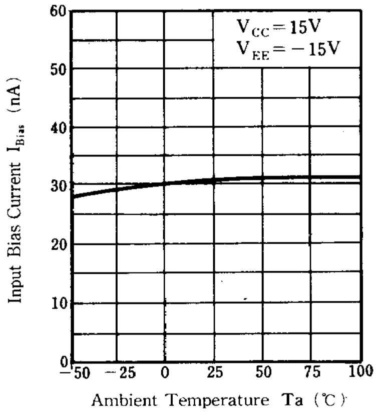
$V_{O(max.)}$—R_L



V_{IO}—Ta



I_{Bias}—Ta



I_{IO}—Ta