

DUAL J-K FLIP-FLOP

MTTL III MC3100/3000 series

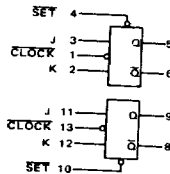
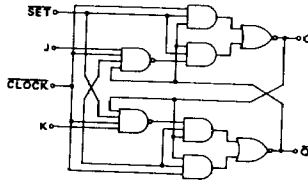
MC3162F • MC3062F
MC3162L • MC3062L,P

This dual J-K flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

the Set up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the SET input.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN



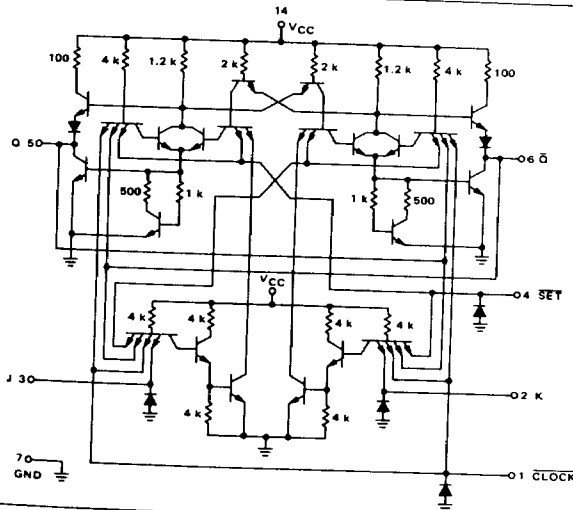
J-K TRUTH TABLE

J	K	Q ⁿ⁺¹	Q ⁿ
0	0	Q ⁿ	0
0	1	0	1
1	0	1	0
1	1	Q ⁿ	1

Typical Characteristics
(V_{CC} = 5.0 V, T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
 Toggle Frequency = 50 MHz typ
 Logical '1' Setup Time = 8.0 ns
 Logical '0' Setup Time = 8.0 ns
 Logical '1' and '0' Hold Times = 0 ns
 t_{pd1} = 12 ns
 t_{pd0} = 12 ns

Input Loading Factors:
 CLOCK, SET = 1.75
 J, K = 0.75
 Output Loading Factor = 10



1/2 OF DEVICE SHOWN

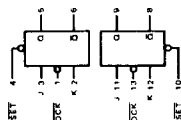
See General Information section for packaging.

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MC3162F, MC3062F/MC3162L, MC3062L,P (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



Characteristic		Symbol	Pin Under Test	MC3162 Test Limits						MC3062 Test Limits						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW												P ₊	Gnd				
				-55°C			+25°C			+75°C			0°C			+25°C			+75°C			@ Test Temperature					mA						
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max
Input Forward Current	I _F	2	-	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5			
	I _{FS}	4	-	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7			
Leakage Current	I _{FC}	1	-	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6	-4.6			
	I _R	2	-	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50	-50			
	I _{FS}	4	-	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150			
	I _{RC}	1	-	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150	-150			
Breakdown Voltage	BV _{in}	2	-	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5	-5.5			
	V _D	3	-	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5			
	V _D	4	-	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5			
	V _D	1	-	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5			
Clamp Voltage	V _D	2	-	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5			
	V _D	4	-	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5			
Output Output Voltage	V _{OL}	5	-	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4			
	V _{OH}	6	-	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4			
Short-Circuit Current	I _{SC}	5	-	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65		
	I _{SC}	6	-	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65		
Power Requirements (Total Device)	I _{max}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			
	I _{PD}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.

mA		V _F		V _R		V _{CC}		V _{CH}		
I _{OL}	I _{OH}	V _F	V _R	V _{CC}	V _{CH}	V _{CC}	V _{CH}	V _{CC}	V _{CH}	
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.4	4.0	-	-	5.0	4.5	5.5
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-	-0.4	2.5	4.0	-	-	5.0	4.75	5.25
20	-2.0	-								

* Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

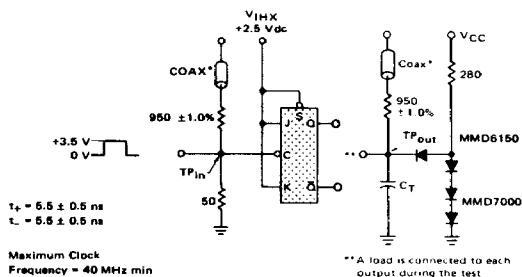
The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the $Q = 1$ state by applying a low level to the SET input. The direct SET inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering - The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

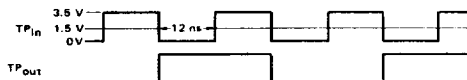
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

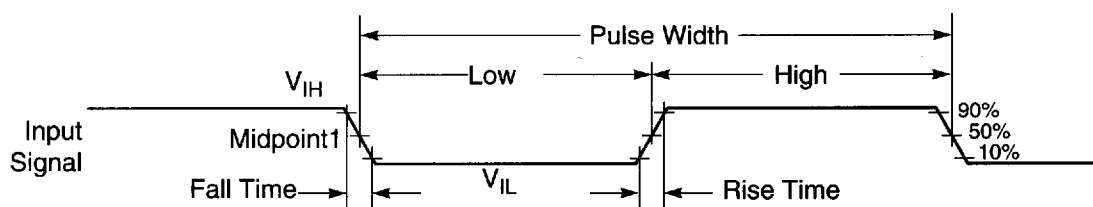
$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference