19-2641; Rev 0; 10/02

EVALUATION KIT AVAILABLE

PWM Buck Converters with Bypass FET for N-CDMA/W-CDMA Handsets

General Description

The MAX8500–MAX8504 PWM DC-to-DC buck converters are optimized with integrated bypass FET (0.25Ω typ) to provide power to the PA in N-CDMA and W-CDMA cell phones. The devices have a low on-resistance FET to bypass the external inductor for low dropout of only 150mV at 600mA load, regardless of inductor series resistance. The supply voltage range is from 2.6V to 5.5V and the guaranteed converter output current is 600mA. The 1MHz PWM switching frequency allows for small external components.

The MAX8500–MAX8503 are dynamically controlled to provide varying output voltages from 0.4V to V_{BATT}. The LDO regulation point is slightly lower than the PWM converter such that the transition into and out of dropout is smooth, regardless of the inductor resistance. The MAX8504 is programmed for fixed 1.25V to 2.5V output with external resistors. It features a high-power bypass mode that connects the output directly to the battery. All devices are designed to achieve an output settling time of less than 30µs for a full-scale change in output voltage and load current.

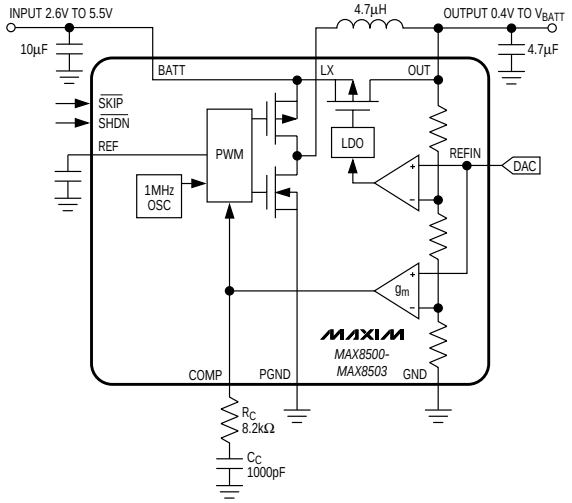
The MAX8500–MAX8504 are available in a 12-lead 4mm x 4mm thin QFN package (0.8mm max height).

Applications

N-CDMA/W-CDMA Cellular Phones

Wireless PDAs and Modems

Typical Operating Circuit



Features

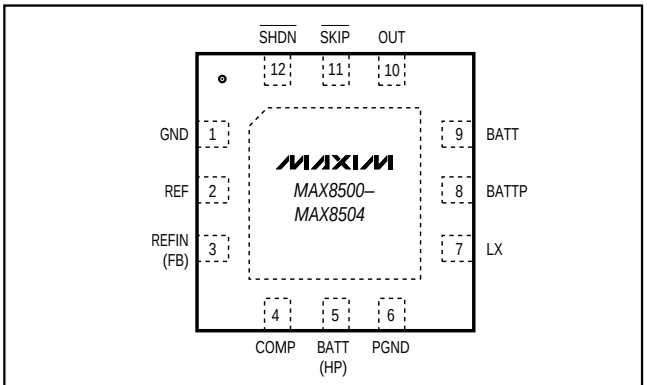
- **Integrated Bypass PFET**
- **150mV Dropout at 600mA Load (Regardless of External Inductor)**
- **Dynamically Adjustable Output from 0.4V to V_{BATT}**
- **Externally Fixed Output from 1.25V to 2.5V with Digitally Controlled High-Power Bypass Mode (MAX8504)**
- **1MHz Fixed-Frequency PWM Switching**
- **600mA Guaranteed Output Current**
- **10% to 100% Duty-Cycle Operation**
- **Low Quiescent Current**
  - **280µA (typ) in Normal Mode**
  - **3.3mA (typ) in PWM Mode**
  - **0.1µA (typ) in Shutdown Mode**
- **12-Pin Thin QFN (4mm x 4mm, 0.8mm max Height)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX8500ETC	-40°C to +85°C	12 Thin QFN	AABQ
MAX8501ETC*	-40°C to +85°C	12 Thin QFN	—
MAX8502ETC*	-40°C to +85°C	12 Thin QFN	—
MAX8503ETC	-40°C to +85°C	12 Thin QFN	AABU
MAX8504ETC	-40°C to +85°C	12 Thin QFN	AABS

**Future product—contact factory for availability.*

Pin Configuration



Thin QFN 4mm x 4mm

( ) MAX8504 ONLY

ABSOLUTE MAXIMUM RATINGS

BATTP, BATT, OUT, $\overline{SHDN}$, $\overline{SKIP}$, HP, REFIN, FB to GND ..... -0.3V to +6V
PGND to GND ..... -0.3V to +0.3V
REF, COMP to GND ..... -0.3V to (V_{BATT} + 0.3V)
LX Current (Note 1) 2.25A
Output Short-Circuit Duration ..... Indefinite

Continuous Power Dissipation (T_A = +70°C)
12-Lead Thin QFN (derate 16.9mW/°C above +70°C) .1349mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: LX has internal clamp diodes to PGND and BATTP. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = V_{BATTP} = 3.6V, $\overline{SHDN}$ = $\overline{SKIP}$ = BATT, V_{REFIN} = 1.932V (MAX8500, MAX8502), V_{REFIN} = 1.70V (MAX8501, MAX8503), C_{REF} = 0.22µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input BATT Voltage	V_{BATT}		2.6		5.5	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{BATT} rising, 1% hysteresis	2.15	2.35	2.50	V
Quiescent Current	I_Q	$\overline{SKIP}$ = GND		280	450	µA
		$\overline{SKIP}$ = BATT, no switching		450	2200	
		$\overline{SKIP}$ = BATT, switching		3300		
Quiescent Current in Dropout		V_{REFIN} = 2.2V (MAX8500, MAX8503), HP = BATT (MAX8504)		400	700	µA
Shutdown Supply Current	I_{SHDN}	$\overline{SHDN}$ = GND, V_{BATT} = V_{BATTP} = 5.5V		0.1	5	µA
OUT Voltage Accuracy (MAX8500, MAX8502)	V_{OUT}	V_{REFIN} = 1.932V, load = 0 to 600mA	3.33	3.40	3.47	V
		V_{REFIN} = 0.227V	0.35	0.40	0.45	
OUT Voltage Accuracy (MAX8501, MAX8503)	V_{OUT}	V_{REFIN} = 1.700V, load = 0 to 600mA	3.33	3.40	3.47	V
		V_{REFIN} = 0.200V	0.35	0.40	0.45	
OUT Voltage-Load Regulation				-0.05		%/A
OUT Voltage-Line Regulation				0.007		%/V
OUT Input Resistance		MAX8500, MAX8503	100	245		kΩ
REFIN Input Current	I_{REF}		-1	0.1	+1	µA
REFIN to OUT Gain (MAX8500, MAX8502)	A_V	PWM buck		1.76		V/V
		LDO linear regulator		1.68		
REFIN to OUT Gain (MAX8501, MAX8503)	A_V	PWM buck		2		V/V
		LDO linear regulator		1.909		
Reference Voltage	V_{REF}		1.225	1.25	1.275	V
Reference Load Regulation		10µA < I_{REF} < 100 µA			6.25	mV
Reference UVLO			0.86	0.96	1.10	V
FB Voltage Accuracy (MAX8504)	V_{FB}		1.225	1.250	1.275	V
FB Input Current (MAX8504)	I_{FB}	V_{FB} = 1.3V		10	150	nA
P-Channel On-Resistance	P_{RDS}	I_{LX} = 180mA, V_{BATT} = 3.6V		0.35	0.70	Ω
		I_{LX} = 180mA, V_{BATT} = 2.6V		0.45		

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = V_{BATTP} = 3.6V, $\overline{SHDN}$ = $\overline{SKIP}$ = BATT, V_{REFIN} = 1.932V (MAX8500, MAX8502), V_{REFIN} = 1.70V (MAX8501, MAX8503), C_{REF} = 0.22µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

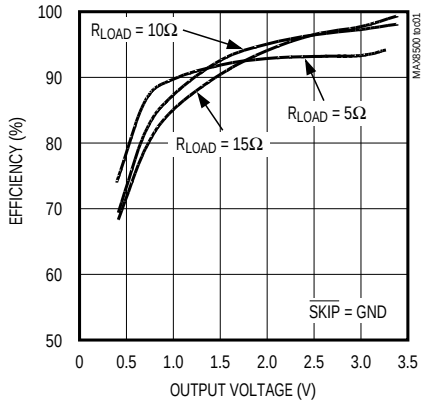
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
N-Channel On-Resistance	N_{RDS}	I_{LX} = 180mA, V_{BATT} = 3.6V		0.26	0.60	Ω
		I_{LX} = 180mA, V_{BATT} = 2.6V		0.33		
LDO/Bypass P-Channel On-Resistance		I_{OUT} = 180mA, V_{BATT} = 3.6V		0.25	0.60	Ω
		I_{OUT} = 180mA, V_{BATT} = 2.6V		0.3		
P-Channel Current-Limit Threshold	I_{LIMP}		1.30	1.45	1.60	A
N-Channel Current-Limit Threshold	I_{LIMN}	$\overline{SKIP}$ = BATT	-0.80	-0.60	-0.40	A
		$\overline{SKIP}$ = GND	30	47	65	mA
P-Channel Pulse-Skipping Current Threshold	I_{SKIP}	$\overline{SKIP}$ = GND	118	148	178	mA
LDO/Bypass P-Channel Current-Limit Threshold			0.70	1.00	1.55	A
LX RMS Current		(Note 3)			1.5	A
LX Leakage Current		V_{BATT} = V_{BATTP} = 5.5V, V_{LX} = 0 to 5.5V	-20	+0.1	+20	µA
Maximum Duty Cycle			100			%
Minimum Duty Cycle		$\overline{SKIP}$ = GND			0	%
		$\overline{SKIP}$ = BATT		10	13	
COMP Clamp Low Voltage			0.7	1.0	1.1	V
COMP Clamp High Voltage			2.0	2.3	2.4	V
Transconductance	g_m	MAX8500, MAX8501	85	142	200	µS
		MAX8502, MAX8503	75	125	175	
		MAX8504	150	250	350	
Current-Sense Transresistance	R_{CS}			0.38		V/A
Internal Oscillator Frequency	f_{OSC}		0.8	1.0	1.2	MHz
LOGIC INPUTS ($\overline{SHDN}$, HP, $\overline{SKIP}$)						
Logic Input High	V_{IH}		1.6			V
Logic Input Low	V_{IL}				0.4	V
Logic Input Current				0.1	1.0	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Temperature				160		°C
Thermal-Shutdown Hysteresis				15		°C

Note 2: Specifications to -40°C are guaranteed by design and not subject to production test.
Note 3: Guaranteed by design, not production tested.

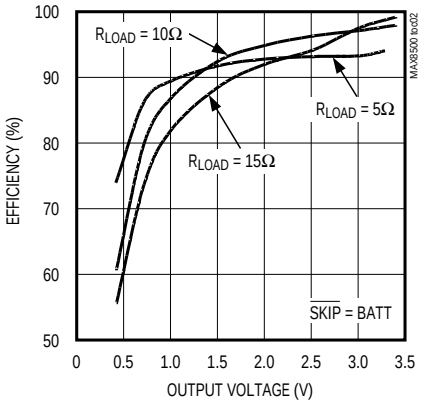
Typical Operating Characteristics

(V_{BATT} = 3.6V, T_A = +25°C, unless otherwise noted.)

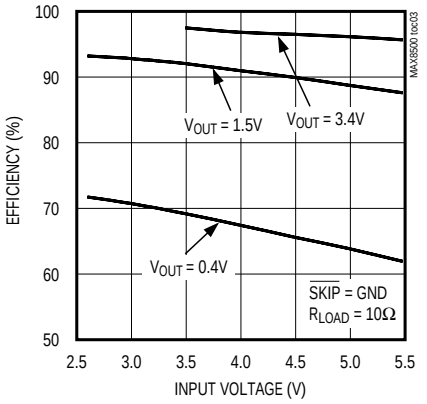
EFFICIENCY vs. OUTPUT VOLTAGE IN NORMAL MODE



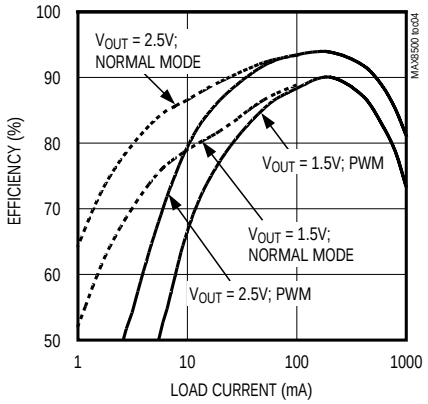
EFFICIENCY vs. OUTPUT VOLTAGE IN PWM MODE



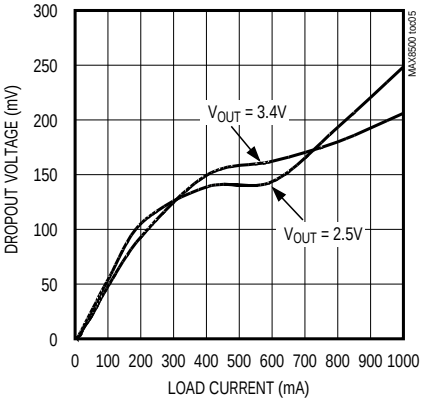
EFFICIENCY vs. INPUT VOLTAGE



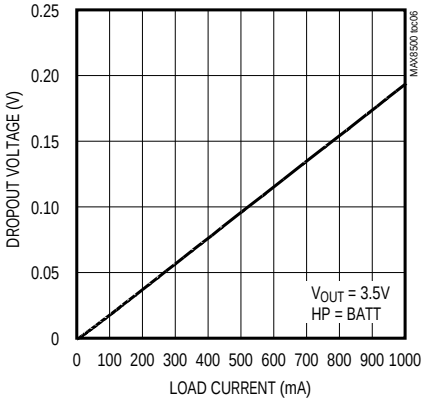
EFFICIENCY vs. LOAD CURRENT



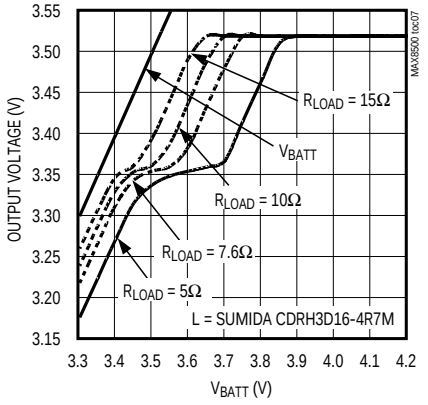
MAX8500/MAX8503 DROPOUT VOLTAGE vs. LOAD CURRENT



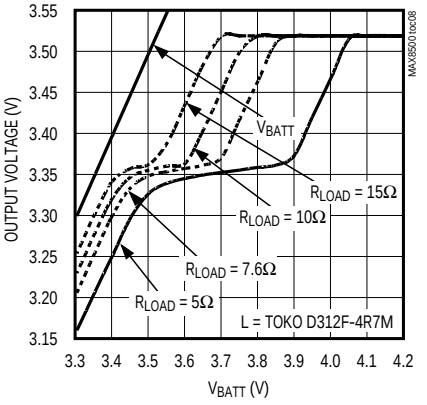
MAX8504 DROPOUT VOLTAGE vs. LOAD CURRENT



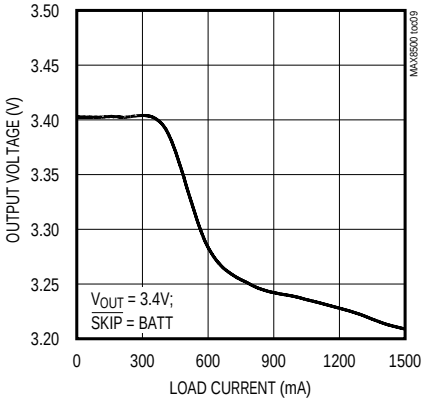
MAX8500/MAX8503 ENTERING REGULATOR DROPOUT REGION



MAX8500/MAX8503 ENTERING REGULATOR DROPOUT REGION



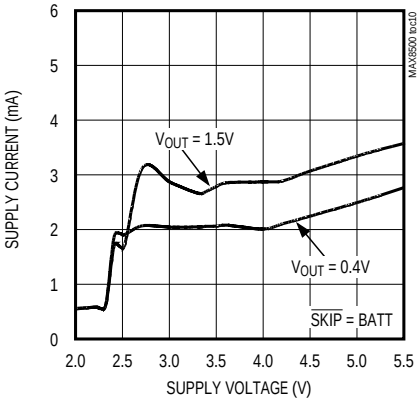
MAX8500/MAX8503 ENTERING REGULATOR DROPOUT REGION



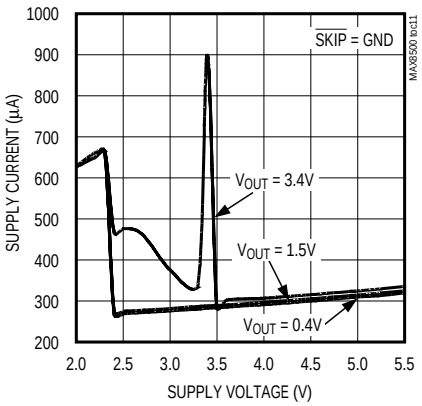
Typical Operating Characteristics (continued)

(V_{BATT} = 3.6V, T_A = +25°C, unless otherwise noted.)

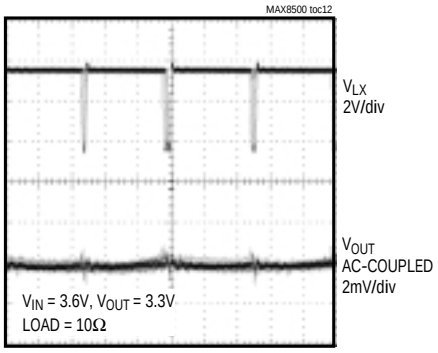
SUPPLY CURRENT vs. SUPPLY VOLTAGE IN PWM MODE



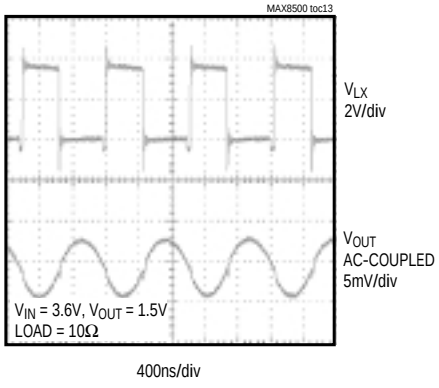
SUPPLY CURRENT vs. SUPPLY VOLTAGE IN NORMAL MODE



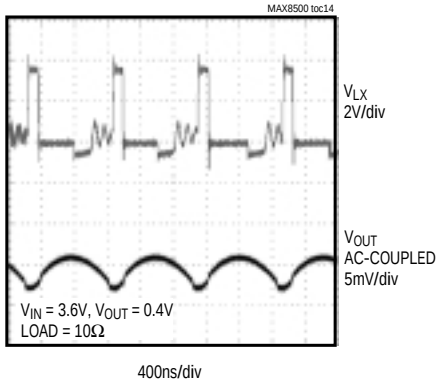
HEAVY-LOAD SWITCHING WAVEFORM



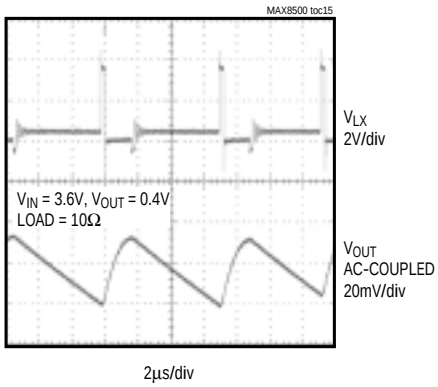
MEDIUM-LOAD SWITCHING WAVEFORM



LIGHT-LOAD SWITCHING WAVEFORM IN PWM MODE



LIGHT-LOAD SWITCHING WAVEFORM IN SKIP MODE

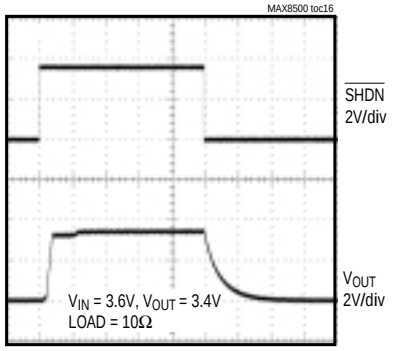


PWM Buck Converters with Bypass FET for N-CDMA/W-CDMA Handsets

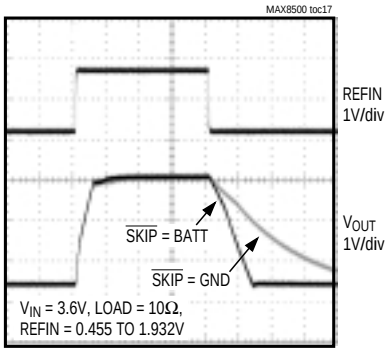
Typical Operating Characteristics (continued)

(V_{BATT} = 3.6V, T_A = +25°C, unless otherwise noted.)

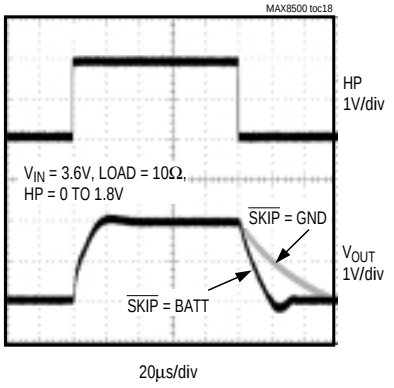
EXITING AND ENTERING SHUTDOWN



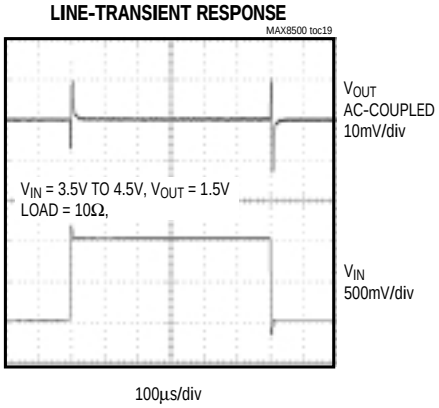
REFIN TRANSIENT RESPONSE



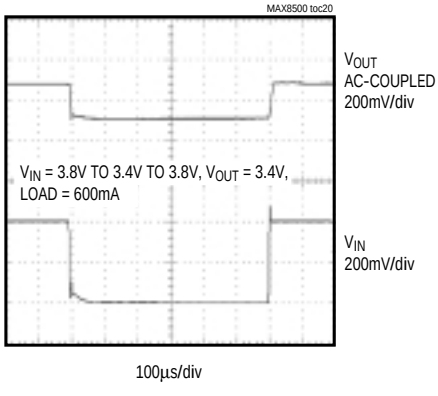
HP TRANSIENT RESPONSE



LINE-TRANSIENT RESPONSE



ENTERING AND EXITING DROPOUT



Pin Description

PIN		NAME	FUNCTION
MAX8500–MAX8503	MAX8504		
1	1	GND	Ground
2	2	REF	Reference Bypass Pin. Connect a 0.22µF ceramic capacitor from this pin to GND.
3	—	REFIN	External Reference Input. Connect REFIN to the output of a DA converter for dynamic adjustment of the output voltage.
—	3	FB	Output Feedback Sense Input. To set the output voltage, connect FB to the center of an external resistive voltage-divider between OUT and GND. FB voltage regulates to 1.25V when HP is logic 0.
4	4	COMP	Compensation. Connect a series resistor and capacitor from this pin to GND to stabilize the regulator (see the *Compensation, Stability, and Output Capacitor* section).
5, 9	9	BATT	IC Supply Voltage Input. Connect to BATTP.
—	5	HP	High-Power Bypass Mode. Connect to GND or logic 0 for OUT to regulate to the voltage set by the external resistors on FB. Drive with logic 1 for OUT to be connected to BATT through the internal bypass PFET.
6	6	PGND	Power Ground
7	7	LX	Inductor Connection to the Drains of the Internal Power MOSFETs. High impedance in shutdown mode.
8	8	BATTP	Power-Supply Voltage Input. Connect to a 2.6V to 5.5V source. Bypass with a low-ESR 10µF capacitor.
10	10	OUT	Regulator Output. Connect OUT directly to the output voltage.
11	11	$\overline{SKIP}$	Skip Control Input. Connect to GND or logic 0 for normal mode. Connect to BATT or logic 1 for forced-PWM mode.
12	12	$\overline{SHDN}$	Shutdown Control Input. Connect to GND or logic 0 for shutdown mode. Connect to BATT or logic 1 for normal operation.

Detailed Description

The MAX8500–MAX8504 PWM step-down DC-to-DC converters with integrated bypass PFET are optimized for low-voltage, battery-powered applications where high efficiency and small size are priorities (such as linear PA applications). An analog control signal dynamically adjusts the MAX8500–MAX8503s' output voltage from 0.4V to V_{BATT} with a settling time <30µs (Figure 1). The MAX8504 uses external feedback resistors to set the output voltage from 1.25V to 2.5V.

The MAX8500–MAX8504 operate at a high 1MHz switching frequency that reduces external component size. Each device includes an internal synchronous rectifier that provides for high efficiency and eliminates the need for an external Schottky diode. The normal operating mode uses constant-frequency PWM switching at medium and heavy loads, and automatically pulse skips at light loads to reduce supply current and extend battery life. An additional forced-PWM mode switches at a constant frequency, regardless of load, to provide a well-controlled spectrum in noise-sensitive applications. Battery life is maximized by low-dropout operation at 100% duty cycle and a 0.1µA (typ) logic-controlled shutdown mode.

PWM Buck Converters with Bypass FET for N-CDMA/W-CDMA Handsets

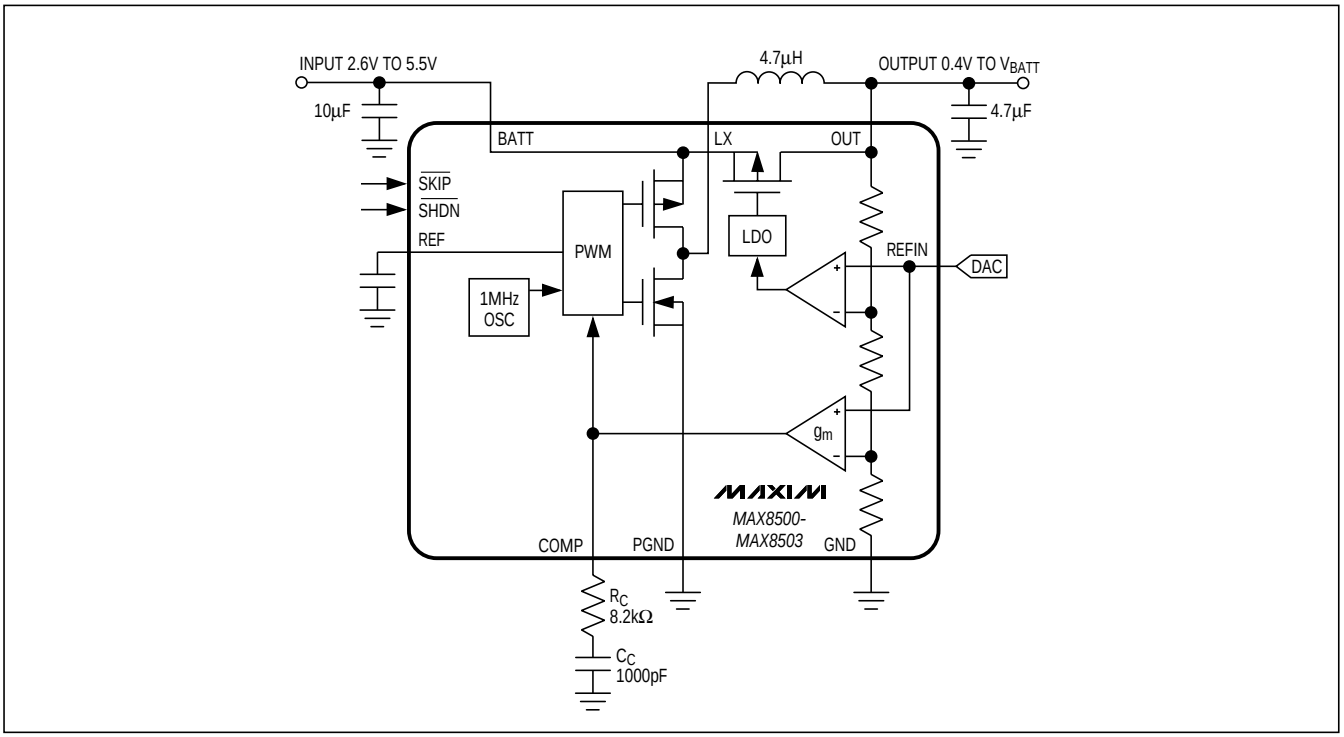


Figure 1. MAX8500–MAX8503 Functional Diagram and Typical Operating Circuit

PWM Control

The MAX8500–MAX8504 use a fixed-frequency, current-mode, PWM controller capable of achieving 100% duty cycle. Current-mode feedback provides cycle-by-cycle current limiting, superior load and line response, as well as overcurrent protection for the internal MOSFET and rectifier. A comparator at the P-channel MOSFET switch detects overcurrent at 1.5A.

During PWM operation, the MAX8500–MAX8504 regulate output voltage by switching at a constant frequency and then modulating the duty cycle with PWM control. The error-amp output, the main switch current-sense signal, and the slope compensation ramp are all summed using a PWM comparator. The comparator modulates the output power by adjusting the peak inductor current during the first half of each cycle based on the output error voltage. The MAX8500–MAX8504 have relatively low AC loop gain coupled with a high gain integrator to enable the use of a small, low-valued output filter capacitor. The resulting load regulation is 0.03% at 0 to 600mA.

Normal Mode Operation

Connecting $\overline{SKIP}$ to GND enables normal operation. This allows automatic PWM control at medium and heavy loads and skip mode at light loads to improve efficiency and reduce quiescent current to 280µA. Operating in normal mode also allows the MAX8500–MAX8504 to pulse skip when the peak inductor current drops below 148mA, corresponding to a load current of approximately 75mA. During skip operation, the MAX8500–MAX8504 switch only as needed to service the load, reducing the switching frequency and associated losses in the internal switch and synchronous rectifier.

There are three steady-state operating conditions for the MAX8500–MAX8504 in normal mode. The device performs in continuous conduction for heavy loads in a manner identical to forced-PWM mode. The inductor current becomes discontinuous at medium loads, requiring the synchronous rectifier to be turned off before the end of a cycle as the inductor current reaches zero. The device enters into skip mode when the converter output voltage exceeds its regulation limit before the inductor current reaches its skip threshold level.

During skip mode, a switching cycle initiates when the output voltage has dropped out of regulation. The P-channel MOSFET switch turns on and conducts cur-

rent to the output filter capacitor and load until the inductor current reaches the skip peak current limit. Then the main switch turns off, and the magnetic field in the inductor collapses, while current flows through the synchronous rectifier to the output filter capacitor and the load. The synchronous rectifier is turned off when the inductor current reaches zero. The MAX8500–MAX8504 wait until the skip comparator senses a low output voltage again.

Forced-PWM Operation

Connect $\overline{SKIP}$ to BATT for forced-PWM operation. Forced-PWM operation is desirable in sensitive RF and data-acquisition applications to ensure that switching harmonics do not interfere with sensitive IF and data-sampling frequencies. A minimum load is not required during forced-PWM operation since the synchronous rectifier passes reverse-inductor current as needed to allow constant-frequency operation with no load. Forced-PWM operation uses higher supply current with no load (3.3mA typ) compared to skip mode (280µA typ).

100% Duty-Cycle Operation and Dropout

The maximum on-time can exceed one internal oscillator cycle, which permits operation at 100% duty cycle. Near dropout, cycles may be skipped, reducing switching frequency. However, voltage ripple remains small because the current ripple is still low. As the input voltage drops even further, the duty cycle increases until the internal P-channel MOSFET stays on continuously. Dropout voltage at 100% duty cycle is the output current multiplied by the sum of the internal PMOS on-resistance (0.35Ω typ) and the inductor resistance. Once the output voltage drops by 5%, the PFET bypass LDO (MAX8500–MAX8503) turns on and reduces the dropout voltage. The dropout in the bypass PFET equals the load current multiplied by the on-resistance (0.25Ω typ) in parallel with the buck converter and inductor dropout resistance.

Undervoltage Lockout (UVLO)

The MAX8500–MAX8504 do not operate with battery voltages below the UVLO threshold of 2.35V (typ). The output remains off until the supply voltage exceeds the UVLO threshold. This guarantees the integrity of the output voltage regulation.

Synchronous Rectification

An N-channel, synchronous rectifier operates during the second half of each switching cycle (off-time). When the inductor current falls below the N-channel current comparator threshold or when the PWM reaches the end of the oscillator period, the synchronous rectifier turns off. This prevents reverse current from the output to the input in pulse-skipping mode. During PWM operation, the I_{LIMN} threshold adjusts to permit reverse current during light loads. This allows regulation with a constant switching frequency and eliminates minimum load requirements for fixed-frequency operation.

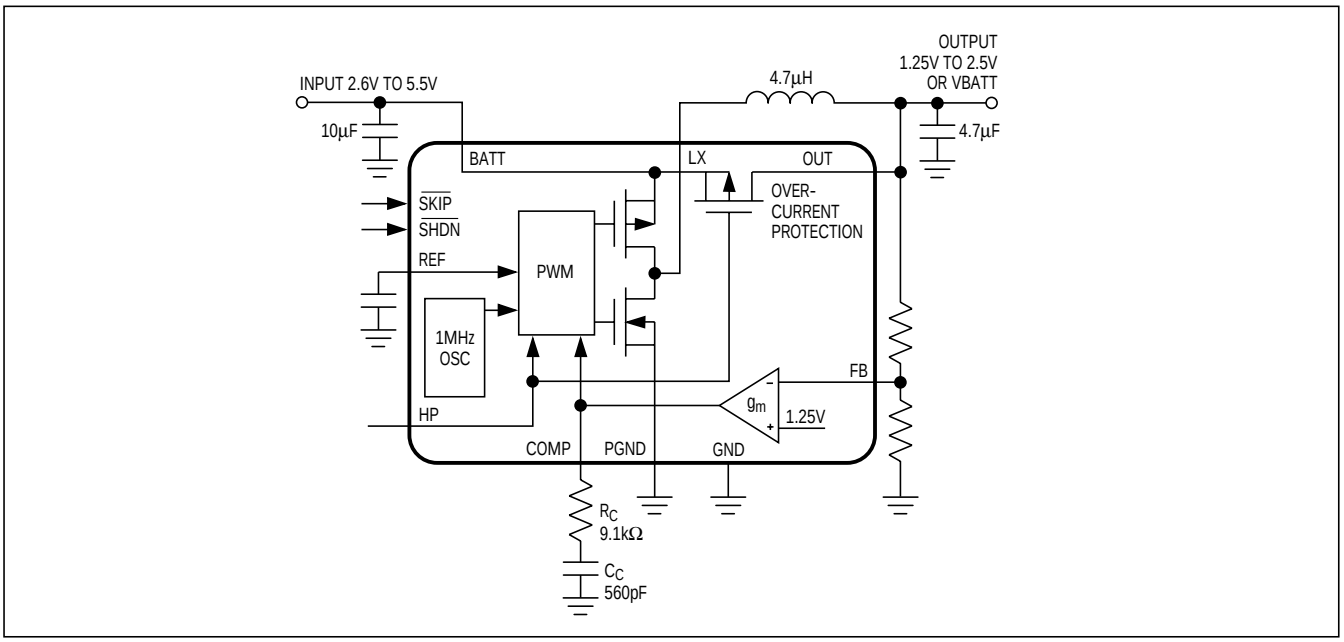


Figure 2. MAX8504 Functional Diagram and Typical Operating Circuit

PWM Buck Converters with Bypass FET for N-CDMA/W-CDMA Handsets

High-Power Bypass Mode (MAX8504)

A high-power bypass mode is available on the MAX8504 for use when a PA transmits at high power. This mode connects OUT to BATT through the bypass PFET. Additionally, the PWM buck converter is forced into 100% duty cycle to further reduce dropout.

Shutdown Mode

Driving $\overline{SHDN}$ to GND places the MAX8500–MAX8504 in shutdown mode. In shutdown, the reference, control circuitry, internal switching MOSFET, and synchronous rectifier turn off and the output becomes high impedance. Input current falls to 0.1µA (typ) during shutdown mode. Drive $\overline{SHDN}$ high for normal operation.

Current-Sense Comparators

The MAX8500–MAX8504 use several internal current-sense comparators. In PWM operation, the PWM comparator terminates the cycle-by-cycle on-time and provides improved load and line response. A second current-sense comparator used across the P-channel switch controls entry into skip mode. A third current-sense comparator monitors current through the internal N-channel MOSFET to prevent excessive reverse currents and determine when to turn off the synchronous rectifier. A fourth comparator used at the P-channel MOSFET detects overcurrent. A fifth comparator used at the bypass/LDO P-channel MOSFET detects overcurrent in the HP mode or at dropout. This protects the system, external components, and internal MOSFETs under overload conditions.

Applications Information

Setting the Output Voltage

Using a DAC (MAX8500–MAX8503)

The MAX8500–MAX8503 are optimized for highest system efficiency when applying power to a linear PA in CDMA handsets. When transmitting at less than full power, the supply voltage to the PA is lowered from V_{BATT} to as low as 0.4V to greatly reduce battery current. Figure 3 shows the typical CDMA PA load profile. The use of DC-to-DC converters such as the MAX8500–MAX8503 dramatically extends talk time in these applications.

The MAX8500–MAX8503s' output voltage is dynamically adjustable from 0.4V to V_{BATT} by the use of the REFIN input. The gain from V_{REFIN} to V_{OUT} is internally set to 1.76X (MAX8500 and MAX8502) or 2X (MAX8501 and MAX8503). V_{OUT} can be adjusted during operation by driving REFIN with an external DAC. The MAX8500–MAX8503 output responds to full-scale change in voltage and current in <30µs.

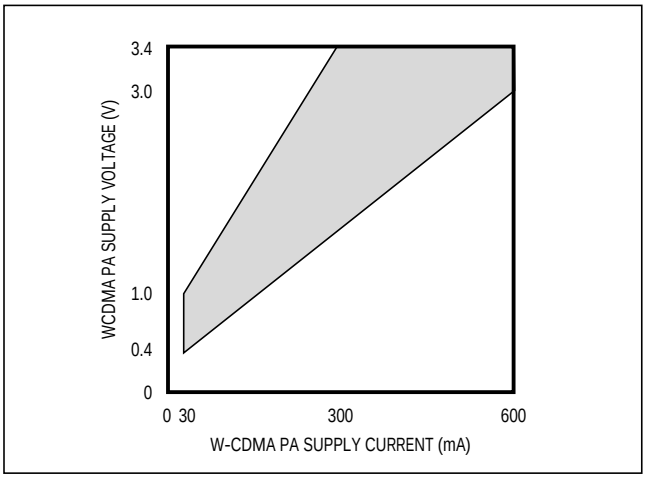


Figure 3. Typical W-CDMA Power Amplifier Load Profile

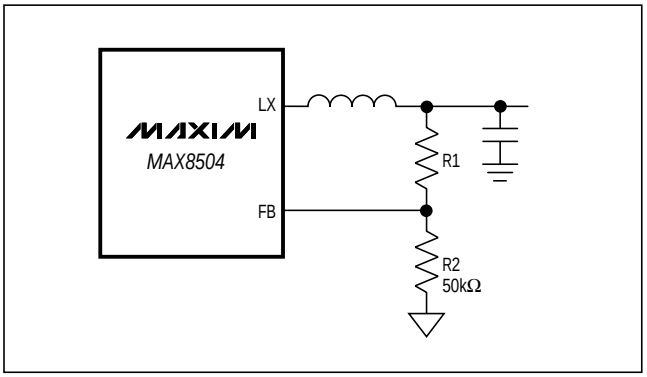


Figure 4. Setting the Adjustable Output Voltage

Using External Divider (MAX8504)

The MAX8504 is intended for two-step V_{CC} control applications where high efficiency is a priority. Select an output voltage between 1.25V and V_{BATT} by connecting FB to a resistive divider between the output and GND (Figure 4). Select feedback resistor R2 in the 5kΩ to 50kΩ range. R1 is then given by:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 1.25V.

Input Capacitor Selection

Capacitor ESR is a major contributor to input ripple in high-frequency DC-to-DC converters. Ordinary aluminum electrolytic capacitors have high ESR and should be avoided. Low-ESR tantalum capacitors or polymer capacitors are better and provide a compact solution for space-constrained surface-mount designs. Ceramic capacitors have the lowest ESR overall.

The input filter capacitor reduces peak currents and noise at the input voltage source. Connect a low-ESR bulk capacitor (≥10µF typ) to the input. Select this bulk capacitor to meet the input ripple requirements and voltage rating rather than capacitance value. Use the following equation to calculate the maximum RMS input current:

$$I_{RMS} = \frac{I_{OUT}}{V_{IN}} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}$$

Compensation, Stability, and Output Capacitor

The MAX8500–MAX8504 are externally compensated by placing a resistor and a capacitor (see Figures 1 and 2, R_C and C_C) in series from COMP to GND. An additional capacitor (C_f) may be required from COMP to GND if high-ESR output capacitors are used. The capacitor integrates the current from the transconductance amplifier, averaging output capacitor ripple. This sets the device speed for transient response and allows the use of small ceramic output capacitors because the phase-shifted capacitor ripple does not disturb the current-regulation loop. The resistor sets the proportional gain of the output error voltage by a factor $g_m \times R_C$. Increasing this resistor also increases the sensitivity of the control loop to output ripple.

The resistor and capacitor set a compensation zero that defines the system's transient response. The load creates a dynamic pole, shifting in frequency with changes in load. As the load decreases, the pole frequency shifts to the left. System stability requires that the compensation zero must be placed to ensure adequate phase margin (at least 30° at unity gain). See Figures 1 and 2 for R_C and C_C recommended values.

Inductor Selection

A 4µH to 6µH inductor is recommended for most applications. For best efficiency, the inductor's DC resistance should be <400mΩ. Saturation current (I_{SAT}) should be greater than the maximum DC load at the PA's supply plus half the inductor current ripple. Two-step V_{CC} applications typically require very small inductors with I_{SAT} in the 200mA to 300mA region. See Table 1 and Table 2 for recommended inductors and manufacturers.

PC Board Layout and Routing

High switching frequencies and large peak currents make PC board layout a very important part of design. Good design minimizes EMI, noise on the feedback paths, and voltage gradients in the ground plane, all of which can result in instability or regulation errors. Connect the inductor, input filter capacitor, and output filter capacitor as close together as possible and keep their traces short, direct, and wide. Connect their ground pins at a single common node in a star ground configuration. The external voltage-feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces, such as those from the LX pin, away from the voltage-feedback network. Position the bypass capacitors as close as possible to their respective pins to minimize noise coupling. For optimum performance, place input and output capacitors as close to the device as possible. Connect GND and PGND directly under the IC to the exposed paddle. The MAX8504 evaluation kit manual illustrates an example PC board layout and routing scheme.

Chip Information

TRANSISTOR COUNT: 2530

PROCESS: BiCMOS

Table 1. Suggested Inductors

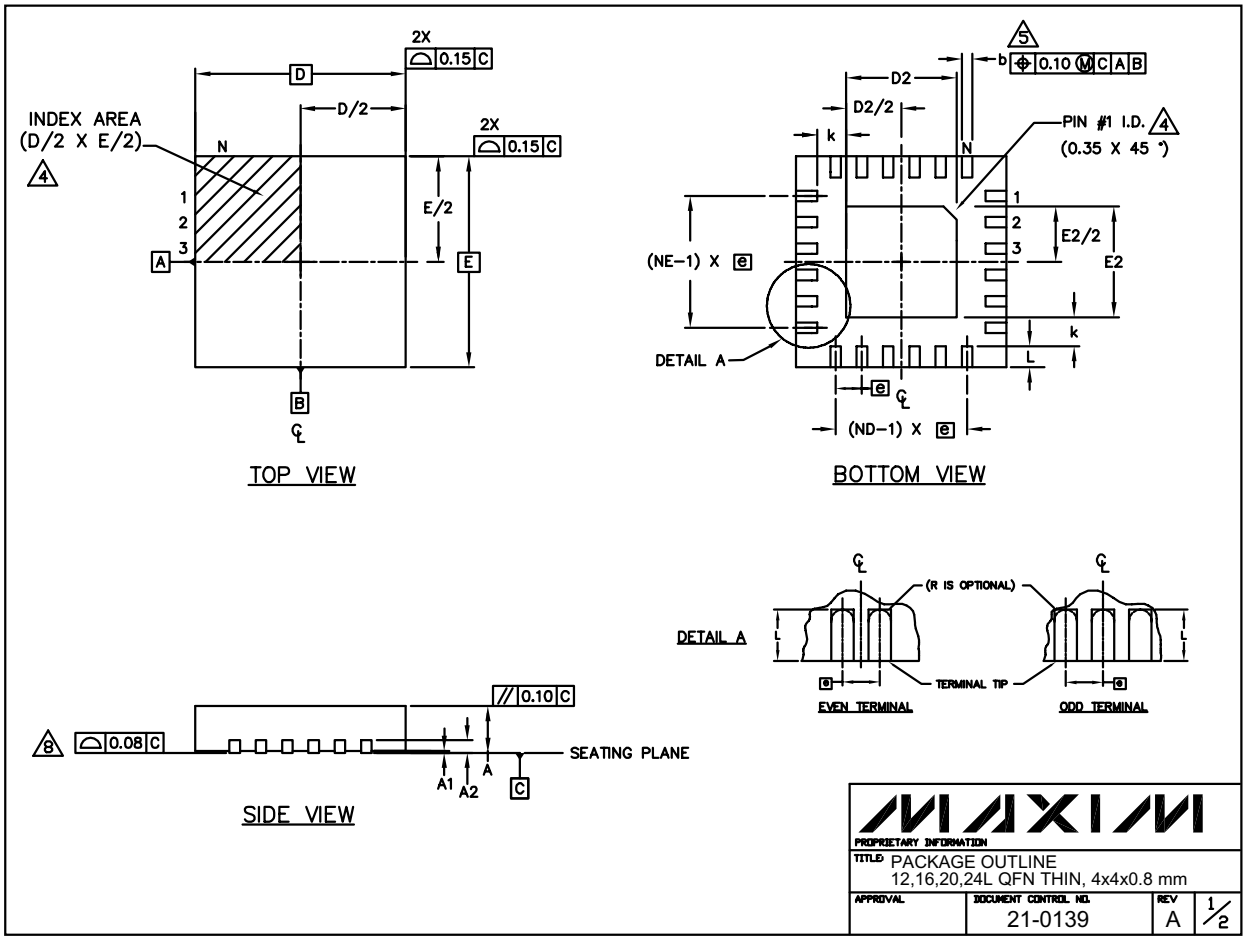
MANUFACTURER	PART NO.	INDUCTANCE (µH)	ESR (mΩ)	SATURATION CURRENT (A)	DIMENSIONS (mm)
Murata	LQH3C	4.7	200	0.45	2.5 x 3.2 x 2
Sumida	CDRH2D18	4.7	63	0.63	3.2 x 3.2 x 2
Taiyo Yuden	LBLQ2016	4.7	250	0.21	1.6 x 2 x 1.6
Toko	D312F	4.7	320	0.83	3.6 x 3.6 x 1.2

Table 2. Manufacturers of Suggested Components

MANUFACTURER	PHONE	WEBSITE
Murata	770-436-1300	www.murata.com
Sumida	847-956-0666 (USA) 81-3-3607-5111 (Japan)	www.sumida.com
Taiyo Yuden	408-573-4150	www.t-yuden.com
Toko	847-297-0070	www.tokoam.com

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



PWM Buck Converters with Bypass FET for N-CDMA/W-CDMA Handsets

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0139	REV A	2/2