

SN54BCT620A, SN74BCT620A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS001B – SEPTEMBER 1987 – REVISED NOVEMBER 1993

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- P-N-P Inputs Reduce DC Loading
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Plastic and Ceramic 300-mil DIPs (J, N)

description

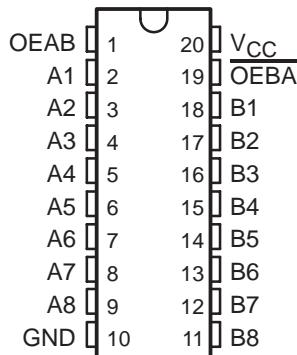
The 'BCT620A bus transceiver is designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing. The 'BCT620A provides inverted data at its outputs.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEAB and \overline{OEBA}) inputs.

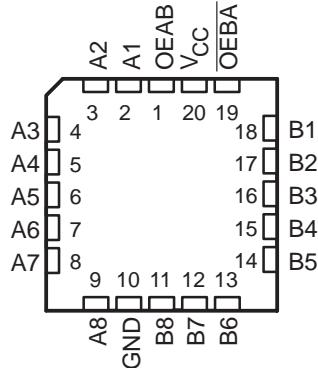
The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and \overline{OEBA} . When both OEAB and \overline{OEBA} are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. In this way, each output reinforces its input in this configuration.

The SN54BCT620A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT620A is characterized for operation from 0°C to 70°C .

SN54BCT620A . . . J OR W PACKAGE
SN74BCT620A . . . DW OR N PACKAGE
(TOP VIEW)



SN54BCT620A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
OEBA	OEAB	
L	L	\overline{B} data to A bus
L	H	\overline{B} data to A bus, A data to B bus
H	L	Isolation
H	H	\overline{A} data to B bus

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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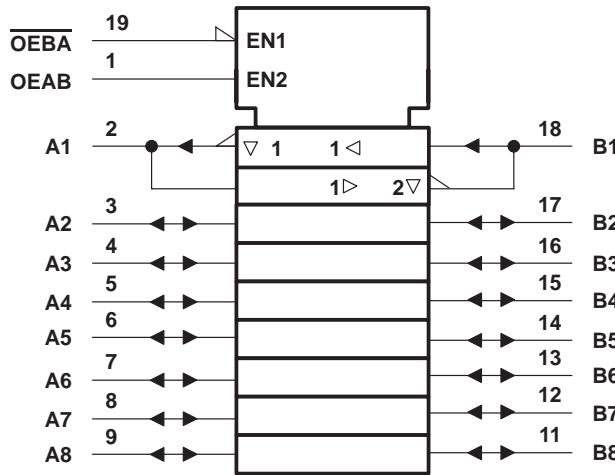
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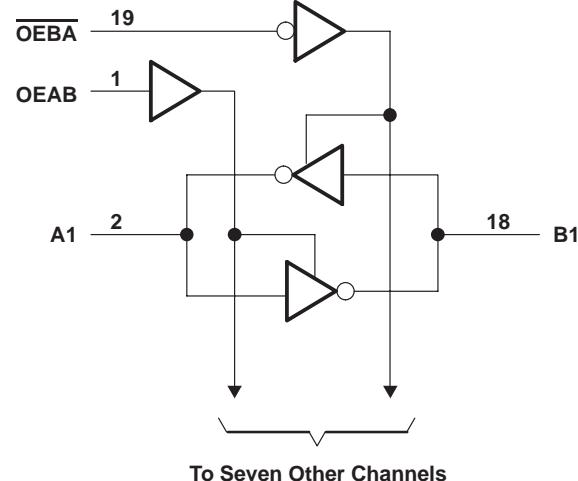
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT620A			SN74BCT620A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2		2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	High-level output current	A port		-3			-3	mA
		B port		-12			-15	
I _{OL}	Low-level output current	A port		20			24	mA
		B port		48			64	
T _A	Operating free-air temperature	-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54BCT620A			SN74BCT620A			UNIT
			MIN	TYPT [†]	MAX	MIN	TYPT [†]	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	A port	V _{CC} = 4.5 V	I _{OH} = -1 mA	2.5	3.4	2.5	3.4		V
			I _{OH} = -3 mA	2.4	3.3	2.4	3.3		
	B port	V _{CC} = 4.5 V	I _{OH} = -3 mA	2.4	3.3	2.4	3.3		
			I _{OH} = -12 mA	2	3.2				
			I _{OH} = -15 mA			2	3.1		
V _{OL}	A port	V _{CC} = 4.5 V	I _{OL} = 20 mA	0.3	0.5				V
			I _{OL} = 24 mA			0.35	0.5		
	B port	V _{CC} = 4.5 V	I _{OL} = 48 mA	0.38	0.55				
			I _{OL} = 64 mA			0.42	0.55		
I _I	A or B port OEAB or <u>OEBA</u>	V _{CC} = 5.5 V, V _I = 5.5 V			1		1		mA
					0.1		0.1		
I _{IH} [‡]	A or B port OEAB or <u>OEBA</u>	V _{CC} = 5.5 V, V _I = 2.7 V			70		70		μA
					20		20		
I _{IL} [‡]	A or B port OEAB or <u>OEBA</u>	V _{CC} = 5.5 V, V _I = 0.5 V			-0.65		-0.65		mA
					-0.6		-0.6		
I _{OS} [§]	A port B port	V _{CC} = 5.5 V, V _O = 0			-60	-150	-60	-150	mA
					-100	-225	-100	-225	
I _{CCL}	A to B	V _{CC} = 5.5 V			53	84	53	84	mA
I _{ICCH}	A to B	V _{CC} = 5.5 V			23	37	23	37	mA
I _{ICCZ}		V _{CC} = 5.5 V			4	10	4	10	mA
C _i	OEAB or <u>OEBA</u>	V _{CC} = 5 V, V _I = 2.5 V or 0.5 V			5		5		pF
C _{io}	A to B	V _{CC} = 5 V, V _O = 2.5 V or 0.5 V			9		9		pF
	B to A				12		12		

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

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switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†			UNIT	
			'BCT620A			SN54BCT620A		SN74BCT620A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	0.6	3.4	5.2	0.6	6.2	0.6	5.8	ns
t _{PHL}			0.1	1.9	3.4	0.1	3.7	0.1	3.6	
t _{PLH}	B	A	0.9	4.1	6	0.9	7.2	0.9	6.9	ns
t _{PHL}			0.1	2	3.7	0.1	4	0.1	3.9	
t _{PZH}	<u>OEBA</u>	A	3.5	7.2	9.2	3.5	10.9	3.5	10.6	ns
t _{PZL}			3.7	7.6	9.9	3.7	11.5	3.7	11.1	
t _{PHZ}	<u>OEBA</u>	A	3.1	5.3	8.6	3.1	10.8	3.1	10	ns
t _{PLZ}			1.3	4.4	6.9	1.3	8.3	1.3	7.8	
t _{PZH}	<u>OEAB</u>	B	2	5.3	6.7	2	7.9	2	7.4	ns
t _{PZL}			2.9	6.1	8.1	2.9	9.2	2.9	9	
t _{PHZ}	<u>OEAB</u>	B	2.1	5.2	7	2.1	8.5	2.1	8.1	ns
t _{PLZ}			0.1	3.7	5.3	0.1	6	0.1	5.9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9075001M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9075001MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9075001MRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
5962-9075001MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
5962-9075001MSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SN74BCT620ADW	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
SN74BCT620ADW	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
SN74BCT620AN	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SN74BCT620AN	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SNJ54BCT620AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54BCT620AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54BCT620AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54BCT620AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
SNJ54BCT620AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54BCT620AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

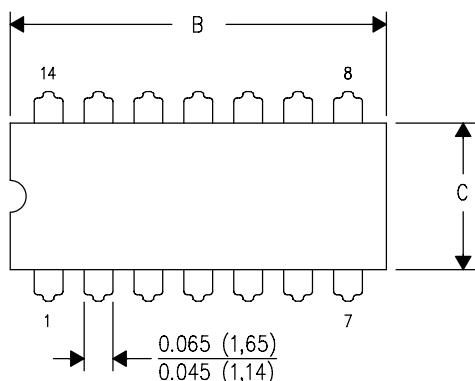
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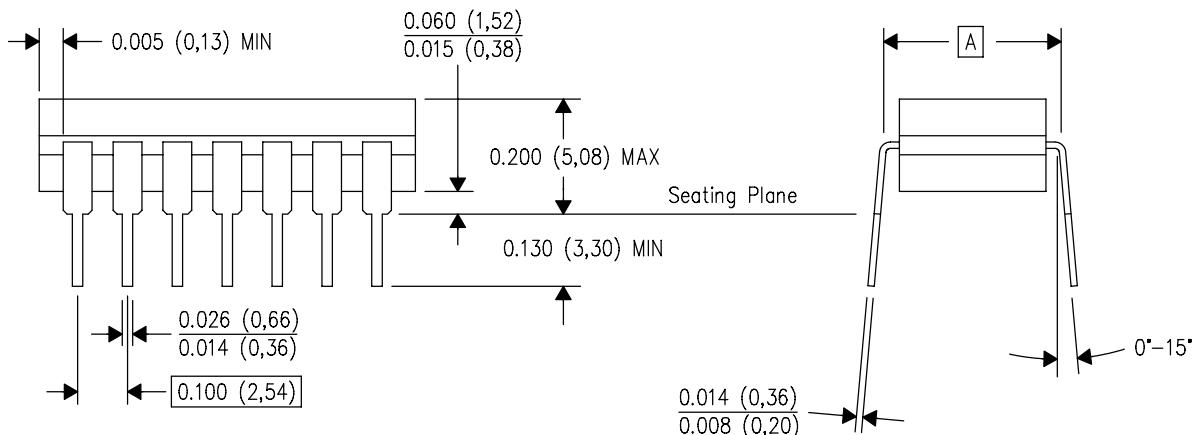
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



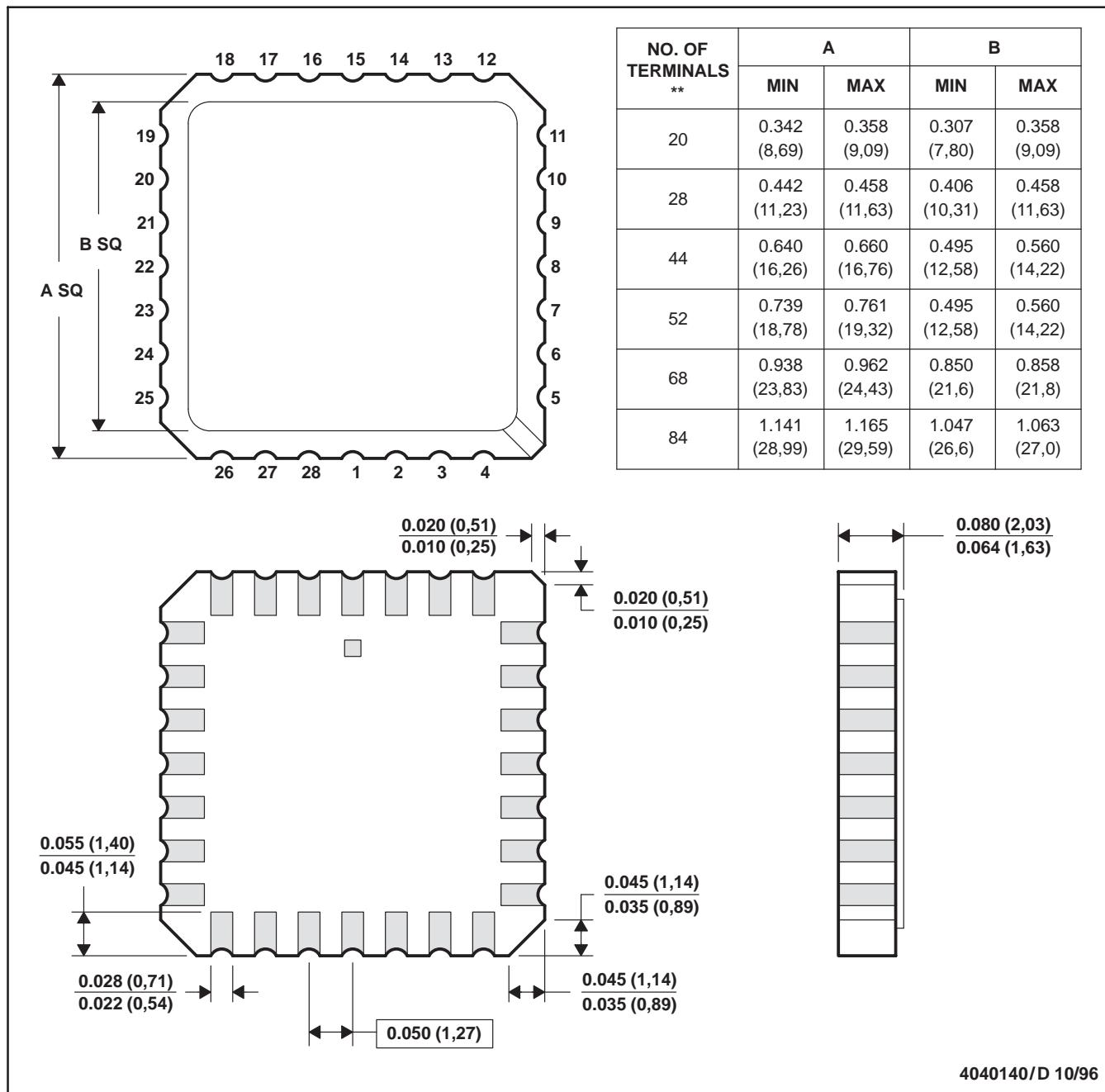
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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

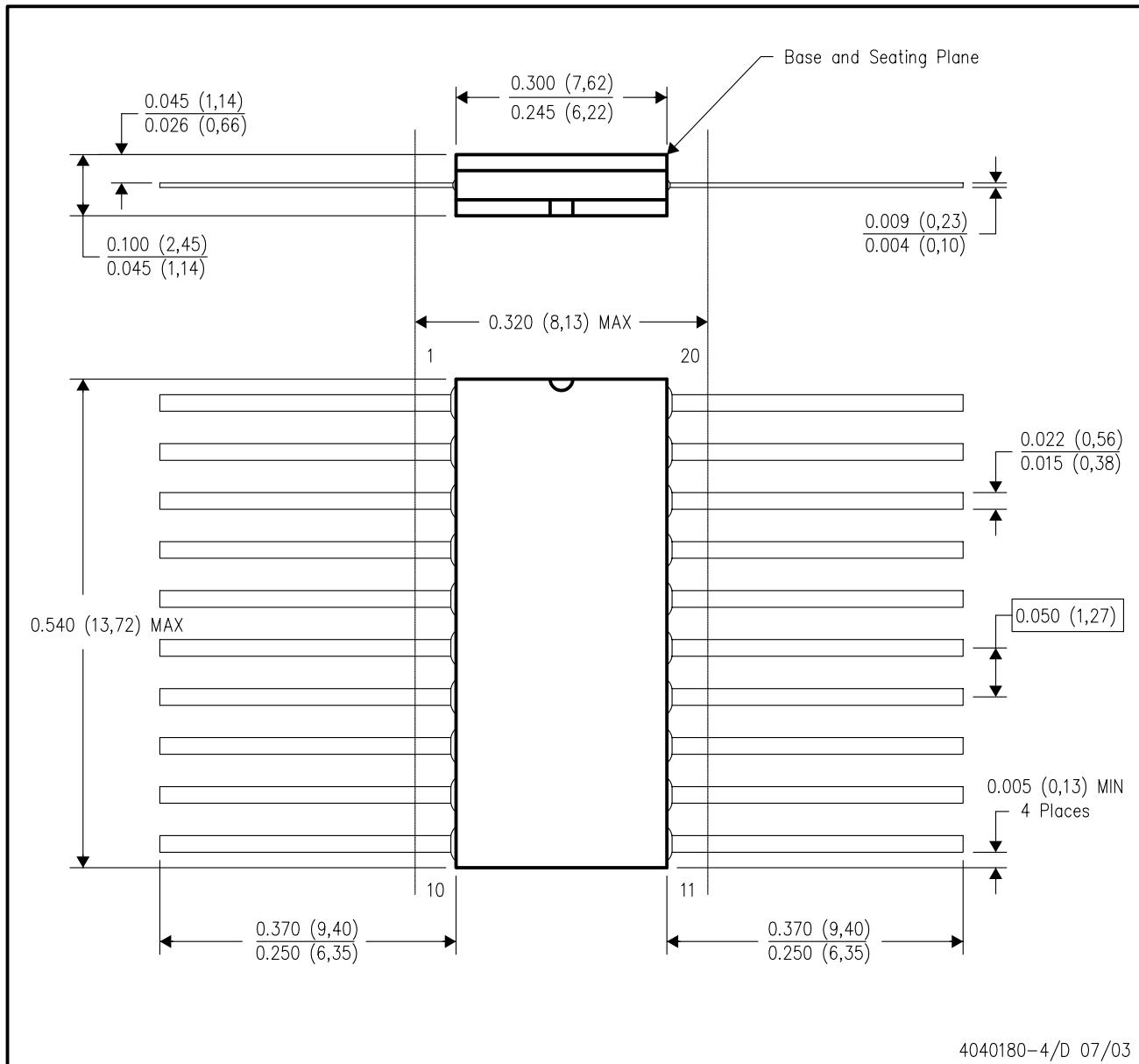


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

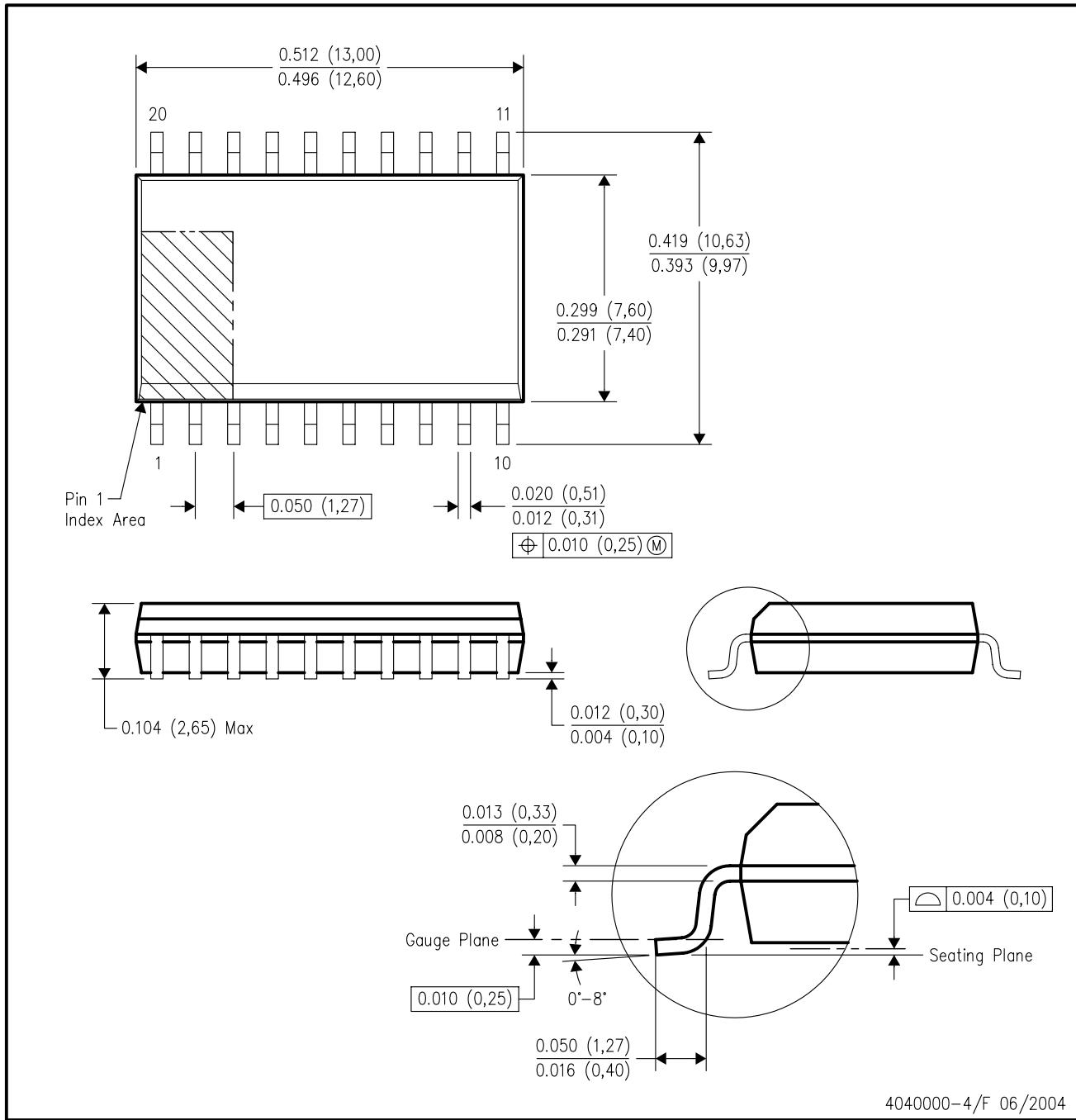


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



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