



MOTOROLA

MC14520B
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MC14521B

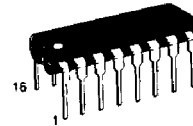
24-STAGE FREQUENCY DIVIDER

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to $2^{24} = 16,777,216$. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

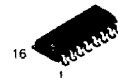
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

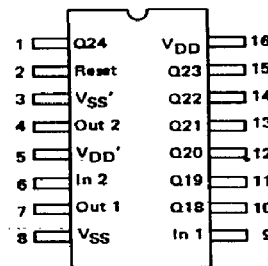
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	- 65 to + 150	$^\circ\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^\circ\text{C}$

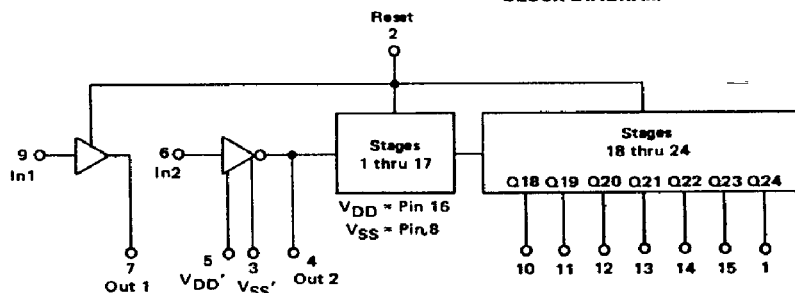
*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P and D/DW" Packages: - 7.0 mW/ $^\circ\text{C}$ From 65°C To 125°C
Ceramic "L" Packages: - 12 mW/ $^\circ\text{C}$ From 100°C To 125°C

PIN ASSIGNMENT



BLOCK DIAGRAM



OUTPUT	COUNT CAPACITY
Q18	$2^{18} = 262,144$
Q19	$2^{19} = 524,288$
Q20	$2^{20} = 1,048,576$
Q21	$2^{21} = 2,097,152$
Q22	$2^{22} = 4,194,304$
Q23	$2^{23} = 8,388,608$
Q24	$2^{24} = 16,777,216$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 "0" Level	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD} "1" Level	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) "0" Level	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) "1" Level	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) Pins 4 & 7 (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) Pins 1, 10, (V _{OH} = 9.5 Vdc) 11, 12, 13, 14 (V _{OH} = 13.5 Vdc) and 15 (V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
		10	-0.62	—	-0.5	-0.9	—	-0.35	—	
		15	-1.8	—	-1.5	-3.5	—	-1.1	—	
		5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (0.42 μA/kHz) f + I _{DD} I _T = (0.85 μA/kHz) f + I _{DD} I _T = (1.40 μA/kHz) f + I _{DD}							μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

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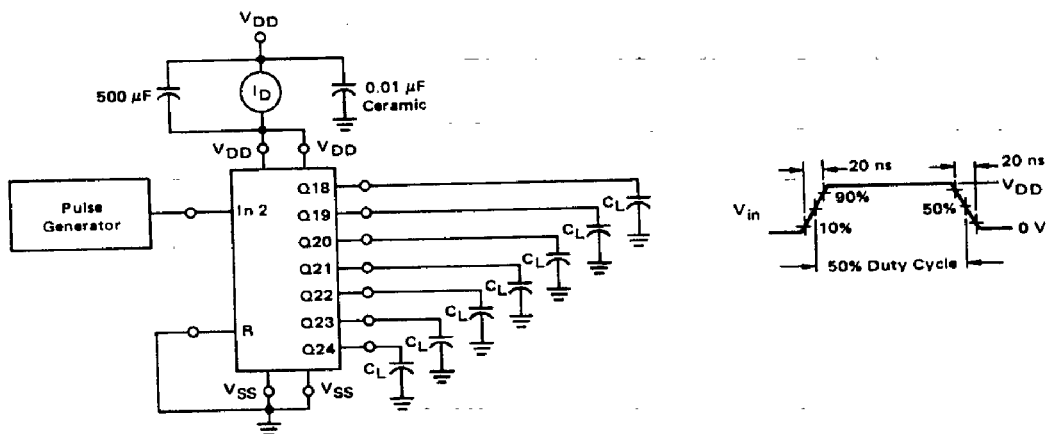
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time (Counter Outputs) $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q18 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 4415 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 1687 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 1275 \text{ ns}$ Clock to Q24 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 5915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 2167 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 1675 \text{ ns}$	t_{PHL}, t_{PLH}	5.0 10 15 5.0 10 15	— — — — — —	4.5 1.7 1.3 6.0 2.2 1.7	9.0 3.5 2.7 12 4.5 3.5	μs
Propagation Delay Time Reset to Q_n $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1215 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 467 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 350 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	1300 500 375	2600 1000 750	ns
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	385 150 120	140 55 40	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.5 9.0 12	2.0 5.0 6.5	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	1400 600 450	700 300 225	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	30 0 -40	-200 -160 -110	— — —	ns

*The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



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FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

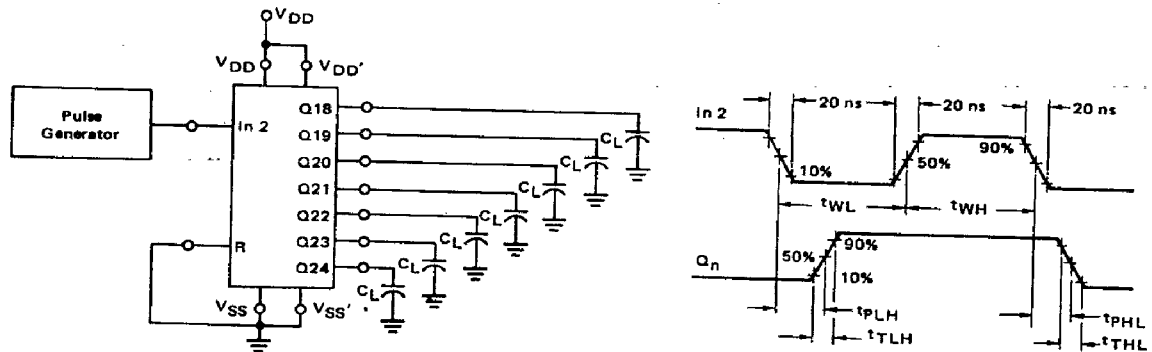
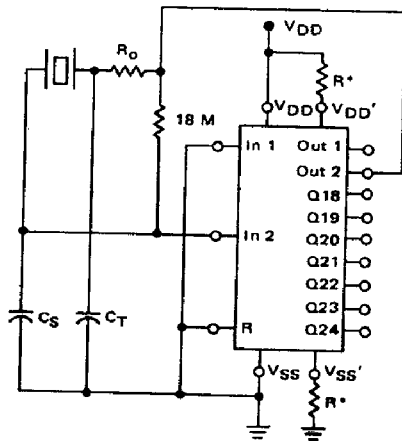


FIGURE 3 – CRYSTAL OSCILLATOR CIRCUIT



*Optional for low power operation.
10 kΩ < R < 70 kΩ

FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, RS	1.0	6.2	kΩ
External Resistor/Capacitor Values			
RO	47	750	kΩ
CT	82	82	pF
CS	20	20	pF
Frequency Stability			
Frequency Change as a Function of VDD (TA = 25°C)			
VDD Change from 5.0 V to 10 V	+6.0	+2.0	ppm
VDD Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (VDD = 10 V)			
TA Change from -55°C to +25°C			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
TA Change from +25°C to +125°C			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

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FIGURE 5 – RC OSCILLATOR STABILITY

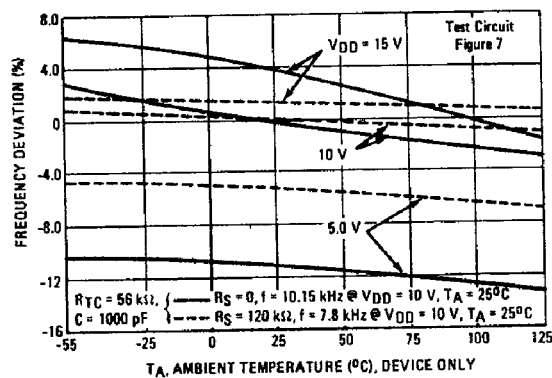


FIGURE 6 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

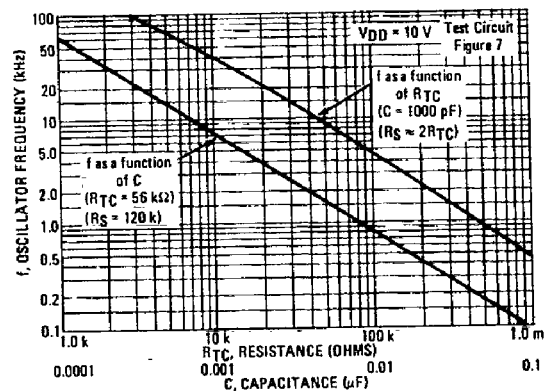


FIGURE 7 – RC OSCILLATOR CIRCUIT

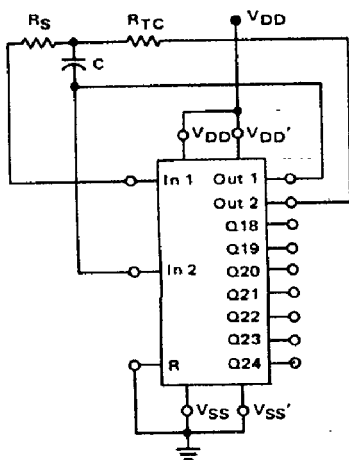
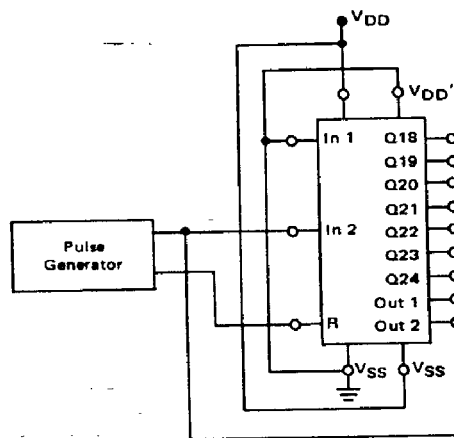


FIGURE 8 – FUNCTIONAL TEST CIRCUIT



FUNCTIONAL TEST SEQUENCE

	INPUTS		OUTPUTS			COMMENTS
	Reset	In 2	Out 2	VSS'	VDD'	
A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.	1	0	0	VDD	Gnd	Counter is in three 8-stage sections in parallel mode. Counter is reset. In 2 and Out 2 are connected together.
	0	1	1	Gnd	VDD	First "0" to "1" transition on In 2, Out 2 node.
		0	0			255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
		1	1			
		0	0			
		1	1			The 255th "0" to "1" transition.
		0	0			1
		1	0			1
		0	1			0
		1	0			Counter converted back to 24-stages in series mode.
		1	0			Out 2 converts back to an output.
		0	1			Counter ripples from an all "1" state to an all "0" stage.

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LOGIC DIAGRAM

