

Dual N-Channel 30-V (D-S) MOSFET

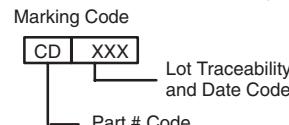
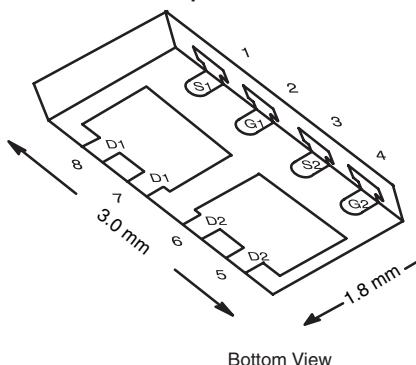
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
30	0.031 at $V_{GS} = 10$ V	6	8 nC
	0.040 at $V_{GS} = 4.5$ V	6	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

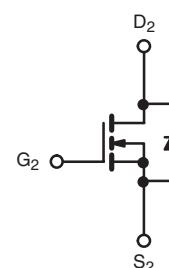
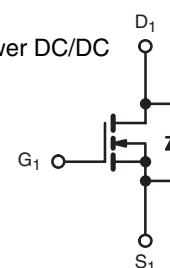


PowerPAK® ChipFET® Dual



APPLICATIONS

- Network
- System Power DC/DC



Ordering Information: Si5906DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	6 ^a	A
		6 ^a	
		6 ^{a, b, c}	
		5.3 ^{b, c}	
		25	
Pulsed Drain Current	I_{DM}	6 ^a	
Continuous Source-Drain Diode Current	I_S	1.9 ^{b, c}	
Maximum Power Dissipation	P_D	10.4	W
		6.7	
		2.3 ^{b, c}	
		1.5 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	43	55
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	9.5	12 °C/W

Notes:

- a. Package limited
- b. Surface Mounted on 1" x 1" FR4 board.
- c. $t = 5$ s.
- d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 105 °C/W.

Si5906DU

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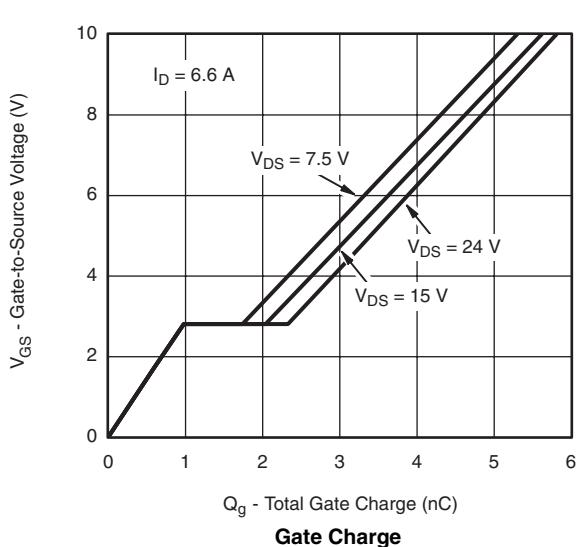
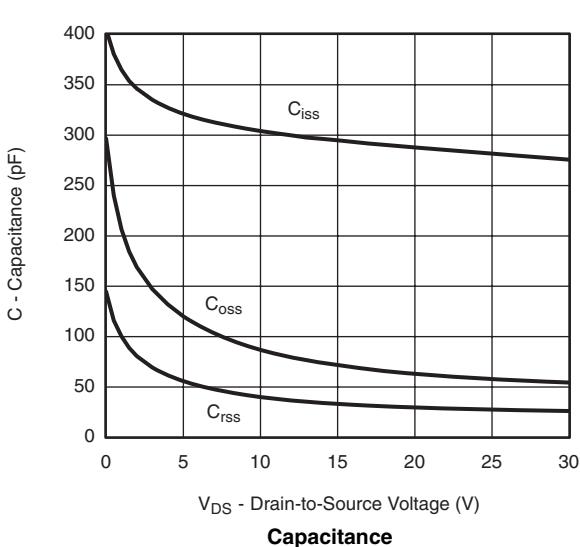
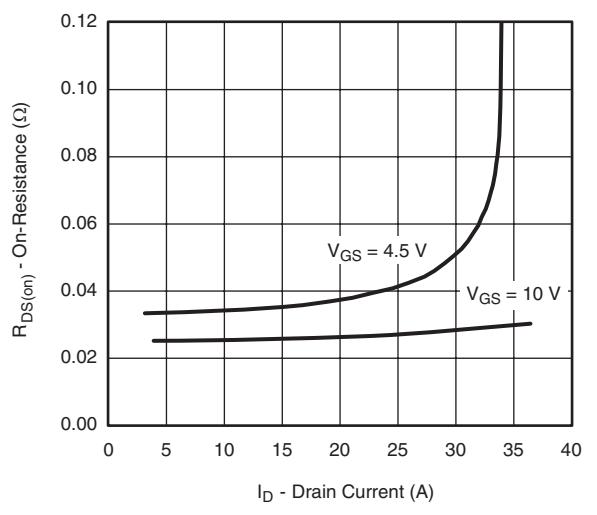
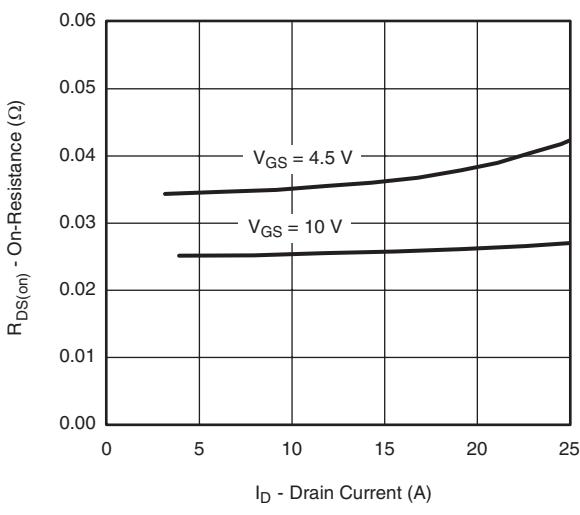
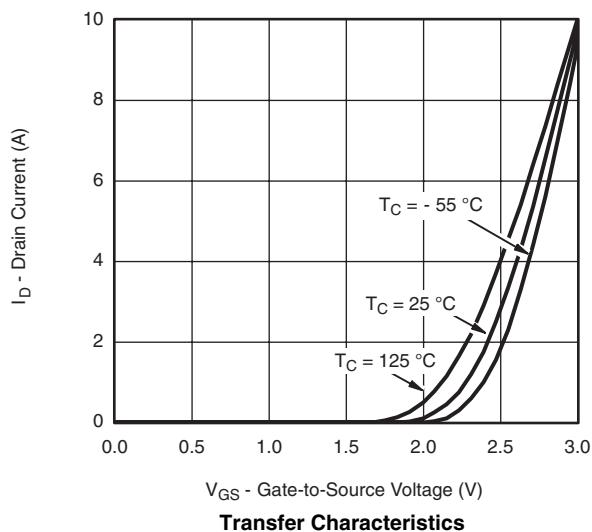
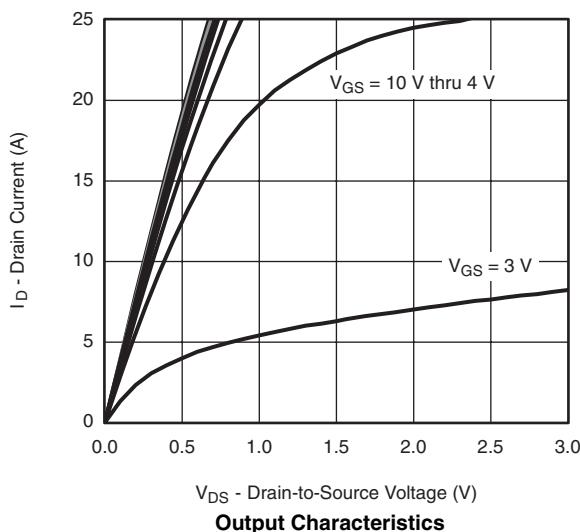
**SPECIFICATIONS** $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		33		$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 3.5		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1.2		2.2	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 4.8 \text{ A}$		0.025	0.031	Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 4.1 \text{ A}$		0.033	0.040	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 4.8 \text{ A}$		14		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		300		pF
Output Capacitance	C_{oss}			72		
Reverse Transfer Capacitance	C_{rss}			34		
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 6.6 \text{ A}$		5.7	8.6	nC
				2.9	4.4	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 6.6 \text{ A}$		1.0		
Gate-Drain Charge	Q_{gd}			1.1		
Gate Resistance	R_g	$f = 1 \text{ MHz}$	0.3	1.8	3.6	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 15 \text{ V}$, $R_L = 2.8 \Omega$ $I_D \geq 5.3 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$		10	15	ns
Rise Time	t_r			90	135	
Turn-Off Delay Time	$t_{d(\text{off})}$			12	20	
Fall Time	t_f			50	75	
Turn-On Delay Time	$t_{d(\text{on})}$			5	10	
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(\text{off})}$			12	20	
Fall Time	t_f			5	10	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			6	A
Pulse Diode Forward Current	I_{SM}				25	
Body Diode Voltage	V_{SD}	$I_S = 6 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 5.3 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		12	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			5	10	
Reverse Recovery Fall Time	t_a			6		
Reverse Recovery Rise Time	t_b			6		

Notes:

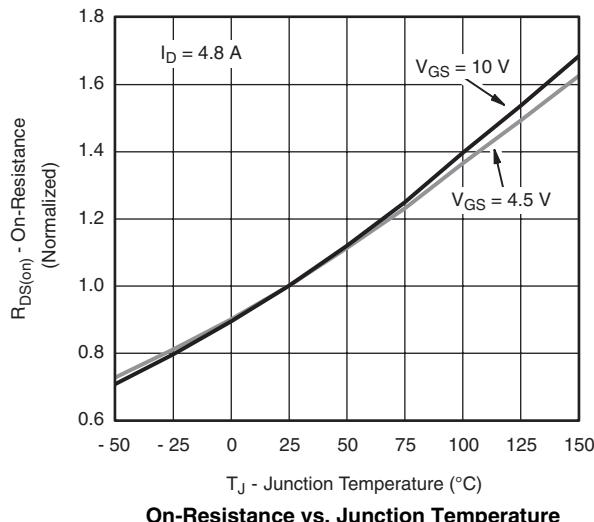
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

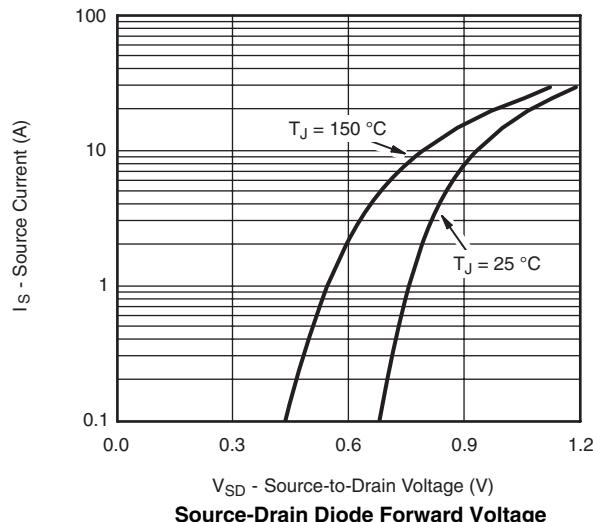
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


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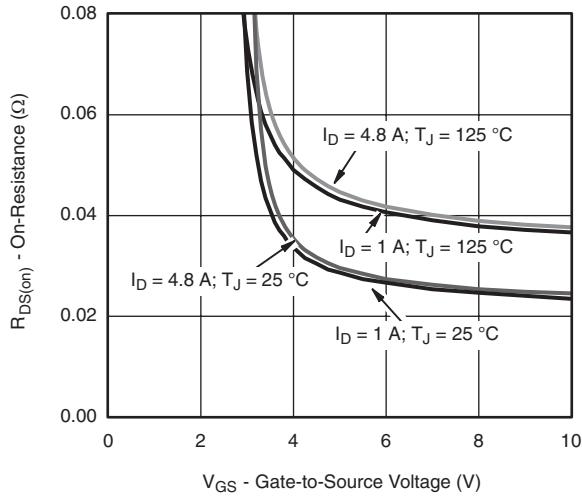
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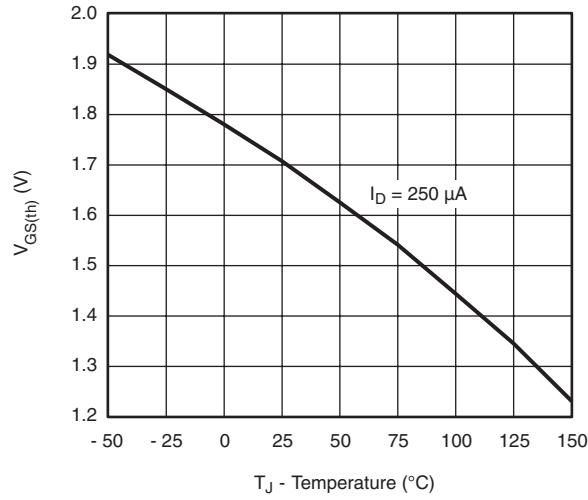
On-Resistance vs. Junction Temperature



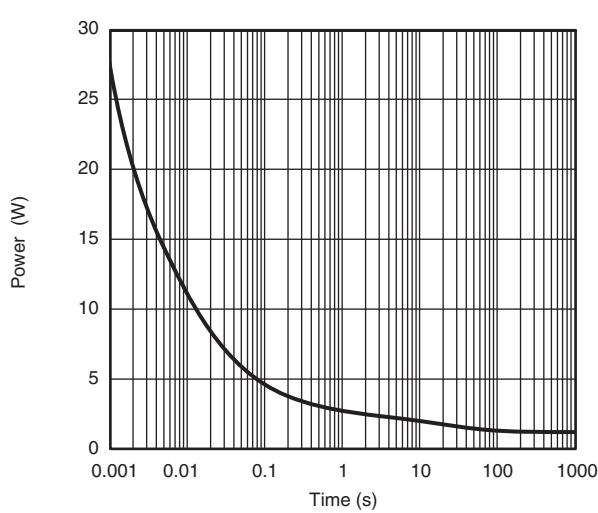
Source-Drain Diode Forward Voltage



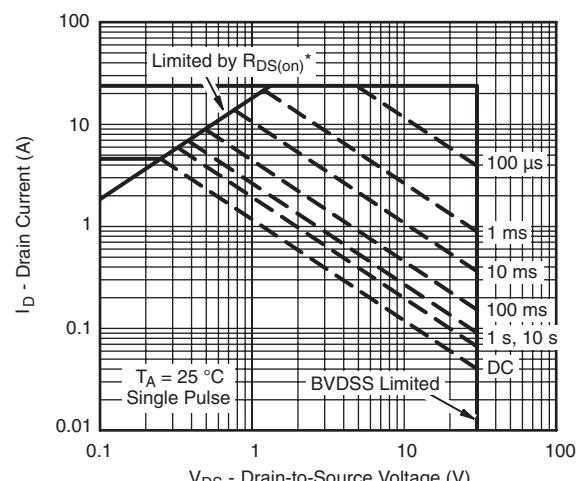
On-Resistance vs. Gate-to-Source Voltage



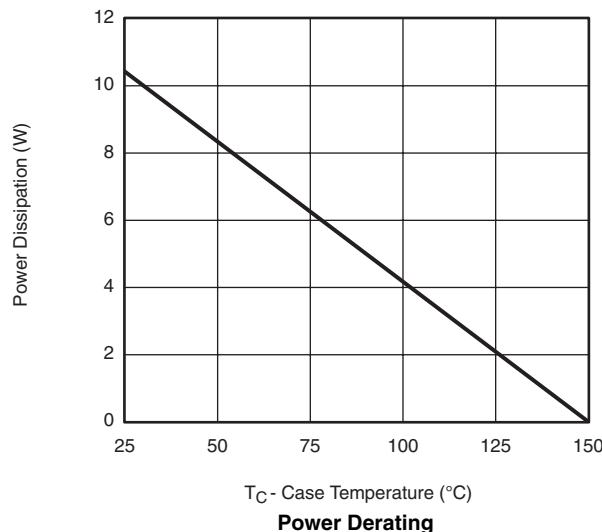
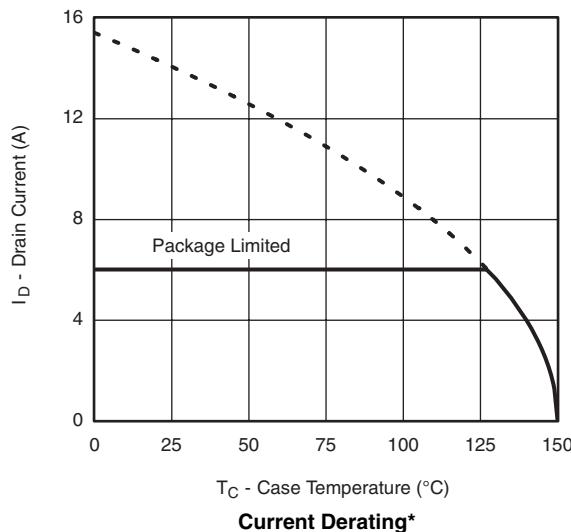
Threshold Voltage



Single Pulse Power (Junction-to-Ambient)



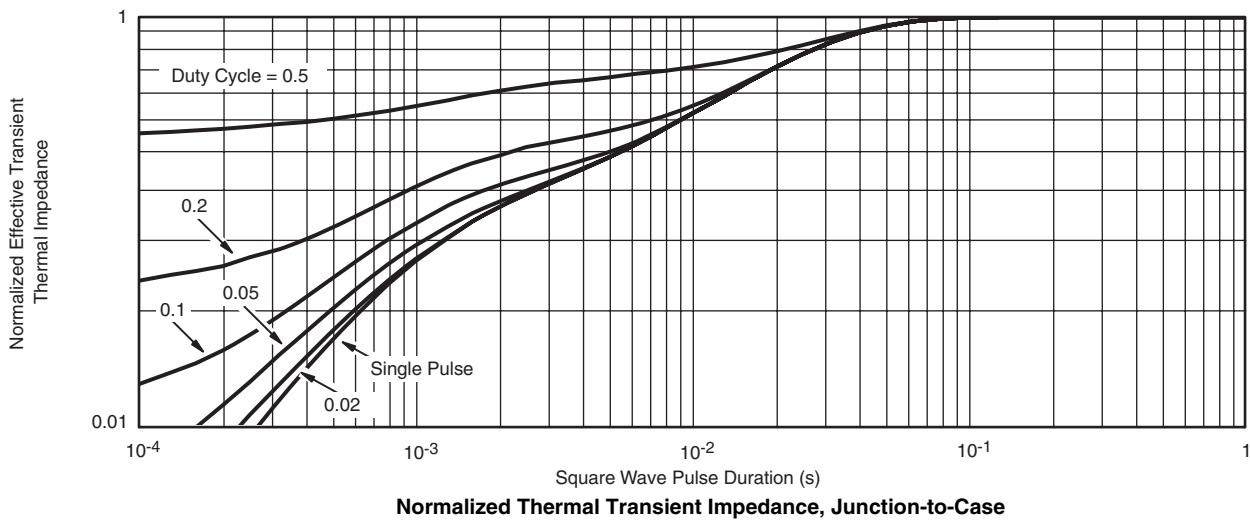
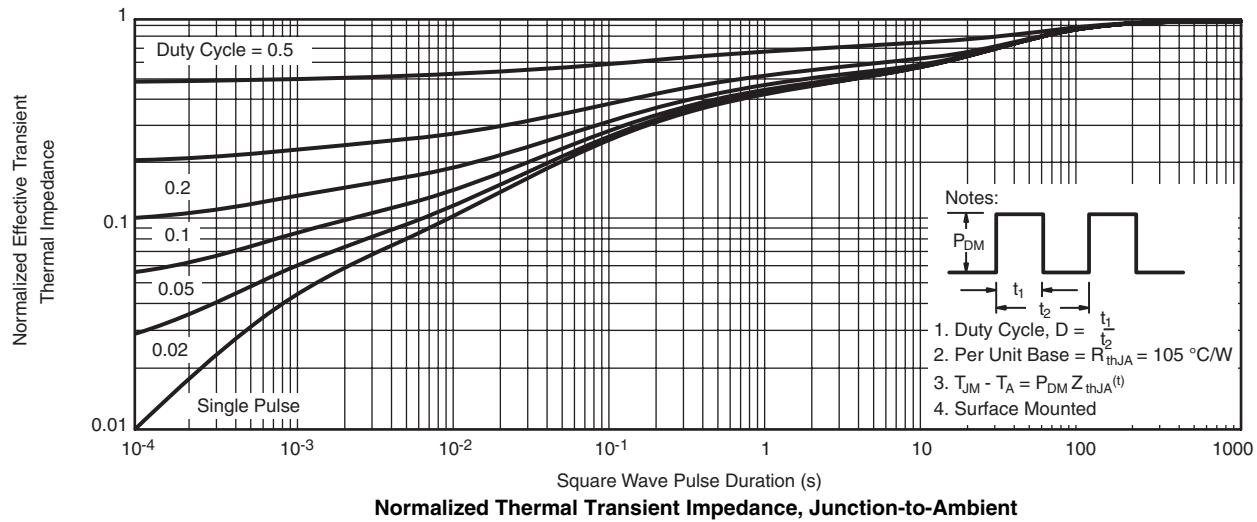
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

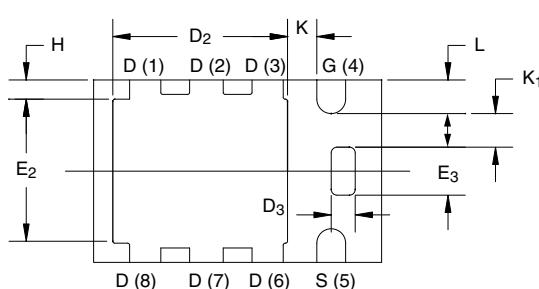
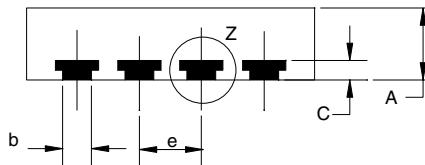
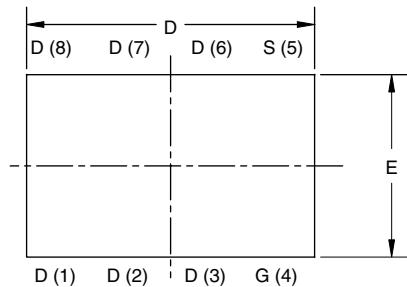
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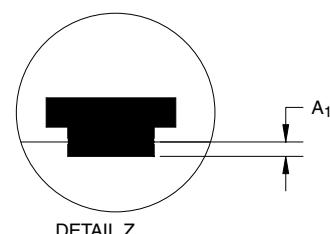
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65168.

PowerPAK® ChipFET® SINGLE PAD

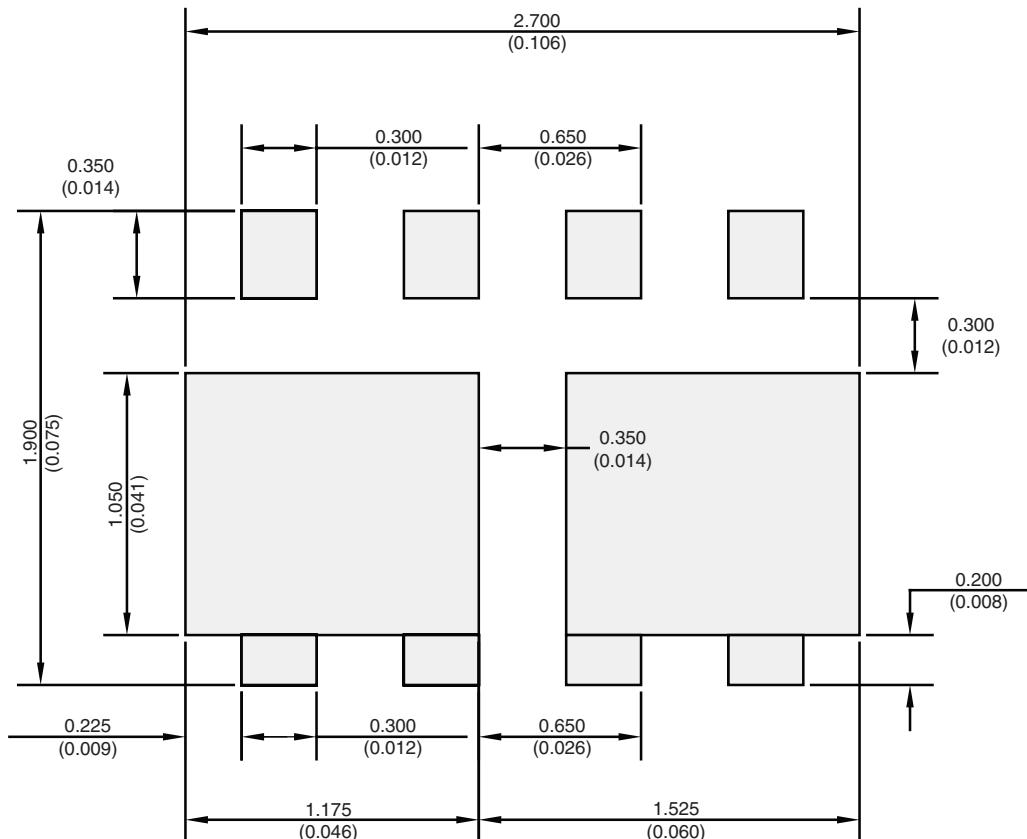


Backside view of single pad



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.75	1.87	2.00	0.069	0.074	0.079
D ₃	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	1.38	1.50	1.63	0.054	0.059	0.064
E ₃	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K ₁	0.30	-	-	0.012	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image
Pin #1 Location is Top Left Corner

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