

# TMC1175A

## Video A/D Converter

### 8 bit, 50 Msps

#### Features

- 8-Bit resolution
- 50 Msps conversion rate
- Low power: 100mW at 20 Msps
- Integral track/hold
- Integral and differential linearity error 0.5 LSB
- Single or dual +5 Volt supplies
- Differential phase 0.5 degree
- Differential gain 1.5%
- Three-state TTL/CMOS-compatible outputs
- Low cost

#### Applications

- Video digitizing
- VGA and CCD digitizing
- LCD projection panels
- Image scanners
- Personal computer video boards
- Multimedia systems
- Low cost, high speed data conversion

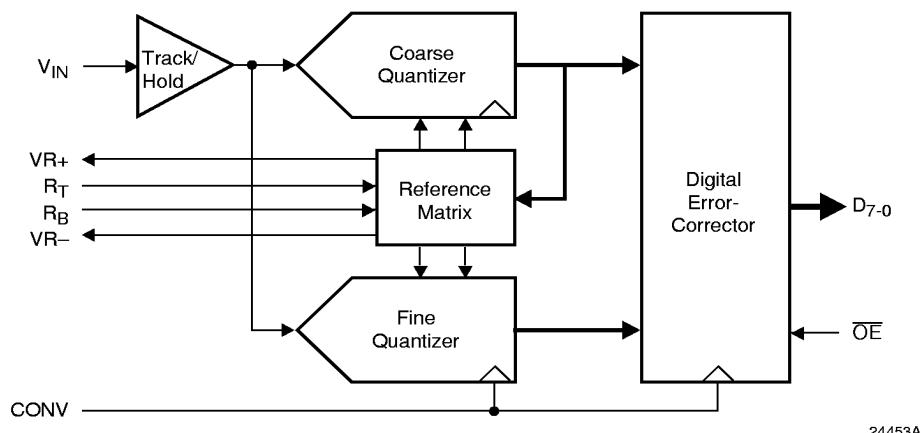
#### Description

The TMC1175A analog-to-digital (A/D) converter employs a two-step flash architecture to convert analog signals into 8-bit digital words at sample rates of up to 50 Msps (Megaspaces per second). An integral Track/Hold circuit delivers excellent performance on signals with full-scale frequency components up to 12 MHz. Innovative architecture and submicron CMOS technology limit typical power dissipation to 100 mW.

Power may be derived from either single or dual +5V supplies. Internal voltage reference resistors allow self-bias operation. Input capacitance is very low, simplifying or eliminating input driving amplifiers. All digital three-state outputs are TTL- and CMOS-compatible.

The TMC1175A is available in 24-pin plastic DIP, 24-lead plastic SOIC, and 28-lead J-lead PLCC packages. Performance specifications are guaranteed from -20°C to 75°C.

#### Block Diagram



24453A

Rev. 1.3.0

## Functional Description

The TMC1175A 8-bit A/D converter uses a two-step architecture to perform analog-to-digital conversion at rates up to 50 Msps. The input signal is held in an integral track/hold stage during the conversion process. Operation is pipelined, with one input sample taken and one output word provided for each CONVert cycle.

The first step in the conversion process is a coarse 4-bit quantization. This determines the range of the subsequent fine 4-bit quantization step. To eliminate spurious codes, the fine 4-bit A/D quantizer output is gray-coded and converted to binary before it is combined with the coarse result to form a complete 8-bit result.

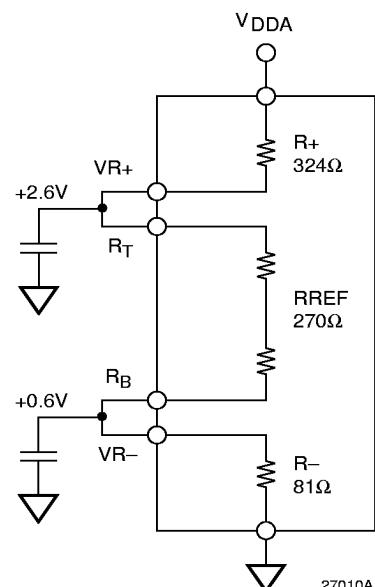
## Analog Input and Voltage References

The TMC1175A converts analog signals in the range **RB** to **RT** into digital data. Input signals outside that range produce “saturated” 00h or FFh output codes. The device will not be damaged by signals within the range **AGND** to **VDDA**.

The A/D converter input range is very flexible and extends from the +5 Volt power supply to ground. The nominal input range is 2 Volts, from 0.6V to 2.6V. The circuit is characterized and performance is specified over that range. However, the part will work well with a full-scale range from 1.0V to 5.0V. A reduced input range may simplify analog signal conditioning circuitry, at the expense of additional noise sensitivity and some reduced differential linearity performance. Similarly, increasing the range can improve differential linearity, but puts a greater burden on the input signal conditioning circuitry.

In many applications, external voltage reference sources are connected to the RT and RB pins. RB can be grounded. Gain and offset errors are directly related to the accuracy and stability of the applied reference voltages.

Two reference pull-up and pull-down resistors connected to VR+ and VR- are provided internally for operation without external voltage reference circuitry (Figure 1). The reference voltages applied to RT and RB may be generated by connecting VR+ to RT and VR- to RB. The power supply voltage is divided by the on-chip resistors to bias the RT and RB points. This sets-up the converter for operation in its nominal range from 0.6V to 2.6V.



**Figure 1. Reference Resistors**

With  $VDDA$  at 5.0V, connecting  $VR+$  to  $RT$  and grounding  $RB$  will provide an input range from 0.0V to 2.27V, while connecting  $RT$  to  $VDDA$  and  $RB$  to  $VR-$  produces a full scale range of 3.85V referenced to  $VDDA$ . External resistors may also be employed to provide arbitrary reference voltages, but they will not match the temperature coefficient of the on-chip resistors as well as  $R+$  and  $R-$ , and will cause the converter transfer function to vary with temperature.

With this implementation, errors in the power supply voltage end up on the conversion data output.

Because a two-step conversion process is employed, it is important that the references remain stable during the ENTIRE conversion process (two clock cycles). The reference voltage can then be changed, but any conversion in progress during a reference change is invalid.

**Table 1. Output Coding**

| Input Voltage   | Output |
|-----------------|--------|
| $R_T + 1$ LSB   | FF     |
| $R_T$           | FF     |
| $R_T - 1$ LSB   | FE     |
| ...             | ...    |
| $R_B + 128$ LSB | 80     |
| $R_B + 127$ LSB | 7F     |
| ...             | ...    |
| $R_B + 1$ LSB   | 01     |
| $R_B$           | 00     |
| $R_B - 1$ LSB   | 00     |

**Note:**

$$1. \text{ LSB} = (R_T - R_B) / 255$$

**Digital Inputs and Outputs**

Sampling of the applied input signal takes place on the **falling** edge of the CONV signal (Figure 2). The output word is delayed by 2 1/2 CONV cycles. It is then available after the **rising** edge of CONV. The previous data on the output

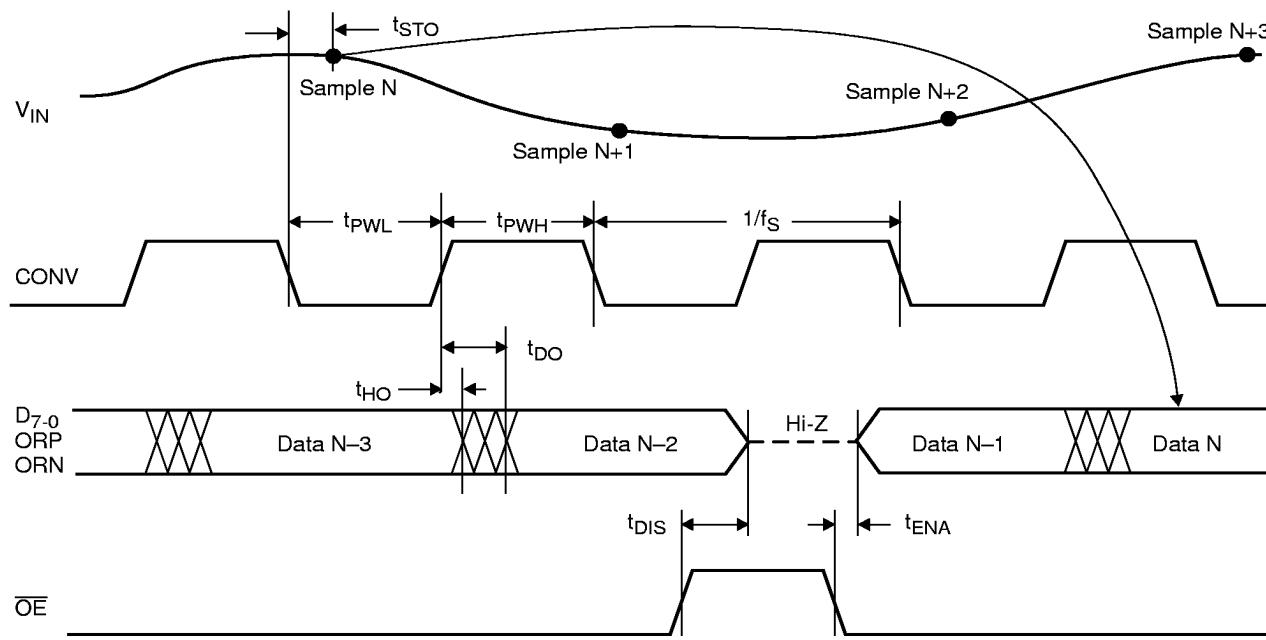
remain valid for  $t_{HO}$  (Output Hold Time), satisfying any hold time requirement of the receiving circuit. The new data become valid  $t_{DO}$  (Output Delay Time) after this rising edge of CONV.

The outputs of the TMC1175A are CMOS- and TTL-compatible, and are capable of driving four low-power Schottky TTL (54/74LS) loads. An Output Enable control,  $\overline{OE}$ , places the outputs in a high-impedance state when HIGH. The outputs are enabled when  $\overline{OE}$  is LOW.

**Power and Ground**

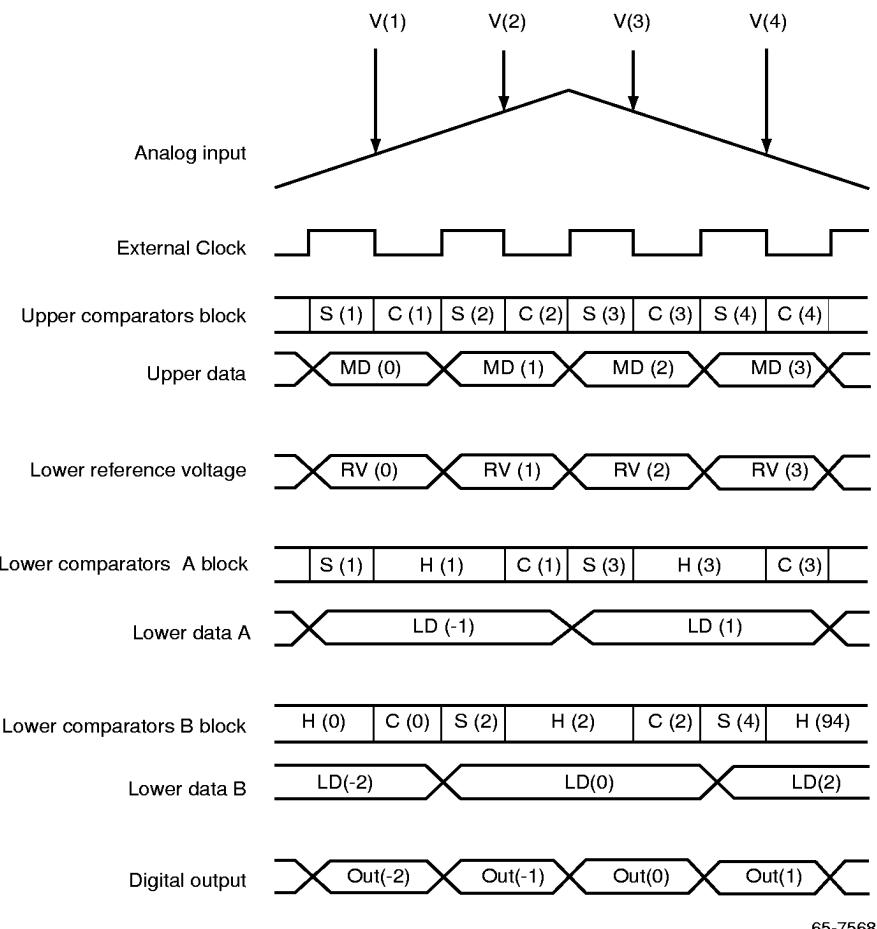
To minimize noise injection into the analog section,  $V_{DDA}$  may be connected to a separate regulated +5 volt supply.  $V_{DDD}$  may be connected to a digital supply. Power up sequence is immaterial. Latch-up will not occur.

AGND and DGND pins should be connected to a common ground plane. For optimum performance treat analog and digital PWB traces as transmission lines. Route analog connections cleanly to the TMC1175A. Segregate digital connections and if necessary terminate clocks to eliminate ringing. Prevent digital return currents from flowing across analog input sections of the TMC1175A.



24455A

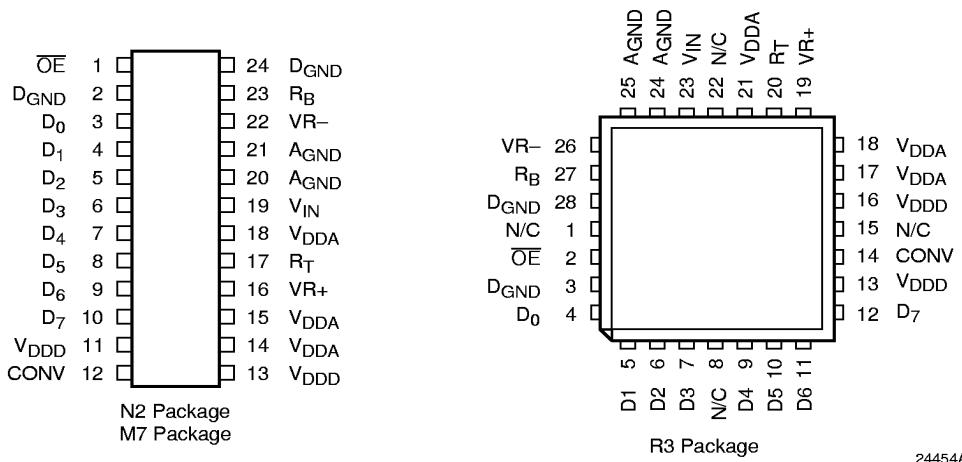
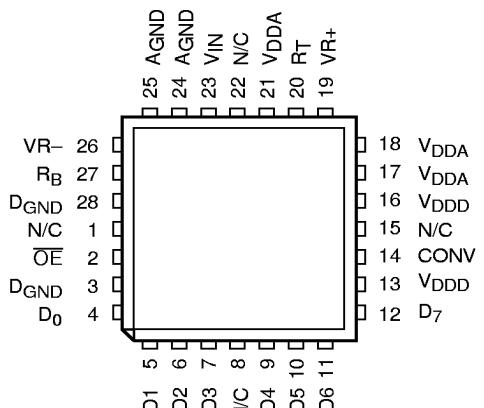
**Figure 2. Conversion Timing**



65-7568

Figure 3. Internal Timing

## Pin Assignments

N2 Package  
M7 Package

R3 Package

24454A

## Pin Descriptions

| Pin Name          | Pin Number |                 | Pin Type     | Pin Function Description   |
|-------------------|------------|-----------------|--------------|--|
|                   | N2, M7     | R3              |              |  |
| <b>Inputs</b>     |            |                 |              |  |
| VIN               | 19         | 23              | RT – RB      | <b>Analog Input.</b> The input voltage conversion range lies between the voltages applied to the RT and RB pins.   |
| RT                | 17         | 20              | 2.6V         | <b>Reference Voltage Top Input.</b> RT is the top input to the reference resistor ladder. A DC voltage applied to RT defines the positive end of the VIN conversion range.       |
| RB                | 23         | 27              | 0.6V         | <b>Reference Voltage Bottom Input.</b> RB is the bottom input to the reference resistor ladder. A DC voltage applied to RB defines the negative end of the VIN conversion range. |
| VR+               | 16         | 19              |              | <b>Reference Voltage Top Source.</b> VR+ is the internal pull-up reference resistor for self-bias operations.  |
| VR-               | 22         | 26              |              | <b>Reference Voltage Bottom Source.</b> VR- is the internal pull-down reference resistor for self-bias operations.   |
| OE                | 1          | 2               | CMOS         | <b>Output Enable.</b> (CMOS-compatible) When LOW, D7-0 are enabled. When HIGH, D7-0 are in a high-impedance state.   |
| CONV              | 12         | 14              | CMOS         | <b>Convert (Clock) Input.</b> (CMOS-compatible) VIN is sampled on the falling edge of CONV.  |
| <b>Outputs</b>    |            |                 |              |  |
| D7-0              | 10–3       | 12–9,<br>7–4    | CMOS/<br>TTL | <b>Data Outputs (D7 = MSB).</b> Eight-bit CMOS- and TTL-compatible digital outputs. Data is output following the rising edge of CONV.  |
| <b>Power</b>      |            |                 |              |  |
| VDDA              | 14, 15, 18 | 17, 18,<br>21   | +5V          | <b>Analog Supply Voltage.</b> Independent +5 volt power connection to analog comparator circuits.  |
| VDDD              | 11, 13     | 13, 16          | +5V          | <b>Digital Supply Voltage.</b> Independent +5 volt power connection to digital error correction and output drivers.  |
| AGND              | 20, 21     | 24, 25          | 0.0V         | <b>Analog Ground.</b> Connect to the system analog ground plane.   |
| DGND              | 2, 24      | 3, 28           | 0.0V         | <b>Digital Ground.</b> Connect to the system analog ground plane.  |
| <b>No Connect</b> |            |                 |              |  |
| N/C               |            | 1, 8, 15,<br>22 | open         | Not Connected.   |

## Bandwidth Specification Notes

The specification for bandwidth of an A/D converter is somewhat different from the normal frequency-response specification used in amplifiers and filters. An understanding of the differences will help in selecting converters properly for particular applications.

A/D conversion comprises two distinct processes: *sampling* and *quantizing*. *Sampling* is “grabbing” a snapshot of the input signal and holding it steady for quantizing. The *quantizing* process is approximating the analog input, which may be any value within the conversion range, with its nearest numerical value. While sampling is a high-frequency process, quantizing operates on a dc signal, held steady by the track/hold circuit. Therefore, the sampling process is what relates to the dynamic characteristics of the converter.

Sampling involves an *aperture time*, the time during which the track/hold is trying to capture the input signal and settle on a dc value to hold. It is analogous to the shutter speed of a camera: the shorter the aperture (or faster the shutter) the less the signal will be blurred, and the less uncertainty there will be in the quantized value.

For example, a 10 MHz sinewave with a 1V peak amplitude (2Vp-p) has a maximum slew rate of  $2\pi fA$  at zero crossing, or  $62.8V/\mu s$ . With an 8-bit A/D converter,  $q$  (the quantization step size) =  $2V/255 = 7.8mV$ . The input signal will slew one LSB in 124ps. To limit the error (and noise) contribution due to *aperture effects* to 1/2LSB, the aperture must be shorter than 62ps.

This is the primary reason that the signal to noise ratio drops off as full scale frequency increases. Note, also, that the slew rate is directly proportional to signal amplitude,  $A$ . A/Ds will handle lower-amplitude signals of higher bandwidth.

All this is of particular interest in applications such as digitizing analog VGA RGB signals, or the output of a CCD imaging chip. These data are effectively pre-sampled: there is a period of rapid slewing from one pixel value to another, followed by a relatively stable dc level before the signal slews to the next pixel value. The goal is, of course, to

sample on these pixel values, not on the slewing between pixels. During the aperture time, the A/D sees essentially a dc signal, and classic bandwidth considerations are not important. As long as the input circuit can slew and settle to the new value in the prescribed period, an accurate conversion will be made.

The TMC1175A is capable of slewing a full 2V and settling between samples taken as little as 25ns apart, making it ideal for digitizing analog VGA and CCD outputs.

## Equivalent Circuits and Threshold Level

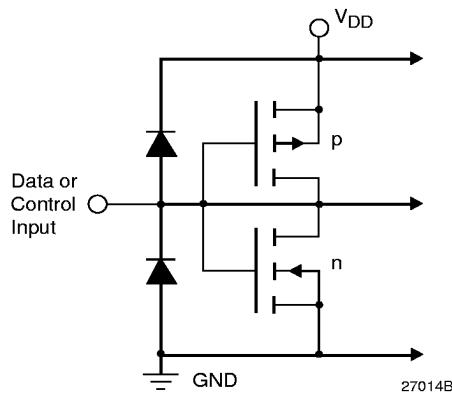


Figure 4. Equivalent Digital Input Circuit

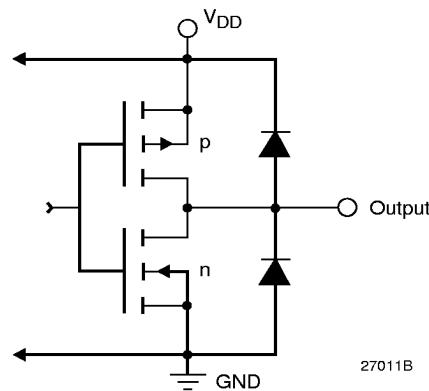


Figure 5. Equivalent Digital Output Circuit

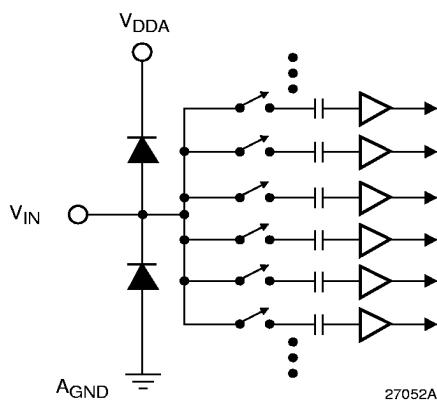


Figure 6. Equivalent Analog Input Circuit

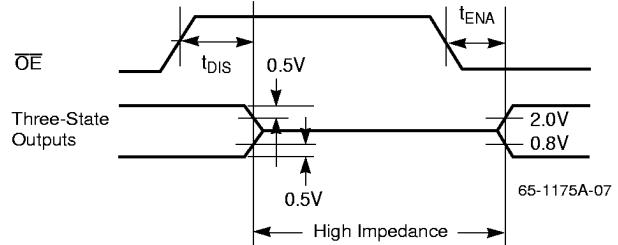


Figure 7. Threshold Levels for Three-State Measurements

**Absolute Maximum Ratings**(beyond which the device may be damaged)<sup>1</sup>

| Parameter                     | Conditions                            | Min   | Typ | Max        | Unit |
|-------------------------------|---------------------------------------|-------|-----|------------|------|
| <b>Power Supply Voltages</b>  |                                       |       |     |            |      |
| VDDA                          | Measured to AGND                      | -0.5  |     | 7.0        | V    |
| VDDD                          | Measured to DGND                      | -0.5  |     | 7.0        |      |
| VDDA                          | Measured to VDDD                      | -0.5  |     | 0.5        | V    |
| AGND                          | Measured to DGND                      | -0.5  |     | 0.5        |      |
| <b>Digital Inputs</b>         |                                       |       |     |            |      |
| Applied Voltage <sup>2</sup>  | Measured to DGND                      | -0.5  |     | VDDD + 0.5 | V    |
| Forced Current <sup>3,4</sup> |                                       | -10.0 |     | 10.0       | mA   |
| <b>Analog Inputs</b>          |                                       |       |     |            |      |
| Applied Voltage <sup>2</sup>  | Measured to AGND                      | -0.5  |     | VDDA + 0.5 | V    |
| Forced Current <sup>3,4</sup> |                                       | -10.0 |     | 10.0       | mA   |
| <b>Outputs</b>                |                                       |       |     |            |      |
| Applied Voltage <sup>2</sup>  | Measured to DGND                      | -0.5  |     | VDDD + 0.5 | V    |
| Forced Current <sup>3,4</sup> |                                       | -6.0  |     | 6.0        | mA   |
| Short Circuit Duration        | Single output in HIGH state to ground |       |     | 1          | sec  |
| <b>Temperature</b>            |                                       |       |     |            |      |
| Operating, Ambient            |                                       | -20   |     | 110        | °C   |
| Junction                      |                                       |       |     | 150        | °C   |
| Storage                       |                                       | -65   |     | 150        | °C   |
| Lead Soldering                | 10 seconds                            |       |     | 300        | °C   |
| Vapor Phase Soldering         | 1 minute                              |       |     | 220        | °C   |

**Notes:**

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if operating conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device

## Operating Conditions

| Parameter |                                  |             | Min        | Nom | Max        | Units |
|-----------|----------------------------------|-------------|------------|-----|------------|-------|
| VDDD      | Digital Power Supply Voltage     |             | 4.75       | 5.0 | 5.25       | V     |
| VDDA      | Analog Power Supply Voltage      |             | 4.75       | 5.0 | 5.25       | V     |
| AGND      | Analog Ground (Measured to DGND) |             | -0.1       | 0   | 0.1        | V     |
| fs        | Conversion Rate                  | TMC1175A-20 |            |     | 20         | Msps  |
|           |                                  | TMC1175A-30 |            |     | 30         | Msps  |
|           |                                  | TMC1175A-40 |            |     | 40         | Msps  |
|           |                                  | TMC1175A-50 |            |     | 50         | Msps  |
| tPWH      | CONV Pulsewidth, HIGH            | TMC1175A-20 | 15         |     |            | ns    |
|           |                                  | TMC1175A-30 | 13         |     |            | ns    |
|           |                                  | TMC1175A-40 | 12         |     |            | ns    |
|           |                                  | TMC1175A-50 | 9          |     |            | ns    |
| tPWL      | CONV Pulsewidth, LOW             | TMC1175A-20 | 15         |     |            | ns    |
|           |                                  | TMC1175A-30 | 12         |     |            | ns    |
|           |                                  | TMC1175A-40 | 12         |     |            | ns    |
|           |                                  | TMC1175A-50 | 9          |     |            | ns    |
| VRT       | Reference Voltage, Top           |             | 2.0        | 2.6 | VDDA       | V     |
| VRB       | Reference Voltage, Bottom        |             | 0          | 0.6 | 3.0        | V     |
| VRT-VRB   | Reference Voltage Differential   |             | 1.0        |     | 5.0        | V     |
| VIN       | Analog Input Range               |             | VRB        |     | VRT        | V     |
| VIH       | Input Voltage, Logic HIGH        |             | 0.7 x VDDD |     | VDDD       | V     |
| VIL       | Input Voltage, Logic LOW         |             | GND        |     | 0.3 x VDDD | V     |
| IOH       | Output Current, Logic HIGH       |             |            |     | -4.0       | mA    |
| IOL       | Output Current, Logic LOW        |             |            |     | 4.0        | mA    |
| TA        | Ambient Temperature, Still Air   |             | -20        |     | 75         | °C    |

## Electrical Characteristics

| Parameter |                                   | Conditions                      | Min | Typ <sup>1</sup> | Max | Units |
|-----------|-----------------------------------|---------------------------------|-----|------------------|-----|-------|
| IDD       | Power Supply Current <sup>1</sup> | VDDD = VDDA = Max, CLOAD = 35pF |     |                  |     |       |
|           |                                   | fS = 20Msps                     |     | 20               | 30  | mA    |
|           |                                   | fS = 30Msps                     |     | 25               | 35  | mA    |
|           |                                   | fS = 40Msps                     |     | 30               | 40  | mA    |
|           |                                   | fS = 50Msps                     |     | 35               | 48  | mA    |
| IDQ       | Power Supply Current, Quiescent   | VDDD = VDDA = Max               |     |                  |     |       |
|           |                                   | CONV = LOW                      |     | 7                | 18  | mA    |
|           |                                   | CONV = HIGH                     |     | 10               | 20  | mA    |

## Electrical Characteristics (continued)

| Parameter        | Conditions   | Min  | Typ <sup>1</sup>       | Max     | Units      |
|------------------|--|--|------------------------|---------|------------|
| PD               | V <sub>DDDD</sub> = V <sub>D<sup>DDA</sup></sub> = Max, C <sub>LOAD</sub> = 35pF |  |                        |         |            |
|                  | f <sub>S</sub> = 20Msps  |  | 100                    | 160     | mW         |
|                  | f <sub>S</sub> = 30Msps  |  | 125                    | 185     | mW         |
|                  | f <sub>S</sub> = 40Msps  |  | 150                    | 210     | mW         |
|                  | f <sub>S</sub> = 50Msps  |  | 185                    | 250     | mW         |
| C <sub>AI</sub>  | CONV = LOW   |  | 4                      |         | pF         |
|                  | CONV = HIGH  |  | 12                     |         | pF         |
| R <sub>IN</sub>  | Input Resistance   | 500  | 1000                   |         | k $\Omega$ |
| I <sub>CB</sub>  | Input Current, Analog  |  |                        | $\pm 1$ | $\mu$ A    |
| R <sub>REF</sub> | Reference Resistance   | 200  | 270                    | 340     | $\Omega$   |
| I <sub>IH</sub>  | Input Current, HIGH  | V <sub>DDDD</sub> = Max, V <sub>IN</sub> = V <sub>DDDD</sub> |                        | $\pm 5$ | $\mu$ A    |
| I <sub>IL</sub>  | Input Current, LOW   | V <sub>DDDD</sub> = Max, V <sub>IN</sub> = 0V                |                        | $\pm 5$ | $\mu$ A    |
| I <sub>OZH</sub> | Hi-Z Output Leakage  | V <sub>DDDD</sub> = Max, V <sub>IN</sub> = V <sub>DDDD</sub> |                        | $\pm 5$ | $\mu$ A    |
| I <sub>OZL</sub> | Hi-Z Output Leakage  | V <sub>DDDD</sub> = Max, V <sub>IN</sub> = 0V                |                        | $\pm 5$ | $\mu$ A    |
| I <sub>OS</sub>  | Short-Circuit Current  |  |                        | -30     | mA         |
| V <sub>OH</sub>  | Output Voltage, HIGH   | I <sub>OH</sub> = -100 $\mu$ A                               | V <sub>DDDD</sub> -0.3 |         | V          |
|                  |  | I <sub>OH</sub> = -2.5mA                                     | 3.5                    |         | V          |
|                  |  | I <sub>OH</sub> = Max  | 2.4                    |         | V          |
| V <sub>OL</sub>  | Output Voltage, LOW  | I <sub>OL</sub> = Max  |                        | 0.4     | V          |
| C <sub>DI</sub>  | Digital Input Capacitance  |  | 4                      | 10      | pF         |
| C <sub>DO</sub>  | Digital Output Capacitance   |  | 10                     |         | pF         |

**Note:**

1. Typical values with V<sub>DDDD</sub> = V<sub>D<sup>DDA</sup></sub> = Nom and T<sub>A</sub> = Nom, Minimum/Maximum values with V<sub>DDDD</sub> = V<sub>D<sup>DDA</sup></sub> = Max and T<sub>A</sub> = Min.

## Switching Characteristics

| Parameter        | Conditions           | Min                      | Typ | Max | Units |
|------------------|----------------------|--------------------------|-----|-----|-------|
| t <sub>STO</sub> | Sampling Time Offset | 2                        | 5   | 8   | ns    |
| t <sub>HO</sub>  | Output Hold Time     | C <sub>LOAD</sub> = 15pF | 5   |     | ns    |
| t <sub>DO</sub>  | Output Delay Time    | C <sub>LOAD</sub> = 15pF |     | 20  | ns    |
| t <sub>TEN</sub> | Output Enable Time   |                          |     | 27  | ns    |
| t <sub>DIS</sub> | Output Disable Time  |                          |     | 42  | ns    |

## System Performance Characteristics

| Parameter        | Conditions   | Min | Typ <sup>1</sup> | Max                  | Units                    |
|------------------|--|-----|------------------|----------------------|--------------------------|
| ELI              | Integral Linearity Error, Independent<br>VRT = 2.6V<br>VRB = 0.6V  |     | ±0.5             | ±1                   | LSB                      |
| ELD              | Differential Linearity Error<br>VRT = 2.6V<br>VRB = 0.6V   |     | ±0.3             | ±1                   | LSB                      |
| BW               | Bandwidth <sup>2</sup><br>TMC1175A-20<br>TMC1175A-30<br>TMC1175A-40<br>TMC1175A-50                             |     |                  | 10<br>12<br>12<br>12 | MHz<br>MHz<br>MHz<br>MHz |
| EAP              | Aperture Error   |     | 30               |                      | ps                       |
| EOT              | Offset Voltage, Top<br>RT – VIN for most positive code transition  | -8  | -25              | -42                  | mV                       |
| EOB              | Offset Voltage, Bottom<br>RB – VIN for most negative code transition   | 30  | 40               | 60                   | mV                       |
| dg               | Differential Gain<br>fS = 14.3Msps<br>NTSC 40 IRE Mod Ramp<br>VDDA = +5.0V, TA=25°C<br>VRT = 2.6V, VRB = 0.6V  |     | 1.5              | 2.7                  | %                        |
| dp               | Differential Phase<br>fS = 14.3Msps<br>NTSC 40 IRE Mod Ramp<br>VDDA = +5.0V, TA=25°C<br>VRT = 2.6V, VRB = 0.6V |     | 0.5              | 1.0                  | deg                      |
| SNR <sup>3</sup> | fS = 20Msps, VRT = 2.6V, VRB = 0.6V<br>fIN = 1.24MHz   | 44  | 48               |                      | dB                       |
|                  | fIN = 2.48MHz  | 43  | 47               |                      | dB                       |
|                  | fIN = 6.98MHz  | 41  | 45               |                      | dB                       |
|                  | fIN = 10.0MHz  | 37  | 42               |                      | dB                       |
|                  | fS = 30Msps, VRT = 2.6V, VRB = 0.6V<br>fIN = 1.24MHz   | 42  | 47               |                      | dB                       |
|                  | fIN = 2.48MHz  | 40  | 45               |                      | dB                       |
|                  | fIN = 6.98MHz  | 38  | 43               |                      | dB                       |
|                  | fIN = 10.0MHz  | 33  | 39               |                      | dB                       |
|                  | fIN = 12.0MHz  | 30  | 37               |                      | dB                       |
|                  | fS = 40Msps, VRT = 2.6V, VRB = 0.6V<br>fIN = 1.24MHz   | 40  | 45               |                      | dB                       |
|                  | fIN = 2.48MHz  | 38  | 43               |                      | dB                       |
|                  | fIN = 6.98MHz  | 36  | 41               |                      | dB                       |
|                  | fIN = 10.0MHz  | 34  | 38               |                      | dB                       |
|                  | fIN = 12.0MHz  | 32  | 36               |                      | dB                       |
|                  | fS = 50Msps, VRT = 2.6V, VRB = 0.6V<br>fIN = 10.0MHz   | 30  |                  |                      | dB                       |

## System Performance Characteristics (continued)

| Parameter         | Conditions   | Min | Typ <sup>1</sup> | Max | Units |
|-------------------|--|-----|------------------|-----|-------|
| SFDR <sup>4</sup> | f <sub>S</sub> = 20Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V<br>f <sub>IN</sub> = 1.24MHz | 46  | 52               |     | dB    |
|                   | f <sub>IN</sub> = 2.48MHz  | 44  | 51               |     | dB    |
|                   | f <sub>IN</sub> = 6.98MHz  | 41  | 45               |     | dB    |
|                   | f <sub>IN</sub> = 10.0MHz  | 38  | 43               |     | dB    |
|                   | f <sub>S</sub> = 30Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V<br>f <sub>IN</sub> = 1.24MHz | 42  | 49               |     | dB    |
|                   | f <sub>IN</sub> = 2.48MHz  | 40  | 45               |     | dB    |
|                   | f <sub>IN</sub> = 6.98MHz  | 37  | 41               |     | dB    |
|                   | f <sub>IN</sub> = 10.0MHz  | 35  | 40               |     | dB    |
|                   | f <sub>IN</sub> = 12.0MHz  | 34  | 39               |     | dB    |
|                   | f <sub>S</sub> = 40Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V<br>f <sub>IN</sub> = 1.24MHz | 40  | 44               |     | dB    |
|                   | f <sub>IN</sub> = 2.48MHz  | 39  | 43               |     | dB    |
|                   | f <sub>IN</sub> = 6.98MHz  | 38  | 41               |     | dB    |
|                   | f <sub>IN</sub> = 10.0MHz  | 36  | 40               |     | dB    |
|                   | f <sub>IN</sub> = 12.0MHz  | 36  | 39               |     | dB    |
|                   | f <sub>S</sub> = 50Msps, V <sub>RT</sub> = 2.6V, V <sub>RB</sub> = 0.6V<br>f <sub>IN</sub> = 10.0MHz | 33  |                  |     | dB    |

**Notes:**

1. Values shown in Typ column are typical for V<sub>DDD</sub> = V<sub>DDA</sub> = +5V and T<sub>A</sub> = 25°C.
2. Bandwidth is the frequency up to which a full-scale sinewave can be digitized without spurious codes.
3. SNR values do not include the harmonics of the fundamental frequency.
4. SFDR is the ratio in dB of fundamental amplitude to the harmonic with the highest amplitude.

## Typical Performance Characteristics

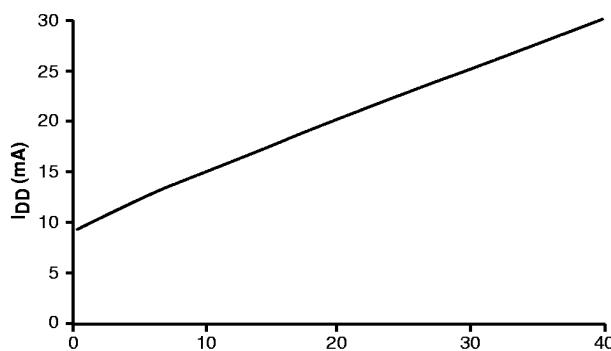


Figure 8. Typical IDD vs fs

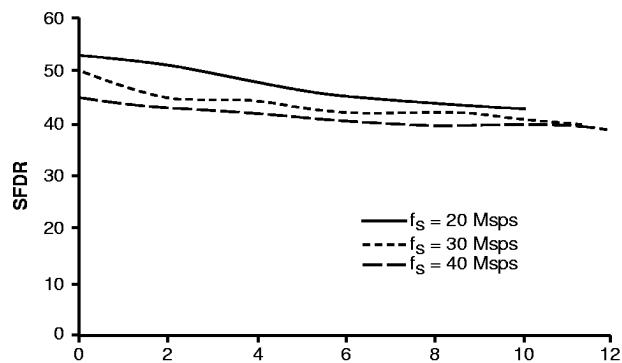


Figure 9. Typical SFDR vs fIN and fs

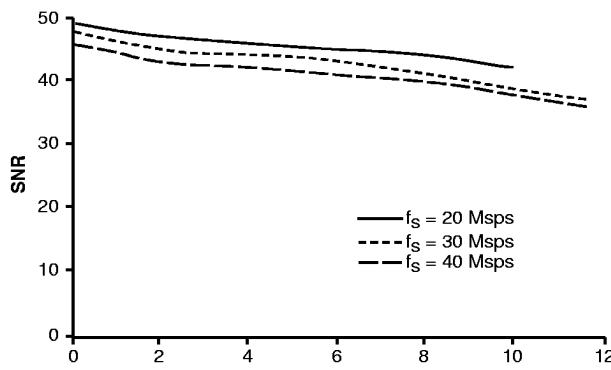


Figure 10. Typical SNR vs fIN and fs

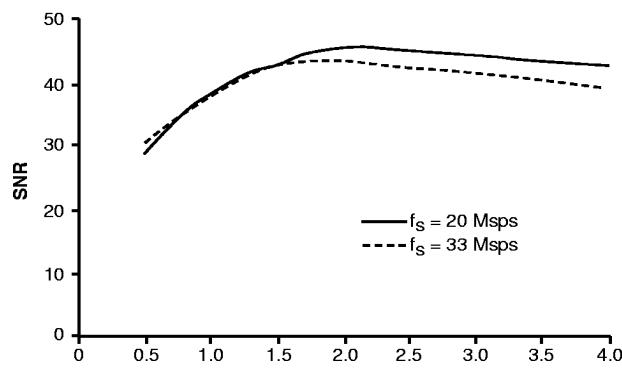


Figure 11. Typical SNR vs Full Scale Input Range

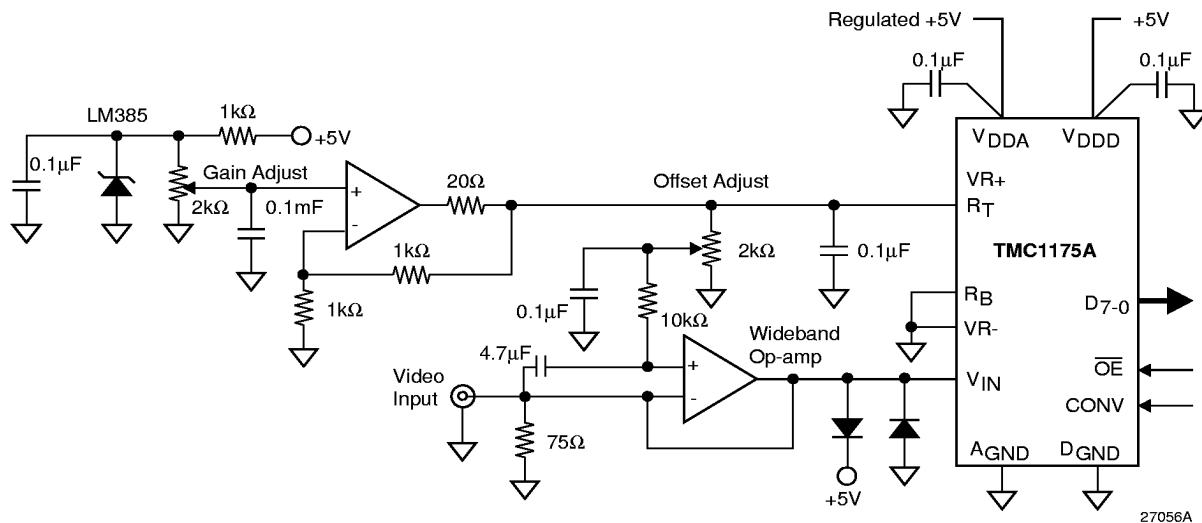
## Applications Discussion

The circuit in Figure 12 employs a band-gap reference to generate a variable RT reference voltage for the TMC1175A as well as a bias voltage to offset the wideband input amplifier to mid-range. An "offset adjust" is also shown for varying the mid-range voltage level. The operational amplifier in the reference circuitry is a standard 741-type.

The voltage reference at RT can be adjusted from 0.0 to 2.4 volts while RB is grounded. Diodes are used to restrict the wideband amplifier output to between -0.7V and VDD +0.7V. Diode protection is good practice to limit the analog input voltage at VIN to the safe operating range.

The circuit in Figure 13 shows self-bias of RT and RB by connection to VR+ and VR-. This sets up a 0.6 to 2.6 Volt input range for VIN. The input range is susceptible to power supply variation since the voltages on RT and RB are directly derived from VDDA. The video input is AC-coupled and biased at a adjustable midpoint of the A/D input range. This circuit offers the advantage of minimum support circuitry for the most cost-sensitive applications.

In Figure 14, an external band-gap reference sets RT to +1.2 Volts while RB is grounded. The internal pull-up resistor, R+, provides the bias current for the band-gap reference. The A/D converter input is biased to the mid-point of the input range.



**Figure 12. Typical Interface Circuit - High Performance**

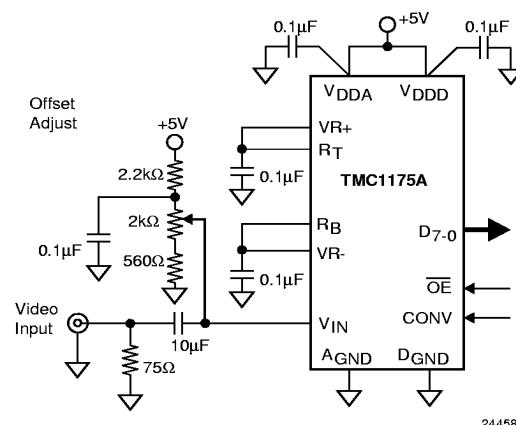
## Grounding

The TMC1175A has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (VDDD and VDDA) originate from separate sources with VDDA regulated, and that ground connections (DGND and AGND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin. The digital circuitry that gets its input from the TMC1175A should be referred to the system digital ground plane.

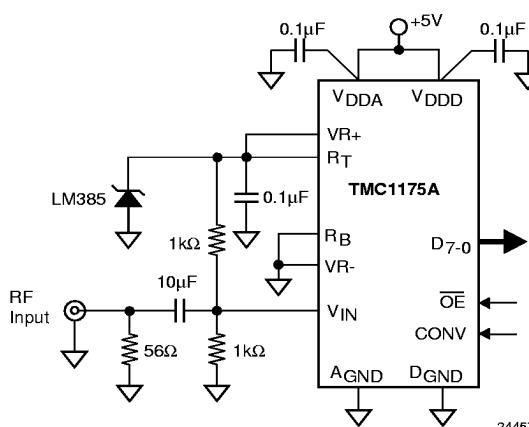
## Printed Circuit Board Layout

Designing with high performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option, even for breadboarding. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (VIN, RT, RB, VR+, VR-) as short as possible and as far as possible from all digital signals. The TMC1175A should be located near the board edge, close to the analog input connectors.
2. The power plane for the TMC1175A should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the VDD pins. If the power supply for the TMC1175A is the same as that of the system's digital circuitry, power to the TMC1175A should be decoupled with ferrite beads and 0.1 $\mu$ F capacitors to reduce noise.
3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.



**Figure 13. Typical Interface Circuit – Low Cost**



**Figure 14. Typical Interface Circuit – Stabilized Reference**

4. Decoupling capacitors should be applied liberally to VDD pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1 $\mu$ F ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.
5. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC1175A, the voltage reference, or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1175A and its related analog circuitry can have an adverse effect on performance.
6. CONV should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line at the CONV input, if required, to eliminate overshoot and ringing.

### Evaluation Board

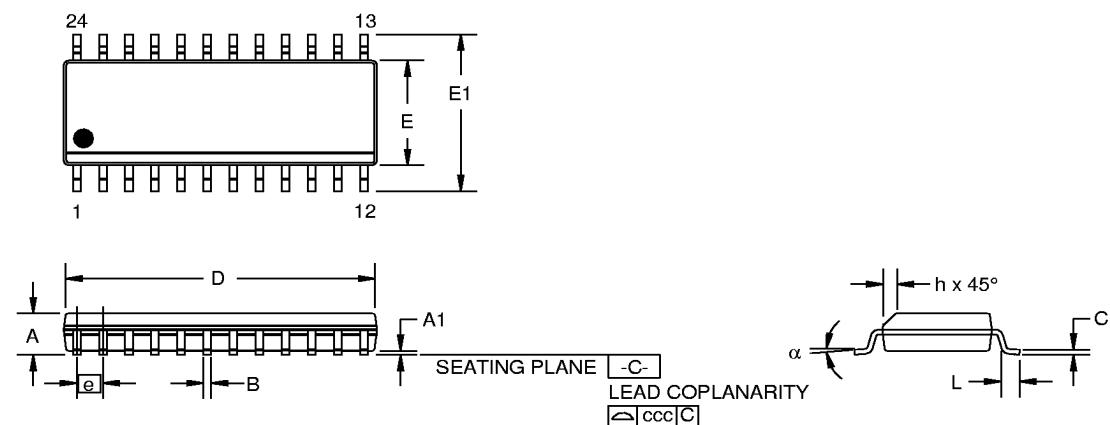
An evaluation board is available that implements good interface practices and provide a convenient testbed for developing system applications and circuit variations. An on-board D/A converter is provided to reconstruct the digitized signal and to evaluate converter performance.

Contact your sales representative for information.

## Mechanical Dimensions

### 24 Lead SOIC (5.4 mm) Package

| Symbol         | Inches   |      | Millimeters |       | Notes |
|----------------|----------|------|-------------|-------|-------|
|                | Min.     | Max. | Min.        | Max.  |       |
| A              | .067     | .075 | 1.70        | 1.90  |       |
| A1             | .004     | .012 | 0.10        | 0.31  |       |
| B              | .014     | .020 | 0.36        | 0.51  |       |
| C              | .006     | .012 | 0.15        | 0.30  |       |
| D              | .587     | .610 | 14.90       | 15.50 |       |
| E              | .205     | .220 | 5.20        | 5.60  |       |
| E1             | .295     | .319 | 7.50        | 8.10  |       |
| e              | .050 BSC |      | 1.27 BSC    |       |       |
| h              | .010     | .020 | 0.25        | 0.50  |       |
| L              | .016     | .050 | 0.41        | 1.27  |       |
| N              | 24       |      | 24          |       |       |
| $\alpha^\circ$ | 0        | 8    | 0           | 8     |       |
| ccc            | -        | .004 | -           | 0.10  |       |



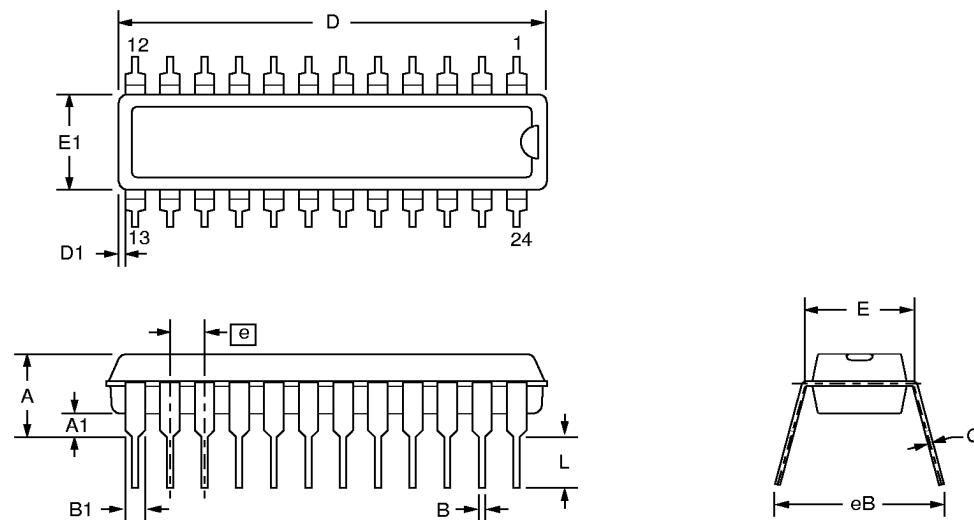
## Mechanical Dimensions (continued)

### 24 Lead Plastic DIP .300" Package

| Symbol | Inches   |       | Millimeters |       | Notes |
|--------|----------|-------|-------------|-------|-------|
|        | Min.     | Max.  | Min.        | Max.  |       |
| A      | —        | .210  | —           | 5.33  |       |
| A1     | .015     | —     | .38         | —     |       |
| A2     | .115     | .195  | 2.53        | 4.95  |       |
| B      | .014     | .022  | .36         | .56   |       |
| B1     | .045     | .070  | 1.14        | 1.78  |       |
| C      | .008     | .015  | .20         | .38   | 4     |
| D      | 1.125    | 1.275 | 28.58       | 32.39 | 2     |
| D1     | .005     | —     | .13         | —     |       |
| E      | .300     | .325  | 7.62        | 8.26  |       |
| E1     | .240     | .280  | 6.10        | 7.11  | 2     |
| e      | .100 BSC |       | 2.54 BSC    |       |       |
| eB     | —        | .430  | —           | 10.92 |       |
| L      | .115     | .160  | 2.92        | 4.06  |       |
| N      | 24       |       | 24          |       | 5     |

#### Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.

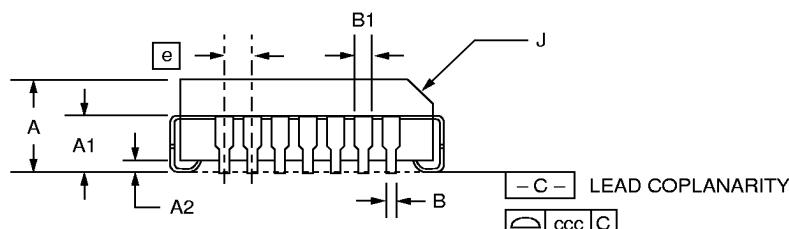
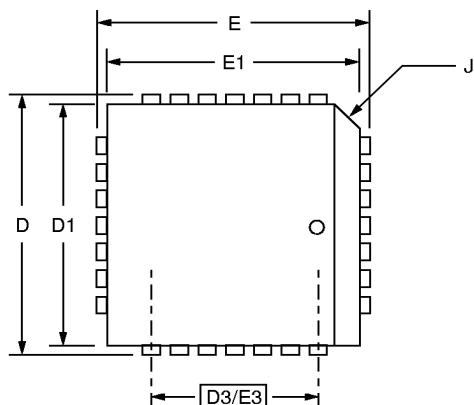


**Mechanical Dimensions** (continued)**28 Lead PLCC Package**

| Symbol | Inches   |      | Millimeters |       | Notes |
|--------|----------|------|-------------|-------|-------|
|        | Min.     | Max. | Min.        | Max.  |       |
| A      | .165     | .180 | 4.19        | 4.57  |       |
| A1     | .090     | .120 | 2.29        | 3.05  |       |
| A2     | .020     | —    | .51         | —     |       |
| B      | .013     | .021 | .33         | .53   |       |
| B1     | .026     | .032 | .66         | .81   |       |
| D/E    | .485     | .495 | 12.32       | 12.57 |       |
| D1/E1  | .450     | .456 | 11.43       | 11.58 | 3     |
| D3/E3  | .300 BSC |      | 7.62 BSC    |       |       |
| e      | .050 BSC |      | 1.27 BSC    |       |       |
| J      | .042     | .048 | 1.07        | 1.22  | 2     |
| ND/NE  | 7        |      | 7           |       |       |
| N      | 28       |      | 28          |       |       |
| ccc    | —        | .004 | —           | 0.10  |       |

**Notes:**

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



## Ordering Information

| Product Number | Conversion Rate | Temperature Range  | Screening  | Package      | Package Marking |
|----------------|-----------------|--------------------|------------|--------------|-----------------|
| TMC1175AM7C20  | 20 Msps         | TA = -20°C to 75°C | Commercial | 24-Lead SOIC | 1175AM7C20      |
| TMC1175AM7C30  | 30 Msps         | TA = -20°C to 75°C | Commercial | 24-Lead SOIC | 1175AM7C30      |
| TMC1175AM7C40  | 40 Msps         | TA = -20°C to 75°C | Commercial | 24-Lead SOIC | 1175AM7C40      |
| TMC1175AM7C50  | 50 Msps         | TA = -20°C to 75°C | Commercial | 24-Lead SOIC | 1175AM7C50      |
| TMC1175AN2C20  | 20 Msps         | TA = -20°C to 75°C | Commercial | 24-Lead PDIP | 1175AN2C20      |
| TMC1175AN2C30  | 30 Msps         | TA = -20°C to 75°C | Commercial | 24-Lead PDIP | 1175AN2C30      |
| TMC1175AN2C40  | 40 Msps         | TA = -20°C to 75°C | Commercial | 24-Lead PDIP | 1175AN2C40      |
| TMC1175AN2C50  | 50 Msps         | TA = -20°C to 75°C | Commercial | 24-Lead PDIP | 1175AN2C50      |
| TMC1175AR3C20  | 20 Msps         | TA = -20°C to 75°C | Commercial | 28-Lead PLCC | 1175AR3C20      |
| TMC1175AR3C30  | 30 Msps         | TA = -20°C to 75°C | Commercial | 28-Lead PLCC | 1175AR3C30      |
| TMC1175AR3C40  | 40 Msps         | TA = -20°C to 75°C | Commercial | 28-Lead PLCC | 1175AR3C40      |
| TMC1175AR3C50  | 50 Msps         | TA = -20°C to 75°C | Commercial | 28-Lead PLCC | 1175AR3C50      |

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.