TPS6102x 96% Efficient Synchronous Boost Converters

1 Features

- Qualified for Automotive Applications
- 96% Efficient Synchronous Boost Converter
- Output Voltage Remains Regulated When Input Voltage Exceeds Nominal Output Voltage
- Device Quiescent Current: 25 µA (Typ)
- Input Voltage Range: 0.9 V to 6.5 V
- Fixed and Adjustable Output Voltage Options Up to 5.5 V
- Power Save Mode for Improved Efficiency at Low Output Power
- Low Battery Comparator
- Low EMI-Converter (Integrated Anti-ringing Switch)
- Load Disconnect During Shutdown
- Over-Temperature Protection
- Small 3-mm × 3-mm QFN-10 Package

2 Applications

- All One-Cell, Two-Cell and Three-Cell Alkaline, NiCd or NiMH or Single-Cell Li Battery Powered Products
- Portable Audio Players
- PDAs
- Cellular Phones
- Personal Medical Products
- Camera White LED Flash Light

3 Description

The TPS6102x devices provide a power supply solution for products powered by either a one-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-polymer battery. Output currents can go as high as 200 mA while using a single-cell alkaline, and discharge it down to 0.9 V. It can also be used for generating 5 V at 500 mA from a 3.3-V rail or a Li-Ion battery. The boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency. At low load currents, the converter enters the *Power Save Mode* to maintain a high efficiency over a wide load current range. The *Power Save Mode* can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum peak current in the boost switch is limited to a value of 800 mA, 1500 mA or 1800 mA depending on the device version.

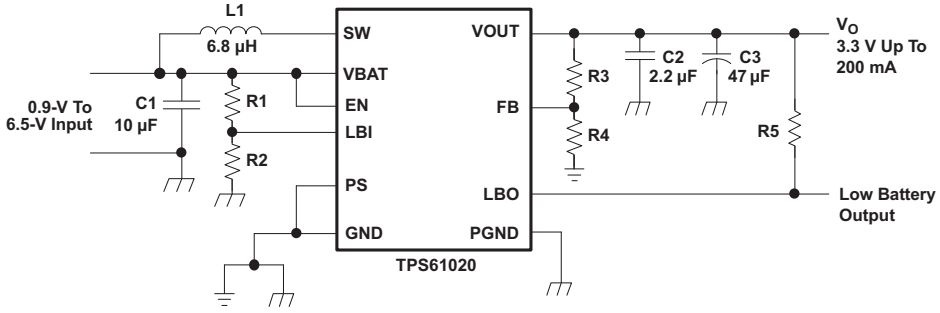
The TPS6102x devices keep the output voltage regulated even when the input voltage exceeds the nominal output voltage. The output voltage can be programmed by an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing and, in effect, lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode. The device is packaged in a 10-pin VSON PowerPAD™ package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61025-Q1	VSON (10)	3.00mm x 3.00mm
TPS61027-Q1		
TPS61029-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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5 Revision History

Changes from Original (November 2009) to Revision A **Page**

- Added Device Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ... 1
- Added ESD Ratings table ... 4
- Improved image quality for all equations and figures. ... 12

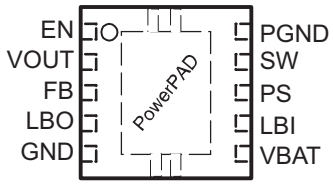
6 Device Comparison Table

PART NUMBER (1)	OUTPUT VOLTAGE (DC/DC)	NOMINAL SWITCH CURRENT LIMIT
TPS61029-Q1	Adjustable	1800 mA
TPS61025-Q1 (2)	3.3 V	1500 mA
TPS61027-Q1 (2)	5 V	1500 mA

(1) For all available packages, see the orderable addendum at the end of the datasheet
(2) Product preview. Contact TI factory for more information

7 Pin Configuration and Functions

VSON (DRC) (DPN)
10-Pin Package
TOP VIEW



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable input (1/VBAT enabled, 0/GND disabled)
FB	3	I	Voltage feedback of adjustable versions
GND	5		Control / logic ground
LBI	7	I	Low battery comparator input (comparator enabled with EN), may not be left floating, should be connected to GND or VBAT if comparator is not used
LBO	4	O	Low battery comparator output (open drain)
PS	8	I	Enable/disable power save mode (1/VBAT disabled, 0/GND enabled)
SW	9	I	Boost and rectifying switch input
PGND	10		Power ground
VBAT	6	I	Supply voltage
VOUT	2	O	Boost converter output
PowerPAD™			Must be soldered to achieve appropriate power dissipation. Should be connected to PGND.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage range	SW, VOUT, LBO, VBAT, PS, EN, FB, LBI	–0.3	7	V
T_J	Operating virtual junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

				VALUE	UNIT
TPS61025-Q1, TPS61027-Q1, and TPS61029-Q1 in **DRC** package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins except EN, GND, VBAT, and PGND	±500	
			Corner pins (EN, GND, VBAT, and PGND)	±750	
TPS61029-Q1 in **DPN** package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins except EN, GND, VBAT, and PGND	±500	
			Corner pins (EN, GND, VBAT, and PGND)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage at VBAT, V_I (TPS61025, TPS61027)	0.9	6.5	V
Supply voltage at VBAT, V_I (TPS61029)	0.9	5.5	V
Operating virtual junction temperature range, T_J	–40	125	°C

8.4 Thermal Information

THERMAL METRIC (1)		DRC	DPN	UNIT
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	47.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.5	58.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.6	22.4	
ψ_{JT}	Junction-to-top characterization parameter	1.7	0.9	
ψ_{JB}	Junction-to-board characterization parameter	21.8	22.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	4.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Over recommended junction temperature range with $T_A = T_J = –40°C$ to 125°C and over recommended input voltage range ,(typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_I	Minimum input voltage for start-up		R_L = 120 Ω		0.9	1.2	V
	Input voltage range, after start-up (TPS61025, TPS61027)			0.9		6.5	V
	Input voltage range, after start-up (TPS61029)			0.9		5.5	V
V_O	Output voltage range (TPS61029)			1.8		5.5	V
V_{FB}	Feedback voltage (TPS61025, TPS61027)			490	500	510	mV
f	Oscillator frequency			480	600	720	kHz
I_{SW}	Switch current limit (TPS61025, TPS61027)		VOUT = 3.3 V	1200	1500	1800	mA
I_{SW}	Switch current limit (TPS61029)		VOUT = 3.3 V	1500	1800	2100	mA
	Start-up current limit				0.4 x I_{SW}		mA
	SWN switch on resistance		VOUT = 3.3 V		260		mΩ
	SWP switch on resistance		VOUT = 3.3 V		290		mΩ
	Total accuracy (including line and load regulation)					±3%	
	Line regulation					0.6%	
	Load regulation					0.6%	
	Quiescent current	VBAT	I_O = 0 mA, V_{EN} = VBAT = 1.2 V, VOUT = 3.3 V, T_A = 25°C		1	3	µA
		VOUT			25	45	µA
	Shutdown current		V_{EN} = 0 V, VBAT = 1.2 V, T_A = 25°C		0.1	1	µA
CONTROL STAGE							
V_{UVLO}	Undervoltage lockout threshold		V_{LBI} voltage decreasing		0.8		V
V_{IL}	LBI voltage threshold		V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis				10		mV
	LBI input current		EN = VBAT or GND		0.01	0.1	µA
V_{OL}	LBO output low voltage		V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
V_{lkg}	LBO output leakage current		V_{LBO} = 7 V		0.01	0.1	µA
V_{IL}	EN, PS input low voltage					0.2 × VBAT	V
V_{IH}	EN, PS input high voltage			0.8 × VBAT			V
	EN, PS input current		Clamped on GND or VBAT		0.01	0.1	µA
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

9 Typical Characteristics

Table of Graphs

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Efficiency	vs Output current (TPS61025)	Figure 2
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	vs Input voltage (TPS61025)	Figure 4
	vs Input voltage (TPS61027)	Figure 5
Output voltage	vs Output current (TPS61025)	Figure 6
	vs Output current (TPS61027)	Figure 7
No load supply current into VBAT	vs Input voltage	Figure 8
No load supply current into VOUT	vs Input voltage	Figure 9

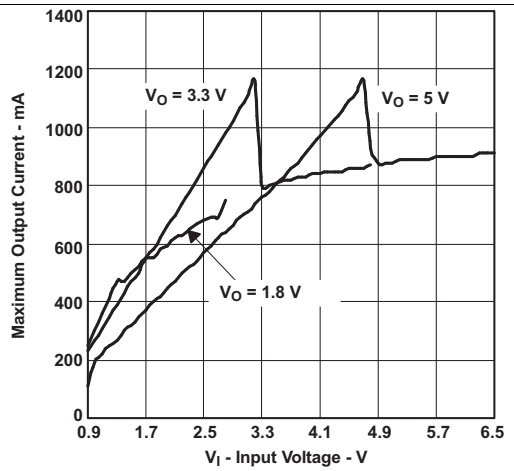


Figure 1. Maximum Output Current vs Input Voltage

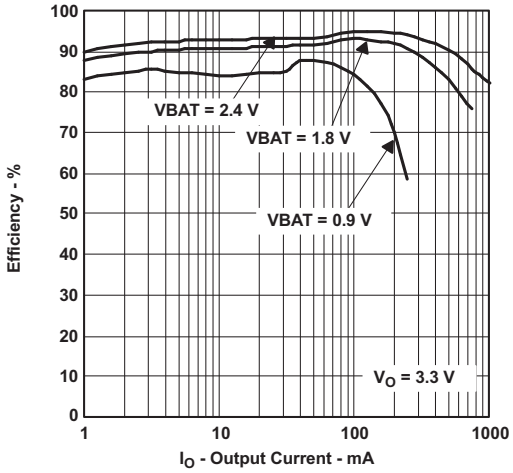


Figure 2. TPS61025 Efficiency vs Output Current

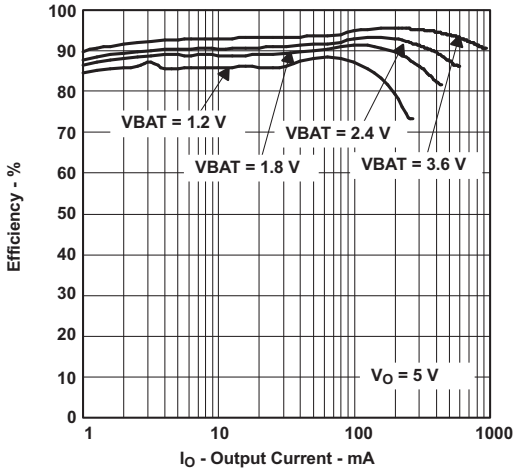


Figure 3. TPS61027 Efficiency vs Output Current

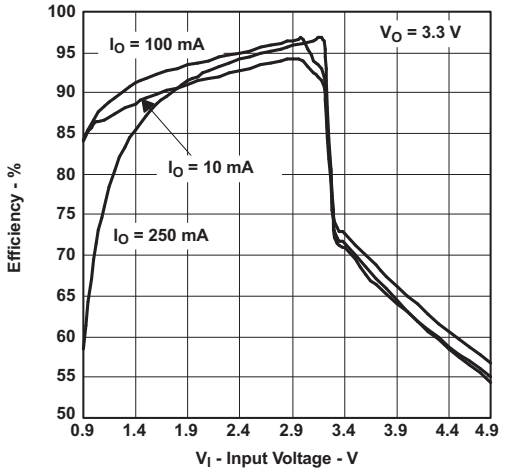


Figure 4. TPS61025 Efficiency vs Input Voltage

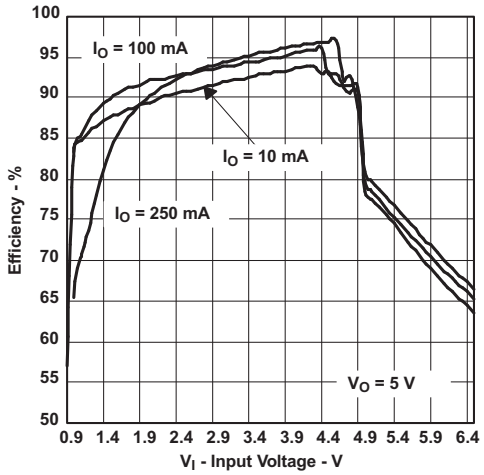


Figure 5. TPS61027 Efficiency vs Input Voltage

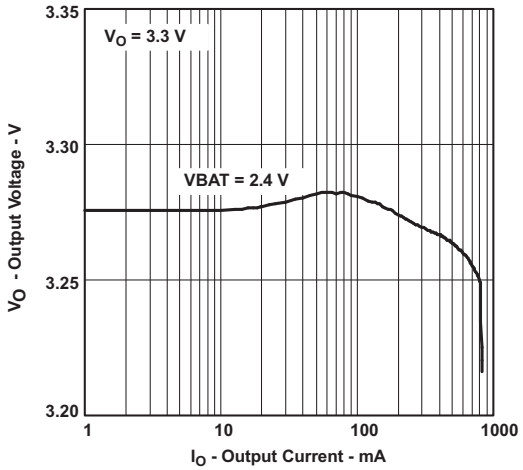


Figure 6. TPS61025 Output Voltage vs Output Current

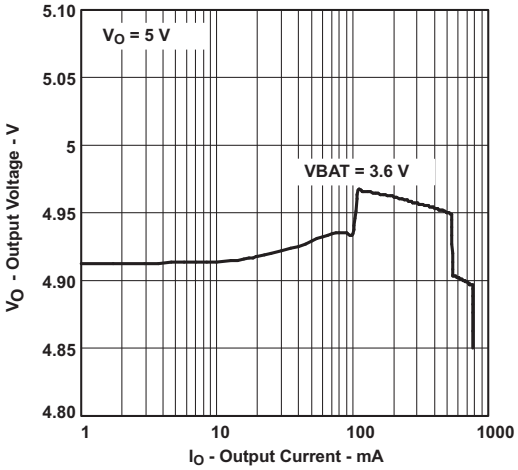


Figure 7. TPS61027 Output Voltage vs Output Current

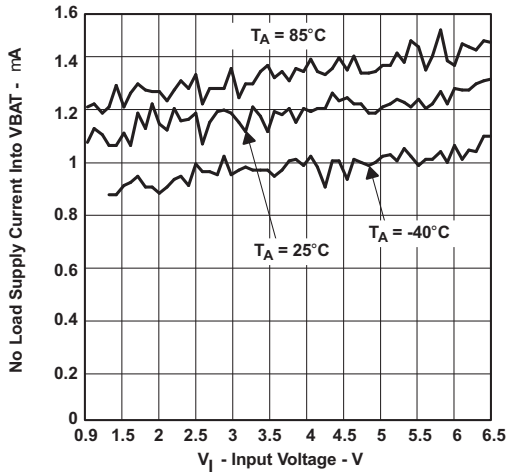


Figure 8. No Load Supply Current Into VBAT vs Input Voltage

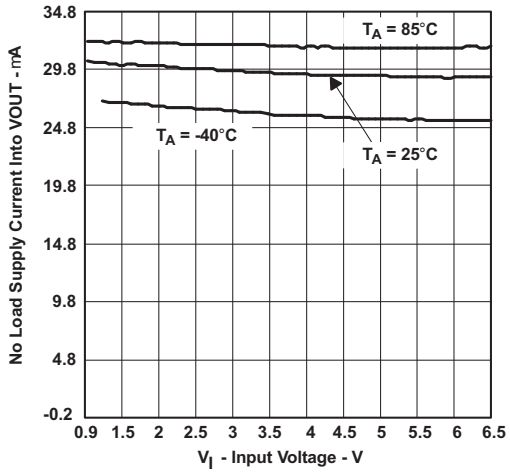
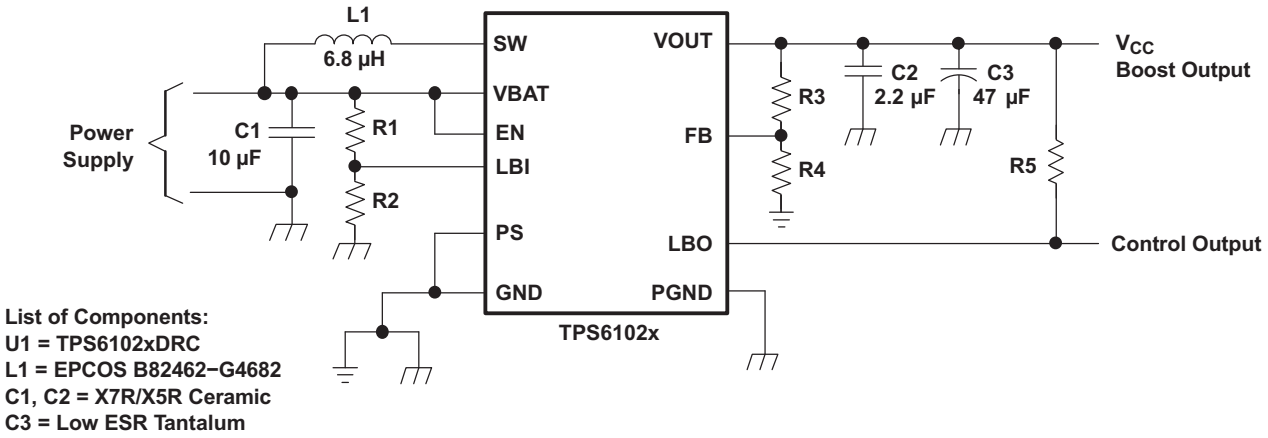


Figure 9. No Load Supply Current Into V_{OUT} vs Input Voltage

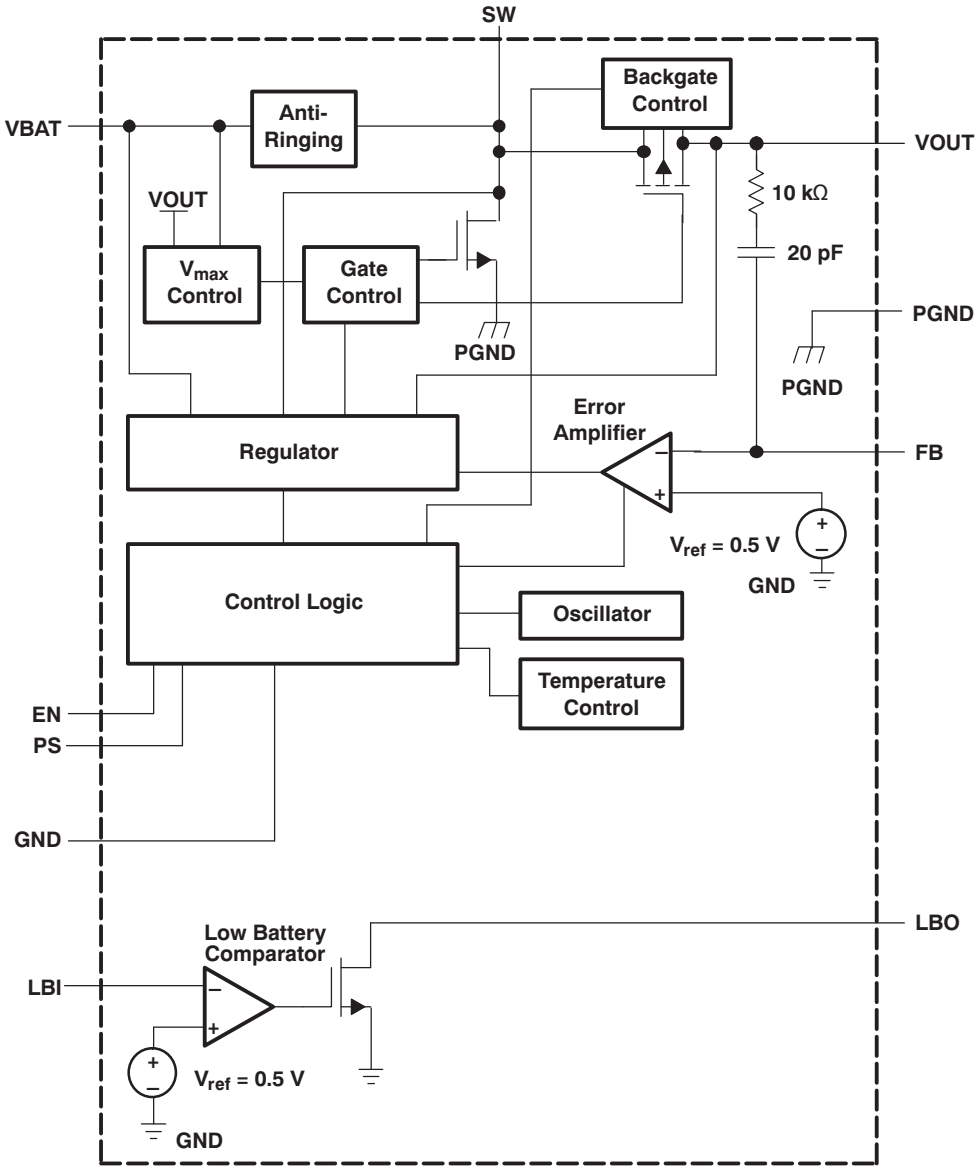
10 Parameter Measurement Information



11 Detailed Description

TPS6102x is based on a fixed frequency, pulse-width-modulation (PWM), controller using synchronous rectification to obtain maximum efficiency. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. At low load currents, the converter enters Power Save Mode to ensure high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency.

11.1 Functional Block Diagram (TPS61029)



11.2 Feature Description

11.2.1 Controller Circuit

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 1500 mA. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

11.2.1.1 Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

11.2.1.2 Down Regulation

In general, a boost converter only regulates output voltages which are higher than the input voltage. This device operates differently. For example, it is able to regulate 3.0 V at the output with two fresh alkaline cells at the input having a total cell voltage of 3.2 V. Another example is powering white LEDs with a forward voltage of 3.6 V from a fully charged Li-Ion cell with an output voltage of 4.2 V. To control these applications properly, a down conversion mode is implemented.

If the input voltage reaches or exceeds the output voltage, the converter changes to the conversion mode. In this mode, the control circuit changes the behavior of the rectifying PMOS. It sets the voltage drop across the PMOS as high as needed to regulate the output voltage. This means the power losses in the converter increase. This has to be taken into account for thermal consideration. The down conversion mode is automatically turned off as soon as the input voltage falls about 50 mV below the output voltage. For proper operation in down conversion mode the output voltage should not be programmed below 50% of the maximum input voltage which can be applied.

11.2.1.3 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

Feature Description (continued)

11.2.1.4 Softstart and Short Circuit Protection

When the device enables, the internal startup cycle starts with the first step, the precharge phase. During precharge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch is current limited during that phase. The current limit increases with the output voltage. This circuit also limits the output current under short circuit conditions at the output. Figure 10 shows the typical precharge current vs output voltage for specific input voltages:

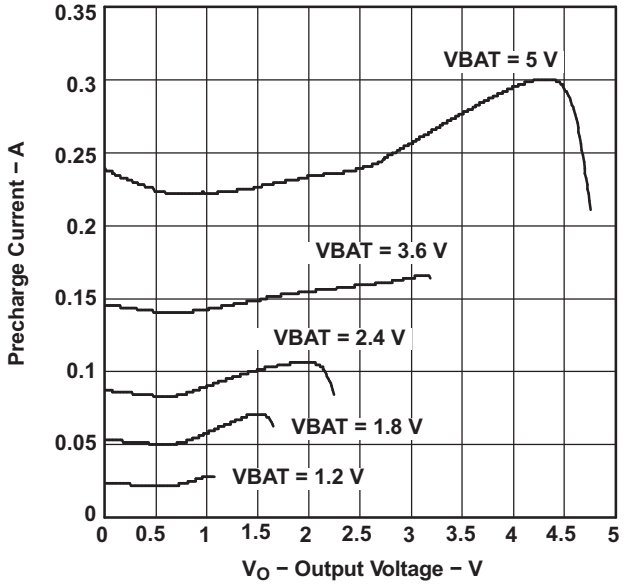


Figure 10. Precharge and Short Circuit Current

After charging the output capacitor to the input voltage, the device starts switching. If the input voltage is below 1.4 V the device works with a fixed duty cycle of 50% until the output voltage reaches 1.4 V. After that the duty cycle is set depending on the input output voltage ratio. Until the output voltage reaches its nominal value, the boost switch current limit is set to 40% of its nominal value to avoid high peak currents at the battery during startup. As soon as the output voltage is reached, the regulator takes control and the switch current limit is set back to 100%.

11.2.1.5 Low Battery Detector Circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

Feature Description (continued)

11.2.1.6 Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

11.3 Device Functional Modes

11.3.1 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 0.8 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 0.8 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

11.3.2 Power Save Mode

The PS pin can be used to select different operation modes. To enable power save, PS must be set low. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the PS to VBAT. In down conversion mode, power save mode is always active and the device cannot be forced into fixed frequency operation at light loads.

11.4 Programming

11.4.1 Programming the Output Voltage

The output voltage of the TPS61020 dc/dc converter can be adjusted with an external resistor divider. The typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across R4 is typically 500 mV. Based on those two values, the recommended value for R4 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using Equation 1:

$$R3 = R4 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1 \right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1.0-MΩ resistor should be chosen for R3. If for any reason the value for R4 is chosen significantly lower than 200 kΩ additional capacitance in parallel to R3 is recommended, in case the device shows instable regulation of the output voltage. The required capacitance value can be easily calculated using Equation 2:

$$C_{parR3} = 20\ pF \times \left(\frac{200\ k\Omega}{R4} - 1 \right) \quad (2)$$

Programming (continued)

11.4.2 Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 µA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2 is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage $V_{BAT,}$ can be calculated using Equation 3.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI-threshold}} - 1 \right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{500\ mV} - 1 \right) \quad (3)$$

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. If not used, the LBO pin can be left floating or tied to GND.

12 Application and Implementation

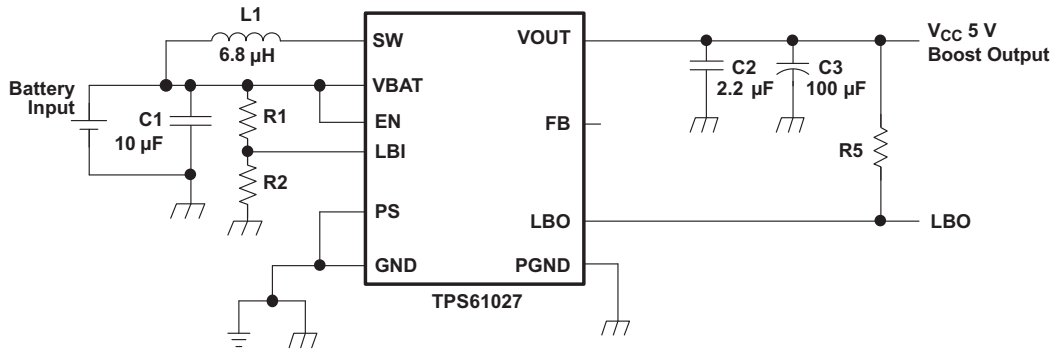
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

12.1 Application Information

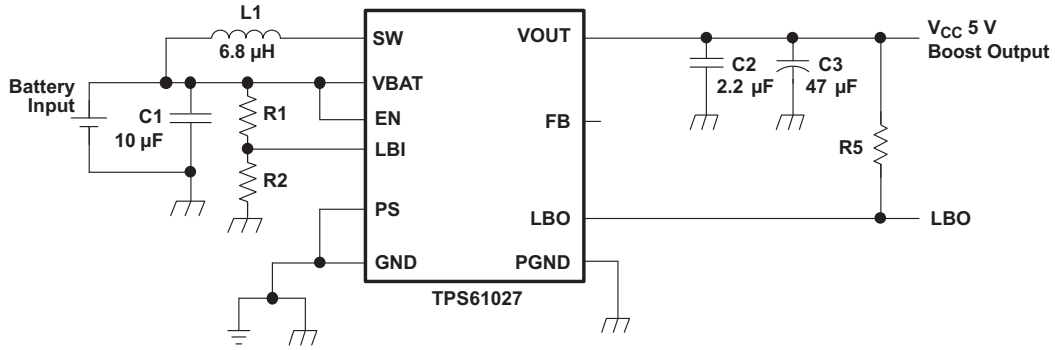
The devices are designed to operate from an input voltage supply range between 0.9 V (Vin rising UVLO is 1.2V) and 6.5 V with a maximum switching current limit up to 1.8A. The devices operate in PWM mode for medium to heavy load conditions and in power save mode at light load currents. In PWM mode the TPS6102x converter operates with the nominal switching frequency of 600kHz typically. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. The Power Save mode can be disabled when connecting PS pin to logic high, forcing the converter to operate at a fixed switching frequency.

12.1.1 Application Examples



List of Components:
U1 = TPS61027DRC
L1 = EPCOS B82462-G4682
C1, C2 = X7R,X5R Ceramic
C3 = Low ESR Tantalum

Figure 11. Power Supply Solution for Maximum Output Power Operating From a Single Alkaline Cell



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C1, C2 = X7R,X5R Ceramic
C3 = Low ESR Tantalum

Figure 12. Power Supply Solution for Maximum Output Power Operating From a Dual/Triple Alkaline Cell or Single Li-Ion Cell

Application Information (continued)

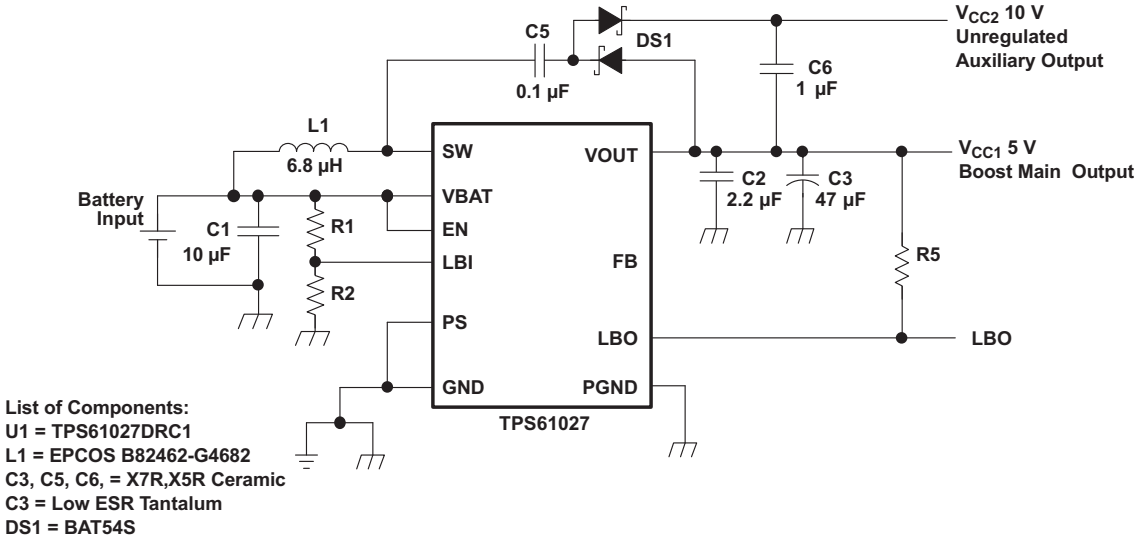


Figure 13. Power Supply Solution With Auxiliary Positive Output Voltage

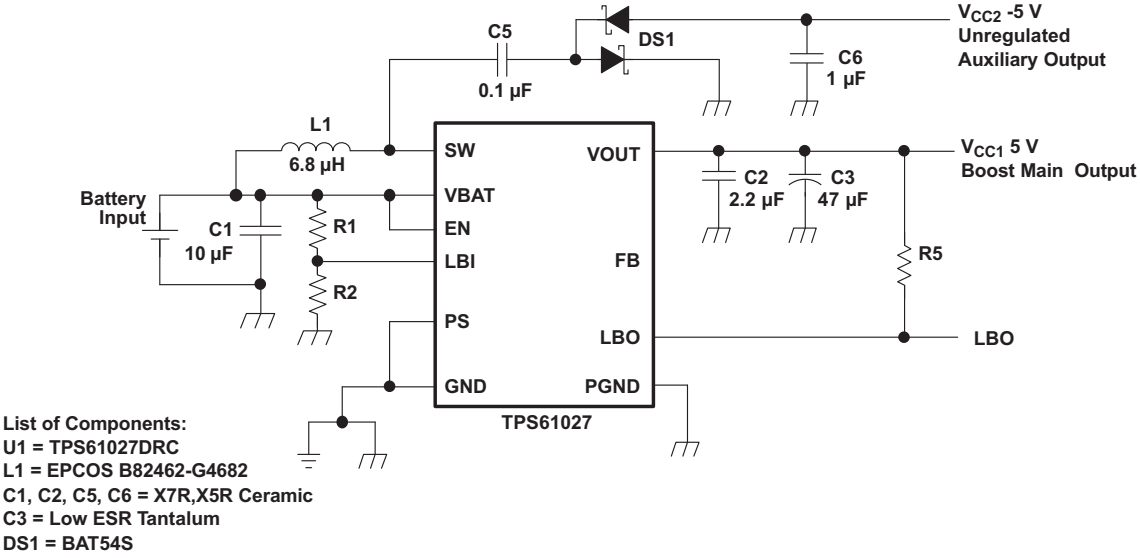


Figure 14. Power Supply Solution With Auxiliary Negative Output Voltage

12.2 Typical Application

TPS6102x with 1.2V-6.5 VIN, 800 mA Output Current

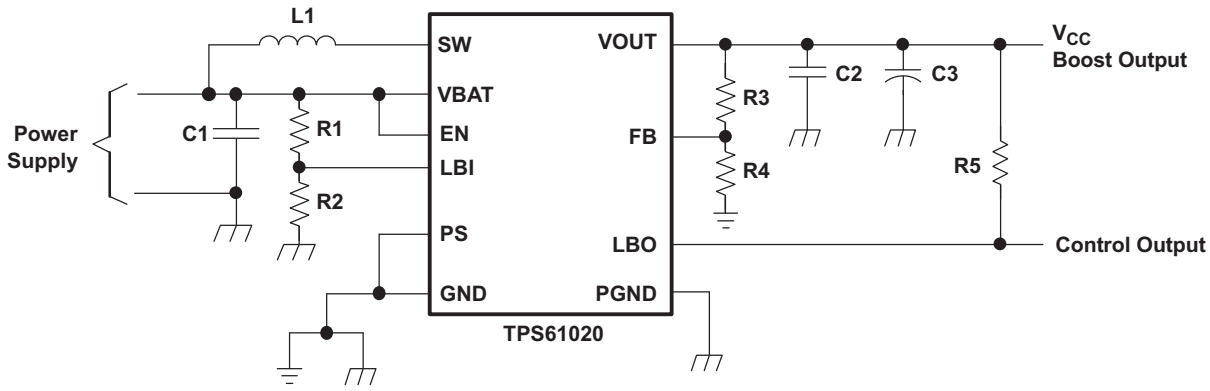


Figure 15. Typical Application Circuit for Adjustable Output Voltage Option

12.2.1 Design Requirements

The TPS6102x dc/dc converters are intended for systems powered by a single up to triple cell Alkaline, NiCd, NiMH battery with a typical terminal voltage between 0.9 V and 6.5 V. They can also be used in systems powered by one-cell Li-Ion or Li-Polymer with a typical voltage between 2.5 V and 4.2 V. Additionally, any other voltage source with a typical output voltage between 0.9 V and 6.5 V can power systems where the TPS6102x is used.

12.2.1.1 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6102xs switch is 1800 mA at an output voltage of 5 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 4:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (4)$$

For example, for an output current of 200 mA at 3.3 V, at least 920 mA of average current flows through the inductor at a minimum input voltage of 0.9 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using Equation 5:

$$L = \frac{V_{BAT} \times (V_{OUT} \pm V_{BAT})}{\Delta I_L \times f \times V_{OUT}} \quad (5)$$

Parameter *f* is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., 20% × I_L. In this example, the desired inductor has the value of 5.5 µH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. In typical applications a 6.8 µH inductance is recommended. The device has been optimized to operate with inductance values between 2.2 µH and 22 µH. Nevertheless operation with higher inductance values may be possible in some applications. Detailed stability analysis is then recommended. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in Equation 5. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been used with the TPS6102x converters:

Table 1. List of Inductors(1)

SUPPLIER	INDUCTOR SERIES
Sumida	CDRH4D28
	CDRH5D28
Wurth Elektronik	7447789
	744042
EPCOS	B82462-G4
Cooper Electronics Technologies	SD25
	SD20

(1) See *Third-Party Products Disclaimer*

12.2.1.2 Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

12.2.1.3 Output Capacitor

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 6:

$$C_{min} = \frac{I_{OUT} \times (V_{OUT} - V_{BAT})}{f \times \Delta v \times V_{OUT}} \quad (6)$$

Parameter *f* is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum capacitance of 24 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (7)$$

An additional ripple of 16 mV is the result of using a tantalum capacitor with a low ESR of 80 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 26 mV. Additional ripple is caused by load transients. This means that the output capacitor has to completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of 24 µF and load transient considerations the recommended output capacitance value is in a 47 to 100 µF range. For economical reasons, this is usually a tantalum capacitor. Therefore, the control loop has been optimized for using output capacitors with an ESR of above 30 mΩ. The minimum value for the output capacitor is 10 µF.

12.2.2 Detailed Design Procedure

12.2.2.1 Small Signal Stability

When using output capacitors with lower ESR, like ceramics, the adjustable voltage version is recommended. The missing ESR can be compensated in the feedback divider. Typically a capacitor in the range of 4.7 pF in parallel to R3 helps to obtain small signal stability with lowest ESR output capacitors. For more detailed analysis, the small signal transfer function of the error amplifier and the regulator, which is given in Equation 8, can be used:

$$A_{REG} = \frac{d}{V_{FB}} = \frac{4 \times (R3 + R4)}{R4 \times (1 + i \times \omega \times 0.9\ \mu s)} \quad (8)$$

12.2.2.2 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6102x devices is 125°C. The thermal resistance of the 10-pin QFN 3 × 3 package (DRC) is $R_{\Theta JA}$ = 47.2°C/W, if the PowerPAD is soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 847 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125°C - 85°C}{47.2°C / W} = 847 \text{ mW} \quad (9)$$

12.2.3 Application Curves

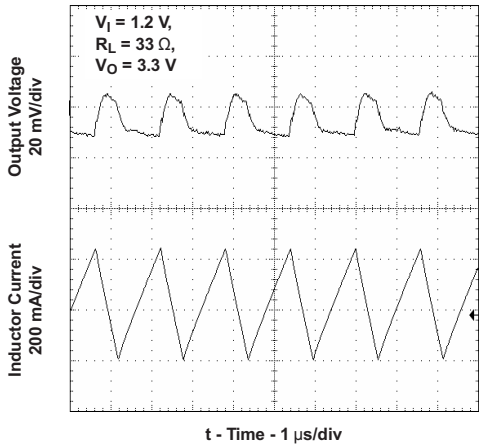


Figure 16. TPS61025 Output Voltage In Continuous Mode

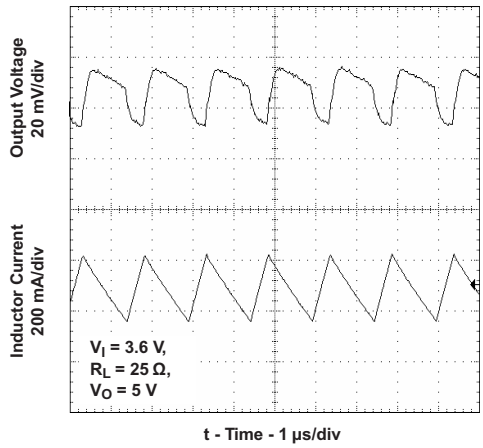


Figure 17. TPS61027 Output Voltage In Continuous Mode

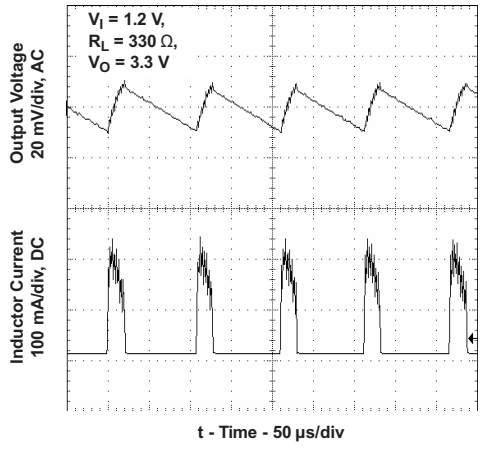


Figure 18. TPS61025 Output Voltage In Power Save Mode

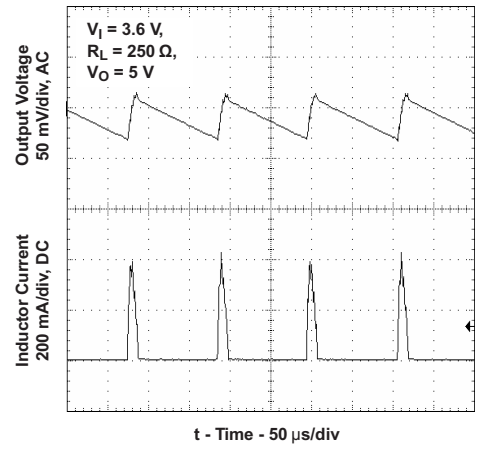


Figure 19. TPS61027 Output Voltage In Power Save Mode

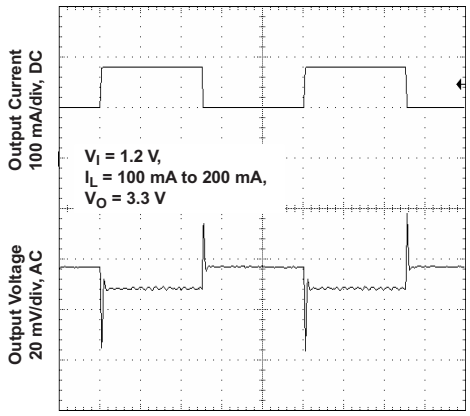


Figure 20. TPS61025 Load Transient Response

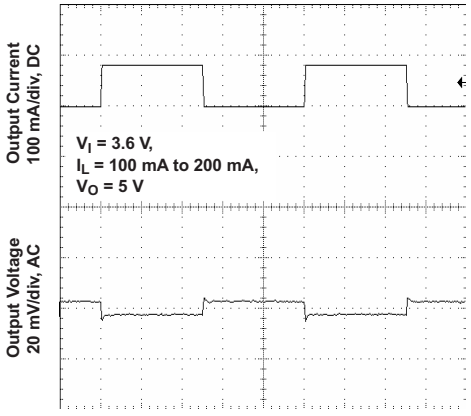


Figure 21. TPS61027 Load Transient Response

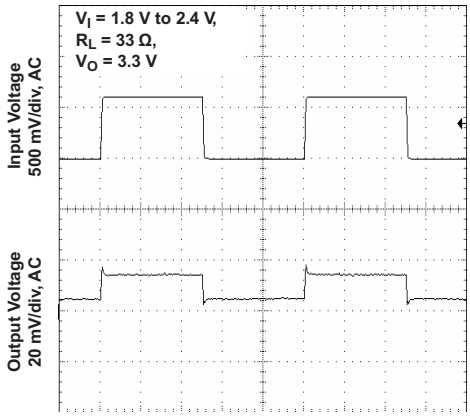


Figure 22. TPS61025 Line Transient Response

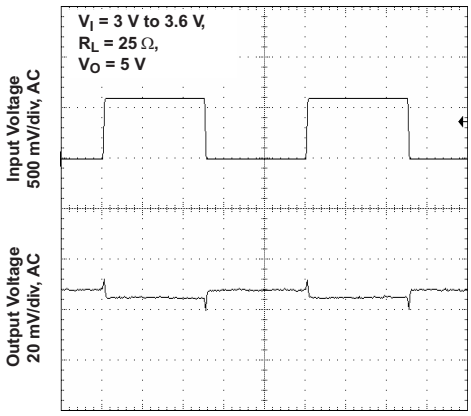


Figure 23. TPS61027 Line Transient Response

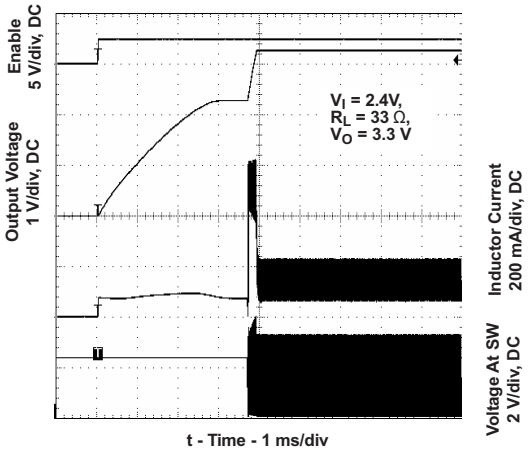


Figure 24. TPS61025 Start-Up After Enable

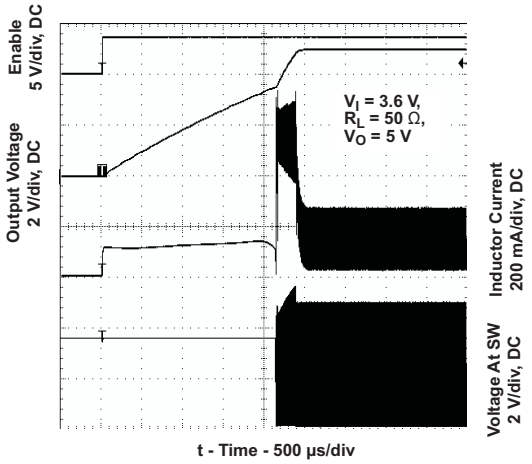


Figure 25. TPS61027 Start-Up After Enable

13 Power Supply Recommendations

This input supply should be well regulated with the rating of TPS6102x. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

14 Layout

14.1 Layout Guidelines

- As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies.
- If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks.
- The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC.
- Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.
- The feedback divider should be placed as close as possible to the control ground pin of the IC.
- To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

14.2 Layout Example

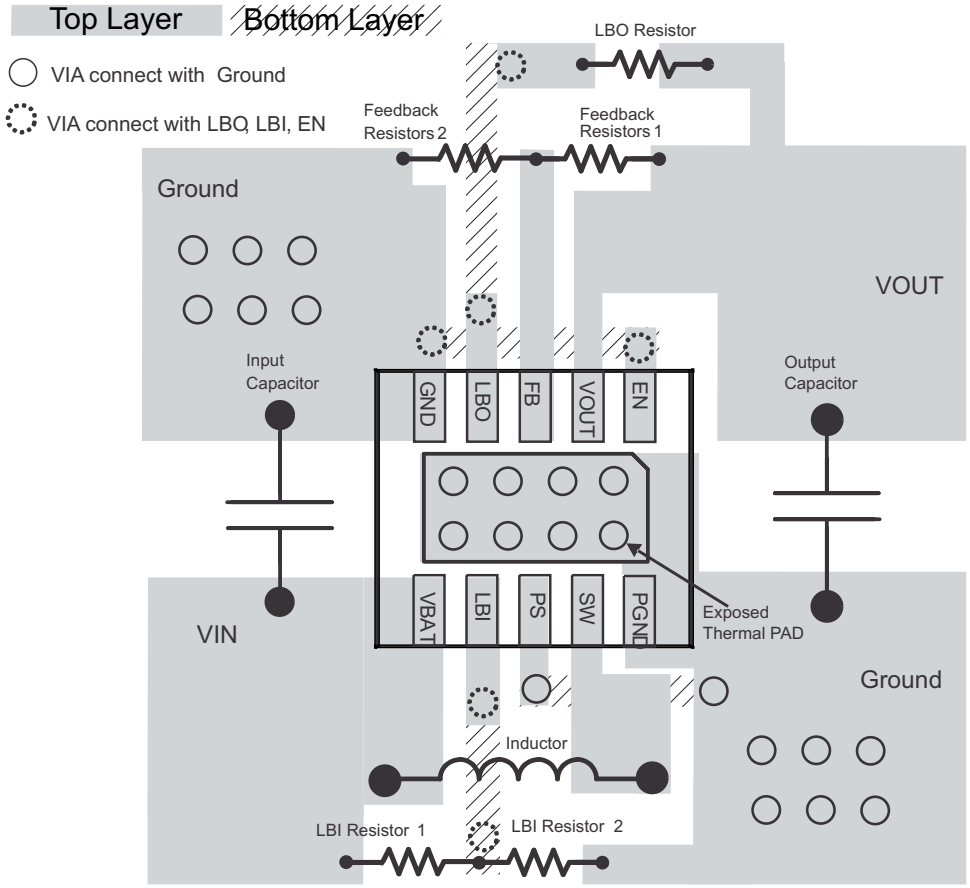


Figure 26. Layout

15 Device and Documentation Support

15.1 Documentation Support

15.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

15.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61025-Q1	Click here	Click here	Click here	Click here	Click here
TPS61027-Q1	Click here	Click here	Click here	Click here	Click here
TPS61029-Q1	Click here	Click here	Click here	Click here	Click here

15.3 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

15.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

15.5 Glossary

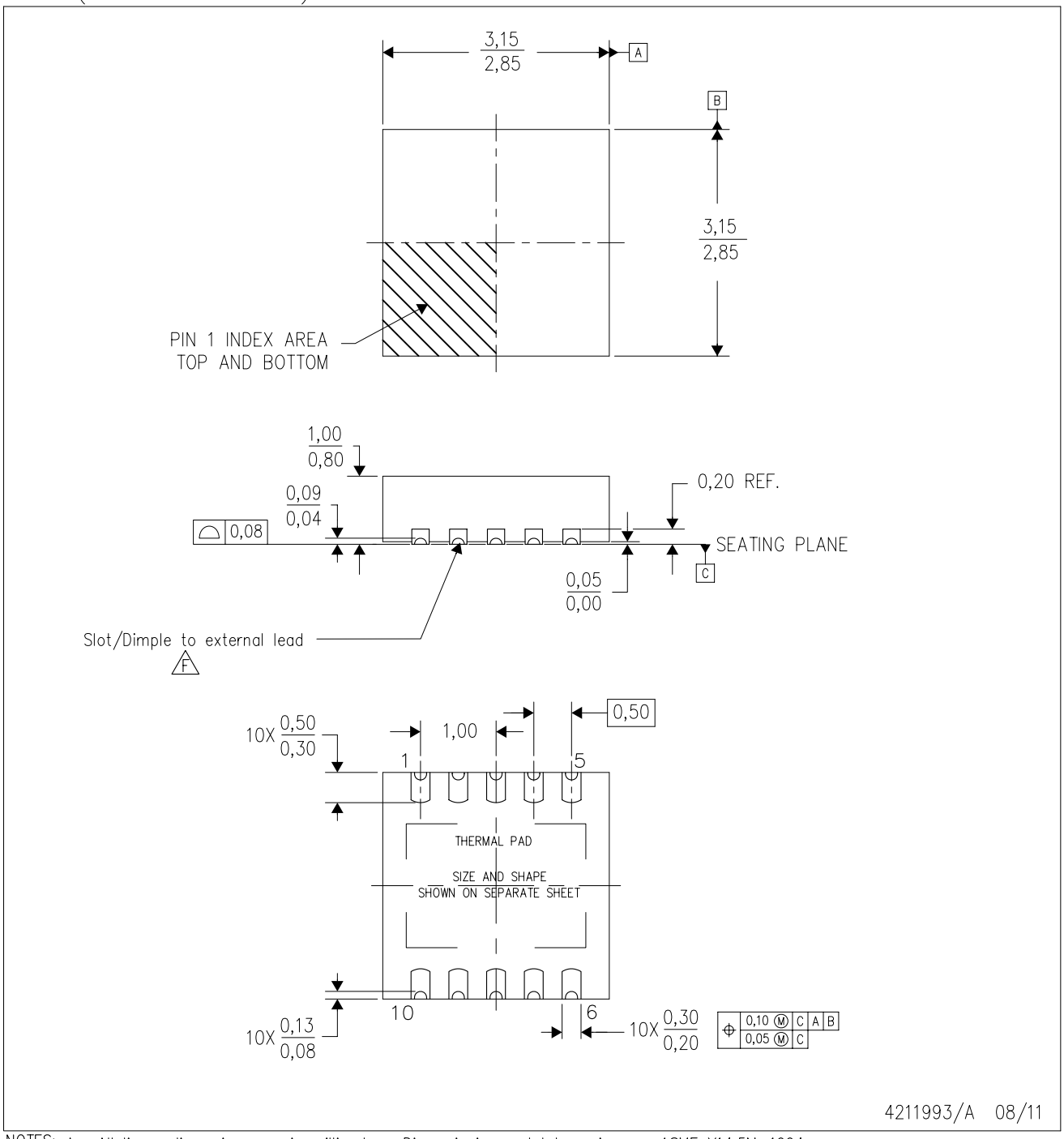
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

16 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

DPN (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Slot/Dimple added to external leads.

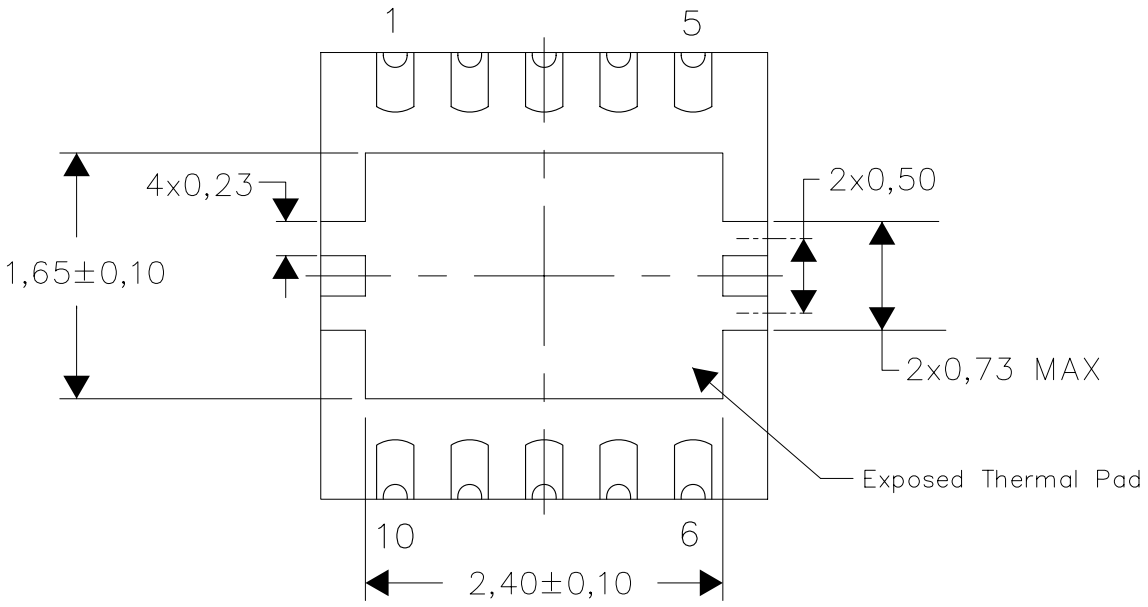
DPN (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212034/A 08/11

NOTES: All linear dimensions are in millimeters

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61029QDPNRQ1	ACTIVE	VSON	DPN	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	61029Q	Samples
TPS61029QDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	OES	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS61029-Q1 :

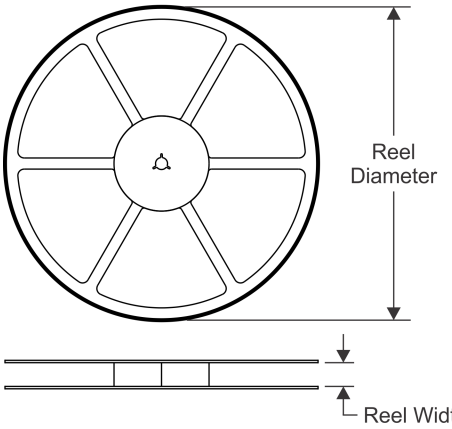
- Catalog: TPS61029

NOTE: Qualified Version Definitions:

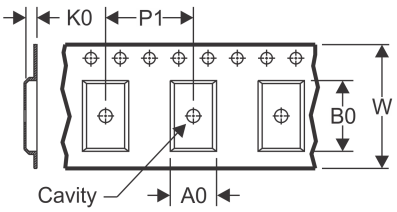
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

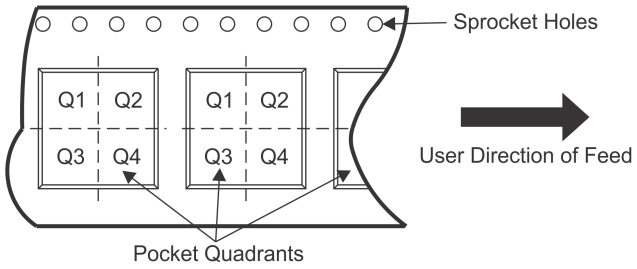


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

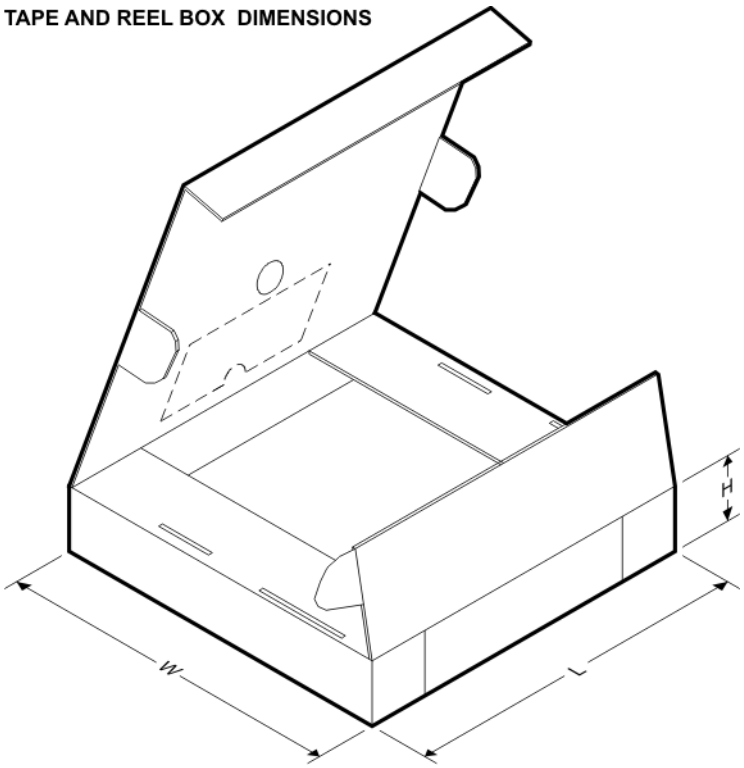
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61029QDPNRQ1	VSON	DPN	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61029QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



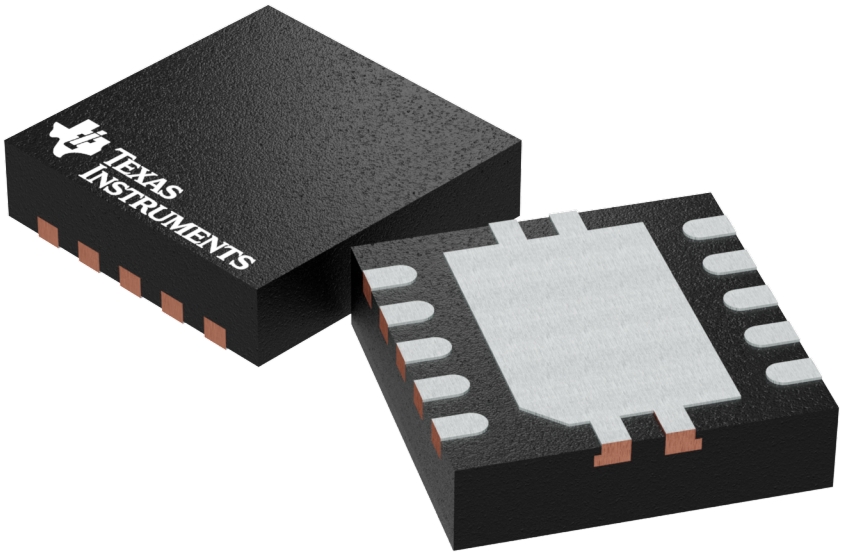
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61029QDPNRQ1	VSON	DPN	10	3000	367.0	367.0	35.0
TPS61029QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

DRC 10

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



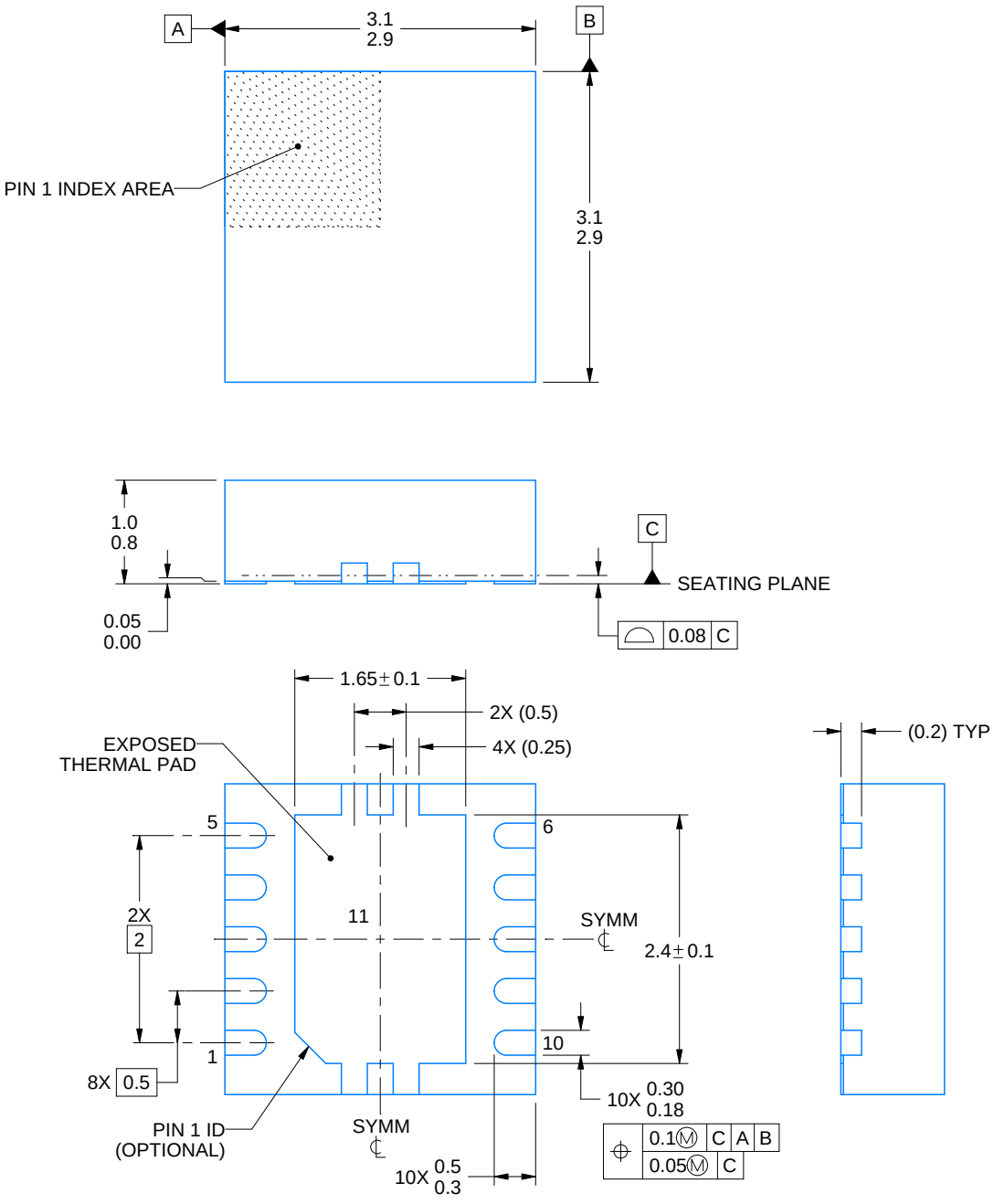
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRC0010J

PACKAGE OUTLINE

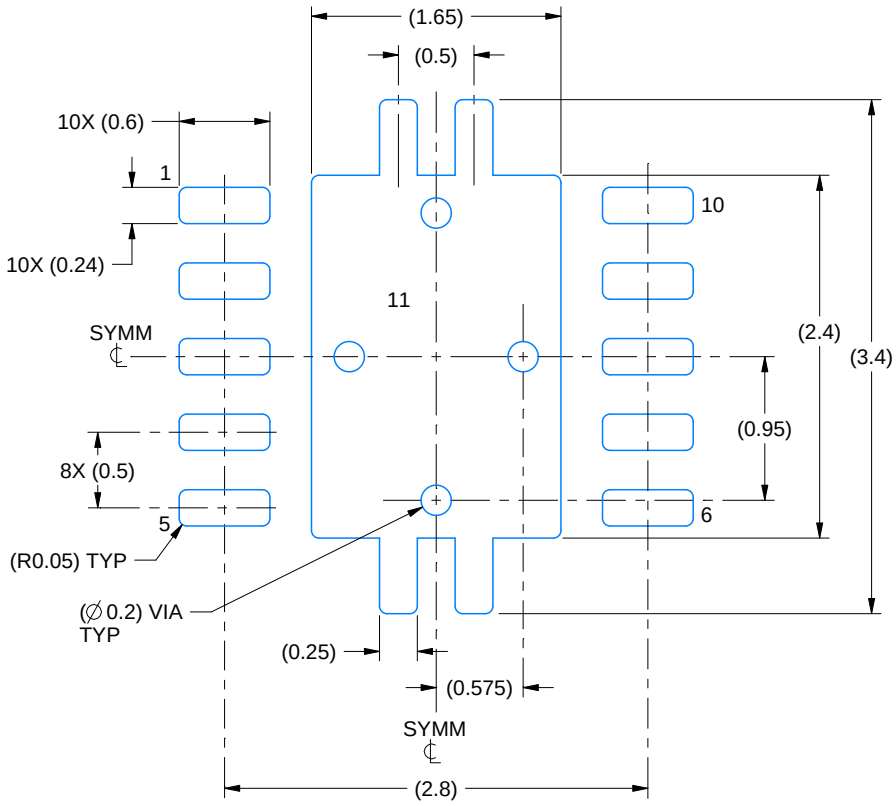
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

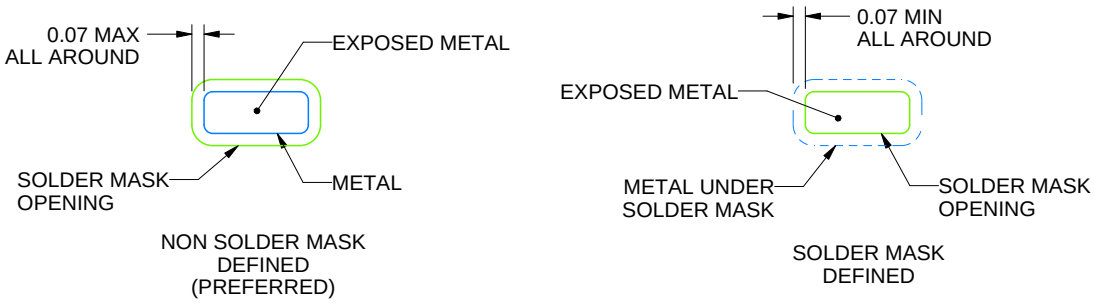


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

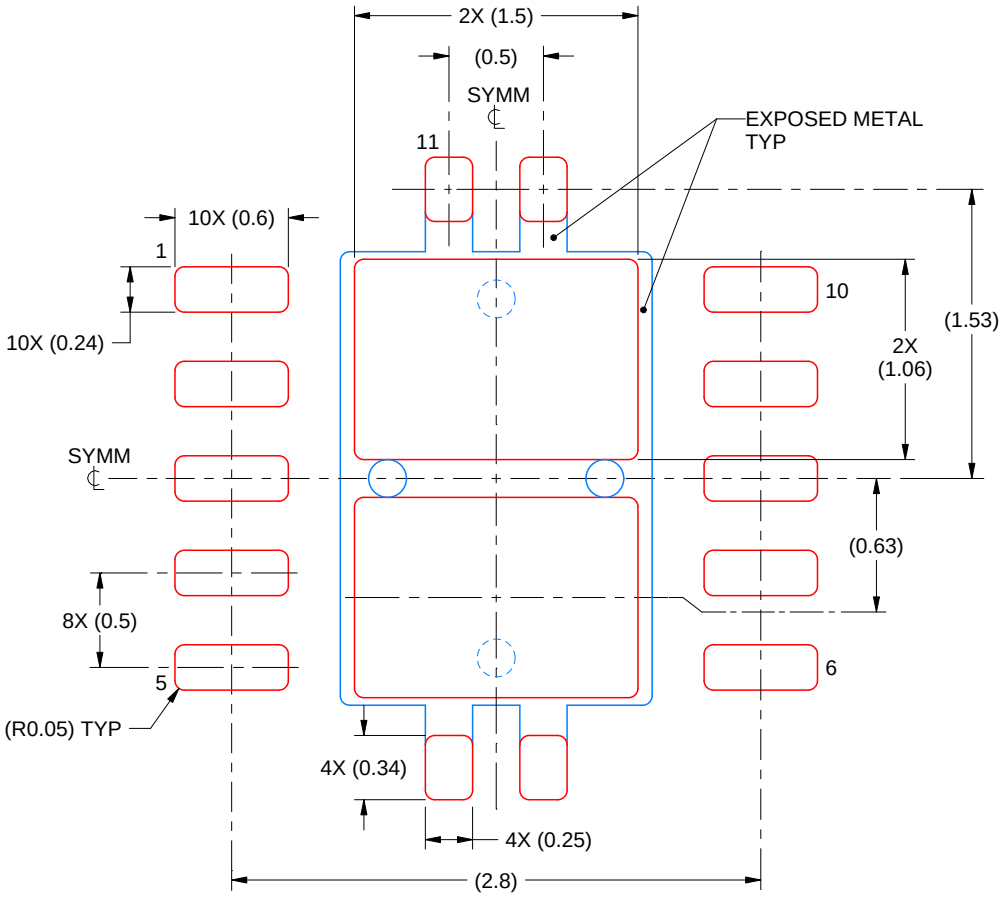
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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