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MC2044C

Postamplifier/Quantizer for Applications from 200 to 622 Mbps
Data Sheet

TABLE OF CONTENTS

Postamplifier/Quantizer for Applications from 200 Mbps to 622 Mbps

FEATURES

- Low-cost IC, fabricated in advanced sub-micron BiCMOS process
- 2 mV typical input sensitivity
- Wide range programmable input-signal level detect
- Fully differential design
- Supports 3.3 V and 5 V supplies
- Available in die form, SOIC16, QSOP16 and BCC++16L packages
- Complimentary PECL data outputs
- Complimentary CMOS signal detect logic outputs

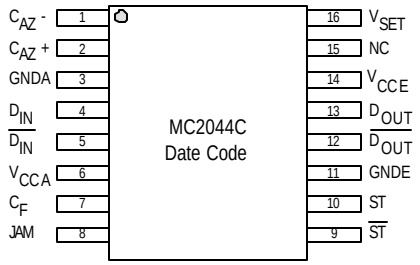
APPLICATIONS

- SDH/SONET/ATM
- Fast Ethernet
- FDDI
- ESCON
- Add/drop multiplexers

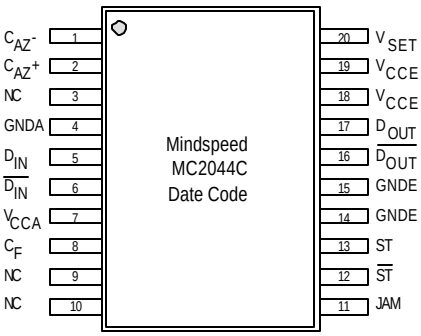
CONNECTIONS

Fig. 1

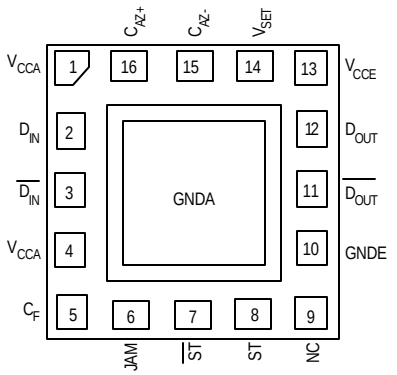
SOIC16
QSOP16
Package



TSSOP20
Package



BCC++16L
Package



DESCRIPTION

The MC2044C is an integrated, high gain limiting amplifier intended for fiber optic communication to 622 Mbps. Normally placed following the photodetector & transimpedance amplifier, the post-amplifier provides the necessary gain to give PECL compatible logic outputs.

The MC2044C also includes a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled. The signal detect function has typically 2.25 dB (optical) of hysteresis which prevents chatter at low input levels.

A JAM function, which turns off the output when no signal is present, is provided by externally connecting the $\overline{ST}$ output to the JAM input.

TABLE 1 ORDERING INFORMATION

Part Number	Pin Package
MC2044CWPDIE	Waffle pack
MC2044CWAFERSPBG	Expanded wafer on a grip ring
MC2044CS16	SOIC16
MC2044CQ16	QSOP16
Contact Sales Representative	TSSOP20
MC2044CB16	BCC++16L
MC2044C-BEVM	BCC16 evaluation board
MC2044C-EVM	QSOP evaluation board

TOP LEVEL DIAGRAM

Fig. 2

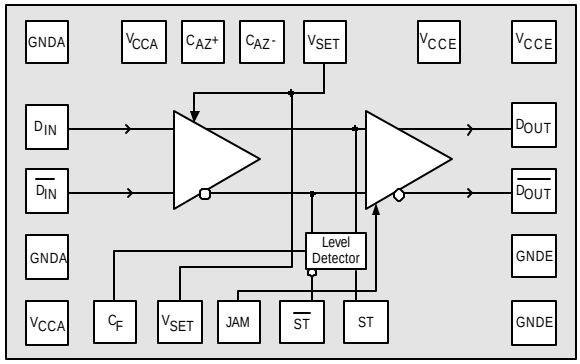


TABLE 2 PIN DESCRIPTION

Name	QSOP16 SOIC16	TSSOP20	BCC++16L	Function
C_{AZ}-	1	1	15	Auto-zero capacitor pin. Connect C_{AZ} between this pin and C_{AZ}+
C_{AZ}+	2	2	16	Auto-zero capacitor pin. Connect C_{AZ} between this pin and C_{AZ}-
GNDA	3	4	-	Analog section ground pin. Connect to most negative supply.Must be at the same potential as GNDE pin
D_{IN}	4	5	2	Differential data input
$\overline{D_{IN}}$	5	6	3	Inverse differential data input
V_{CCA}	6	7	1, 4	Analog section power pin. Connect to most positive supply.Must be at the same potential as V_{CCE} pin
C_F	7	8	5	Level-detect filter capacitor pin. Connect a capacitor between this pin and V_{CCA}
JAM	8	11	6	CMOS and ECL compatible input controlling output buffers (D_{OUT} and $\overline{D_{OUT}}$ pins). On chip pull down defaults to low. Can be driven from CMOS
$\overline{ST}$	9	12	7	Logical inverse of ST pin. Maybe connected to JAM pin to enable automatic squelch function to operate CMOS output
ST	10	13	8	Input signal level status. This CMOS output is LOW when the input signal is below the threshold set by the users
GNDE	11	14, 15	10	Digital section ground pin, Connect to the most negative supply. Must be the same potential as GNDA pin
$\overline{D_{OUT}}$	12	16	11	Differential data output. Logical inverse of D_{OUT} pin. JAM high forces $\overline{D_{OUT}}$ High
D_{OUT}	13	17	12	Differential data output. PECL compatible differential data output. JAM high forces D_{OUT} LOW
V_{CCE}	14	18, 19	13	Digital output section power pin. Connect the most positive supply. Must be at same potential as V_{CCA} pin
NC	15	3, 9, 10	9	Not connected
V_{SET}	16	20	14	Input threshold-level setting circuit. Connect to GND via a resistor

Note:

Pin 17 (center pin) on the BCC++16L package should be connected to GndA.

TABLE 3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC} - GND)	6	V
T_A	Operating ambient	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

TABLE 4 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	3.0 to 5.5	V
T_A	Operating ambient	-40 to +85	°C

TABLE 5 DC CHARACTERISTICS

(V_{CC} = +3.3V ± 10%, T_A = -40°C to +85°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{CC}	Supply current (excluding output current)(1)	-	20	35	mA
V_{OS}	Effective input offset voltage	-	-	50	µV
R_{INJ}	JAM input resistance to ground	-	10	-	kΩ
R_{IN}	Differential Input resistance	-	20	-	kΩ
V_{POH}	PECL (2) output HIGH	V_{CC} - 1.025	-	V_{CC} - 0.880	V
V_{POL}	PECL (2) output LOW	V_{CC} - 1.810	-	V_{CC} - 1.620	V

Dice are designed to operate over an ambient temperature range of -40°C to +85°C (T_A) range, but are tested and guaranteed only at T_A = +25°C.

Note 1: V_{CC} = +3.3 V or +5 V.

Note 2: Load is 50 Ω to V_{CC} - 2 V.

TABLE 6 AC CHARACTERISTICS

(V_{CC}= +3.3 V ±10%, T_A = -40°C to +85°C, unless otherwise noted, Guaranteed by design and characterization.)

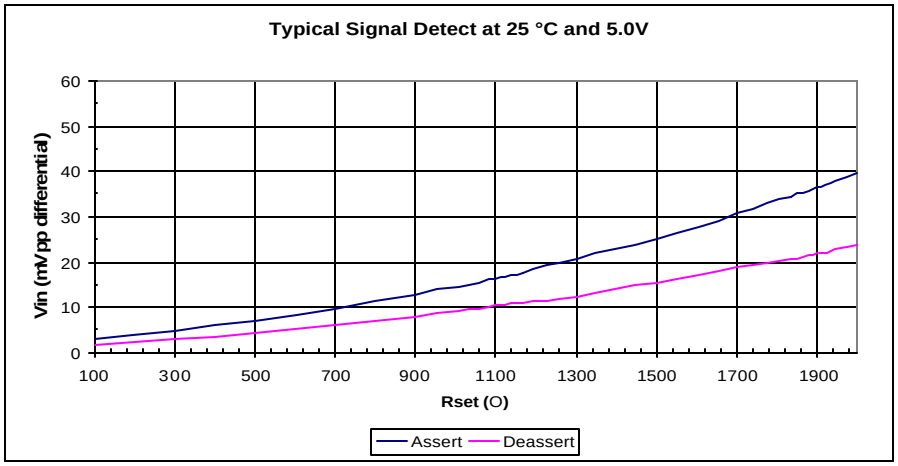
Symbol	Parameter		Min.	Typ.	Max.	Units
V_{IN_MIN}	Input Sensitivity (BER < 10^{-9})		-	2	2.8	mVpp
V_{IN_MAX}	Differential Input Overload (BER < 10^{-9})(1)		800	-	-	mVpp
V_{TH}	Input level detect programmability		2	-	20	mVpp
HYS	Level detect hysteresis (optical)		1.75	2.25	2.75	dB
BW	Small Signal Bandwidth		-	450	-	MHz
C_{IN}	Input capacitance		-	-	2	pF
t_{PWD}	Pulse width distortion		-	-	30	ps
t_R, t_F	Data output rise/fall times (20 - 80%)		-	210	-	ps
T_{LD}	Signal level detect time constant (C1, C2, C_{AZ} and C_F as shown in Figure 5)	Assert level Deassert level		40 40	100 100	µs
V_N	Input noise in 311 MHz		-	200	-	μV_{RMS}

Dice are designed to operate over an ambient temperature range of -40°C to +85°C (T_A) range, but are tested and guaranteed only at T_A = +25°C.

Note 1: Differential voltage is $|V_{DIN} - V_{\overline{DIN}}|$. No single input should exceed 400 mVpp.

TYPICAL PERFORMANCE CURVES

Fig. 3



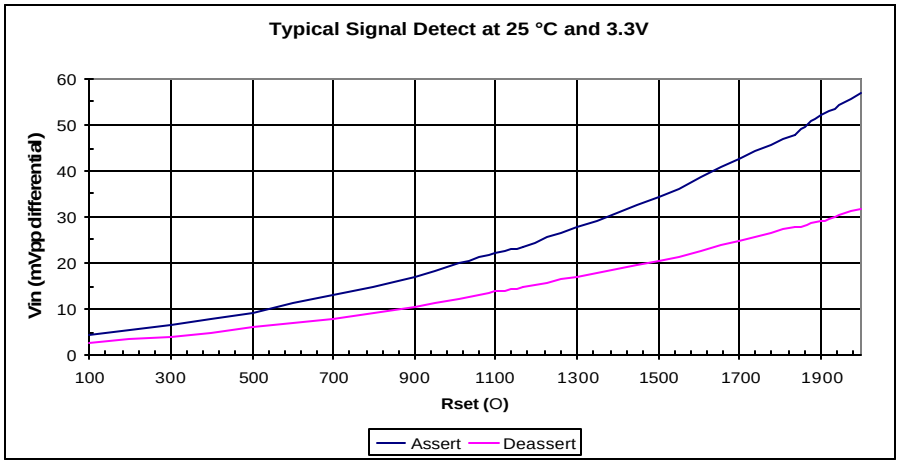
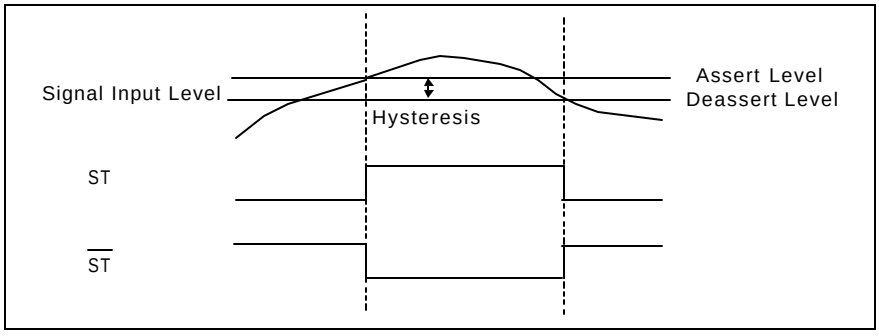


Fig. 3a

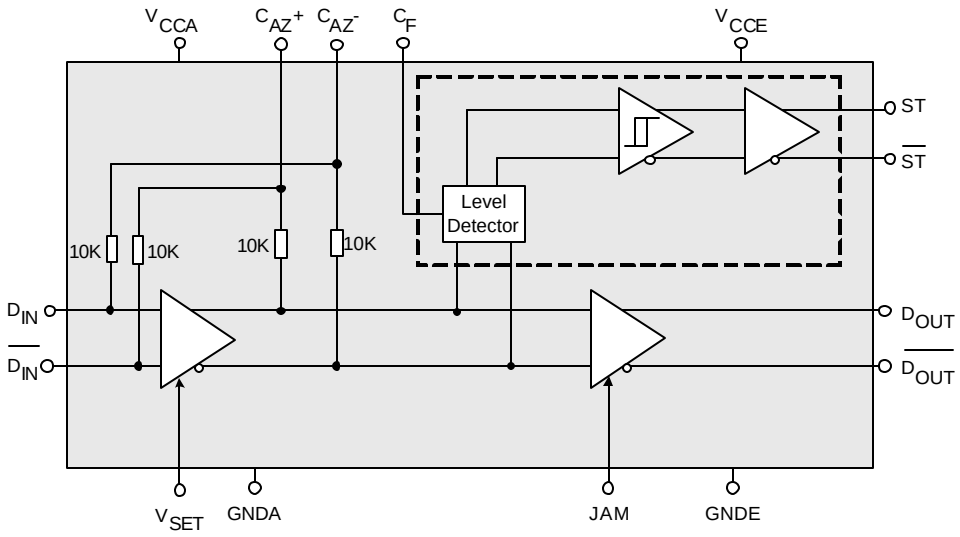


ASSERT DEASSERT LEVEL

Fig. 3a shows the operation of the signal detect function as the signal level varies. The top line indicates the assert level, the bottom the deassert level. The difference between the two levels is the hysteresis. When the signal level goes above the assert level the ST output switches high ($\overline{ST}$ switches low). When the signal level falls below the deassert level, ST output switches low ($\overline{ST}$ switches high).

FUNCTIONAL BLOCK DIAGRAM

Fig. 4



FUNCTIONAL DESCRIPTION

Data Input

The Data Input pins are internally DC-biased at approximately V_{CC} - 1V. The MC2044C inputs are AC coupled, using external capacitors. The capacitors must be large enough to pass the lowest frequencies of interest (consecutive '1's or '0's) considering the input resistance. For example, at 155 Mbps SONET, there can be up to a maximum of 72 consecutive '1's, which is 465 ns.

To minimize the data dependant jitter, the low frequency cut-off needs to be lower by a factor of 10. However, it is better to set it a further decade lower due to the interaction of the time constants for the input stage and the DC restore circuitry. For example setting C1, C2 (Fig. 5) to 10 nF will give a typical -3 dB point of approximately 3.5 kHz.

DC Offset Compensation

Internal feedback is included to remove the effects of DC offsets and acts as a DC auto zero circuit. An external capacitor (C_{AZ}) acting with the internal circuit feedback resistors (typically 10 kΩ) ensures that the feedback is effective only at frequencies below the lowest frequency of interest. C_{AZ} is normally set to 10 nF.

Signal Level Detector (Fig. 5)

The gain of the first stage is determined by R_{SET}. This amplification sets the level of input at which the status thresholds operate. The data is then rectified and low-pass filtered before being compared with a reference voltage. The low-pass filter is formed by C_F (Fig. 5) and an on chip resistor.

With C_F equal to 10 nF the time constant is nominally 2 µs, avoiding false triggering due to variation in edge density of data.

Setting Signal Detect Level

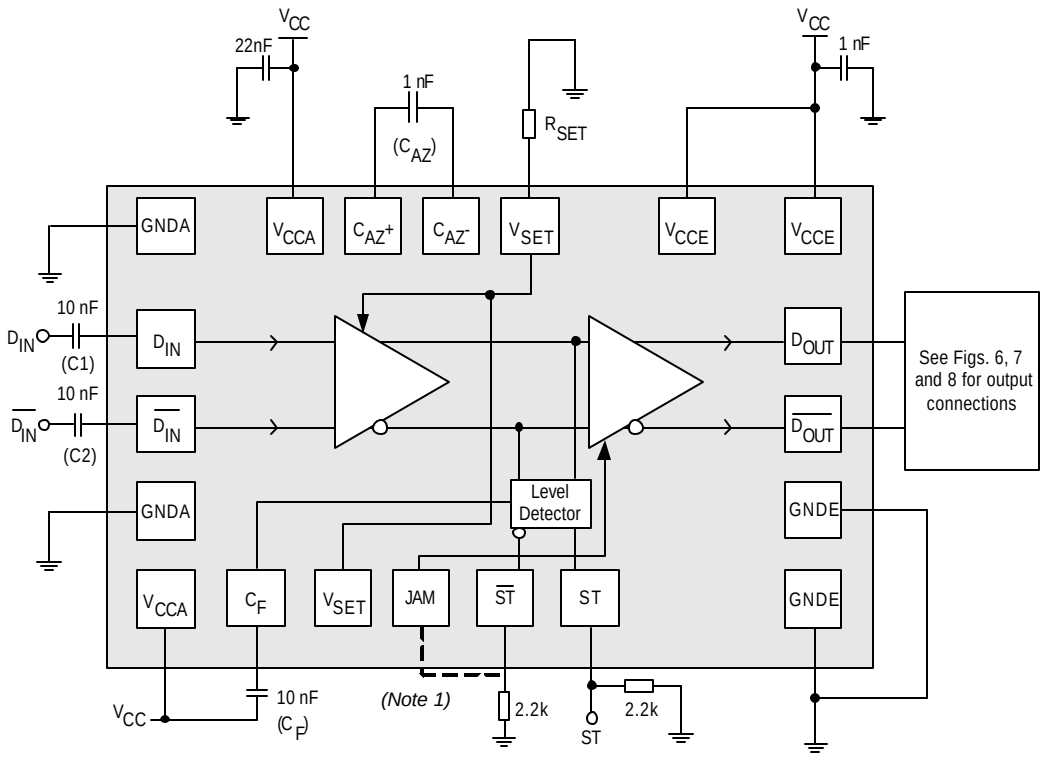
R_{SET} is chosen using the graphs in Fig. 3 to determine the input signal level at which ST goes high (Assert). The value is dependant on supply voltage and should be chosen for 3.3 V or 5 V operation. If 3.3 V and 5 V operation are to be supported interchangeably set R_{SET} based on the 3.3 V graphs.

The comparator following the level detector has the equivalent of 2.25 dB (typical) of optical hysteresis, and this determines the deassert level (ST goes LOW).

If the level detect function is not required connect V_{SET} to GndA (maximum gain).

TYPICAL APPLICATIONS CIRCUIT

Fig. 5



Note 1: Optional connection to enable JAM function

APPLICATIONS INFORMATION

JAM Function

The JAM function sets the data output to a fixed state when no valid signal is present at the input. This is implemented by externally connecting the $\overline{ST}$ output to the JAM input.

This is normally used to allow data to propagate only when the signal is above the users' Bit-Error-Rate (BER) requirement. It therefore stops the data outputs toggling due to noise when no signal is present.

D_{OUT} and $\overline{D_{OUT}}$ PECL Termination

The outputs of the MC2044C are PECL compatible and any standard AC or DC-coupling termination technique can be used. Fig. 6 and 7 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drift and compatibility with non-PECL interfaces. Fig. 6 shows the circuit configuration and Table 7 the resistor values. If using transmission lines other than 50 ohms, the shunt terminating resistance Z_T should equal twice the impedance of the transmission line (Z_O).

DC-coupling can be used when driving PECL interfaces and has the advantage of a reduced component count. A Thevenin termination is used at the receive end to give a 50 Ω load and the correct DC bias. Fig. 7 shows the circuit configuration and Table 7 the resistor values.

Alternatively, if available, terminating to V_{CC} - 2V as shown in Fig. 8 has the advantage that the resistance value is the same for 3.3 V and 5 V operation and it also has performance advantages at high data rates.

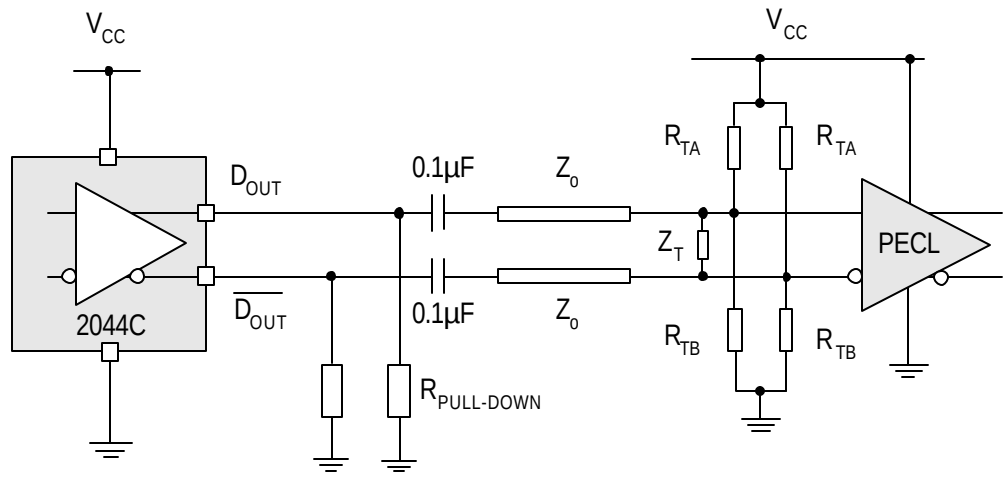
APPLICATIONS INFORMATION

TABLE 7 TERMINATION RESISTOR VALUES

Supply	Output Impedance	$R_{PULL-DOWN}$	Z_T	R_{TA} / R_{TB}	R_T / R_B
5 V	50 Ω	270 Ω	100 Ω	2.7 kΩ / 7.8 kΩ	82 Ω / 130 Ω
3.3 V	50 Ω	150 Ω	100 Ω	2.7 kΩ / 4.3 kΩ	130 Ω / 82 Ω

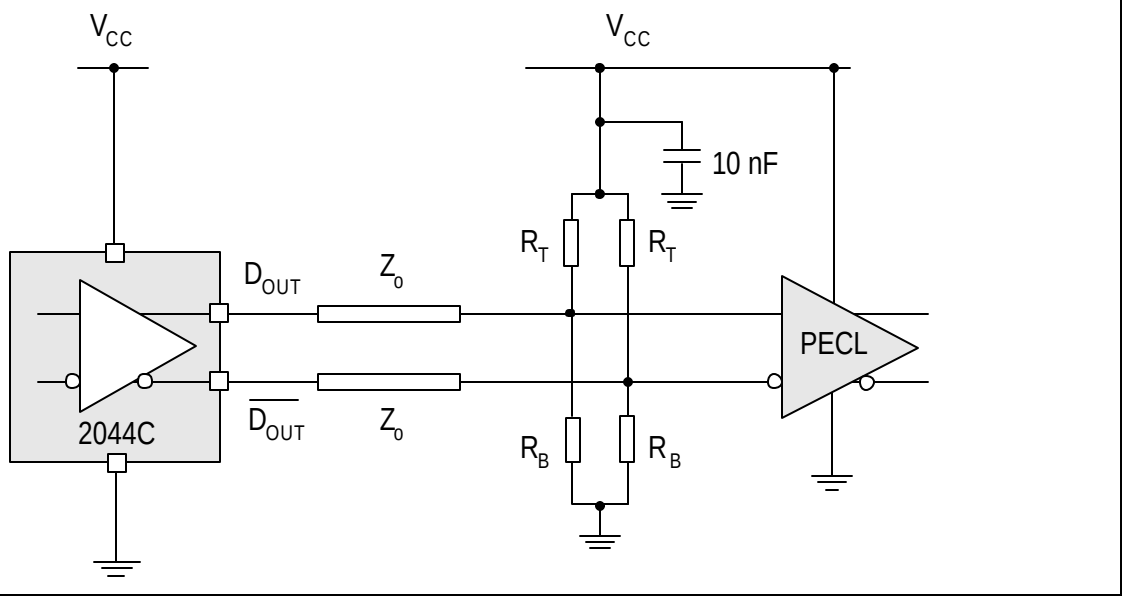
AC-COUPLED PECL TERMINATION

Fig. 6



DC-COUPLED PECL TERMINATION

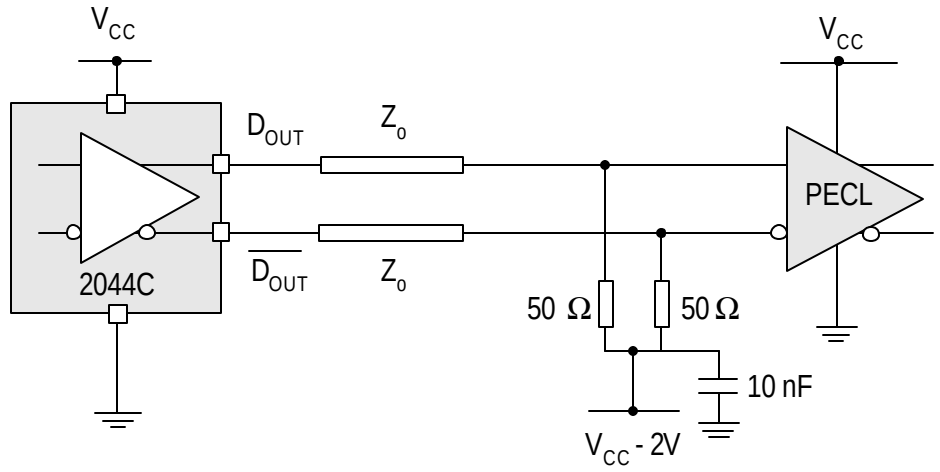
Fig. 7



APPLICATIONS INFORMATION

ALTERNATIVE PECL TERMINATION

Fig. 8



Power supply decoupling & optimizing sensitivity

In most applications the MC2044C will give adequate performance without ferrite beads. In applications where maximum sensitivity is required V_{CCA} and GNDA may be connected to their respective power rails via a ferrite suppressor, such as a Murata BLM31A601SPT.

Capacitors should be chosen with low effective series resistance, low dissipation factor and high Q. NPO or COG temperature characteristics are preferred because they provide more reliable performance over a wide range of environmental conditions.

Small surface mount packages are recommended since they exhibit less parasitic inductance which can lower the overall effectiveness of the bypass capacitor at high frequencies. Filter capacitors should be placed close to power and ground pins to minimize noise coupling.

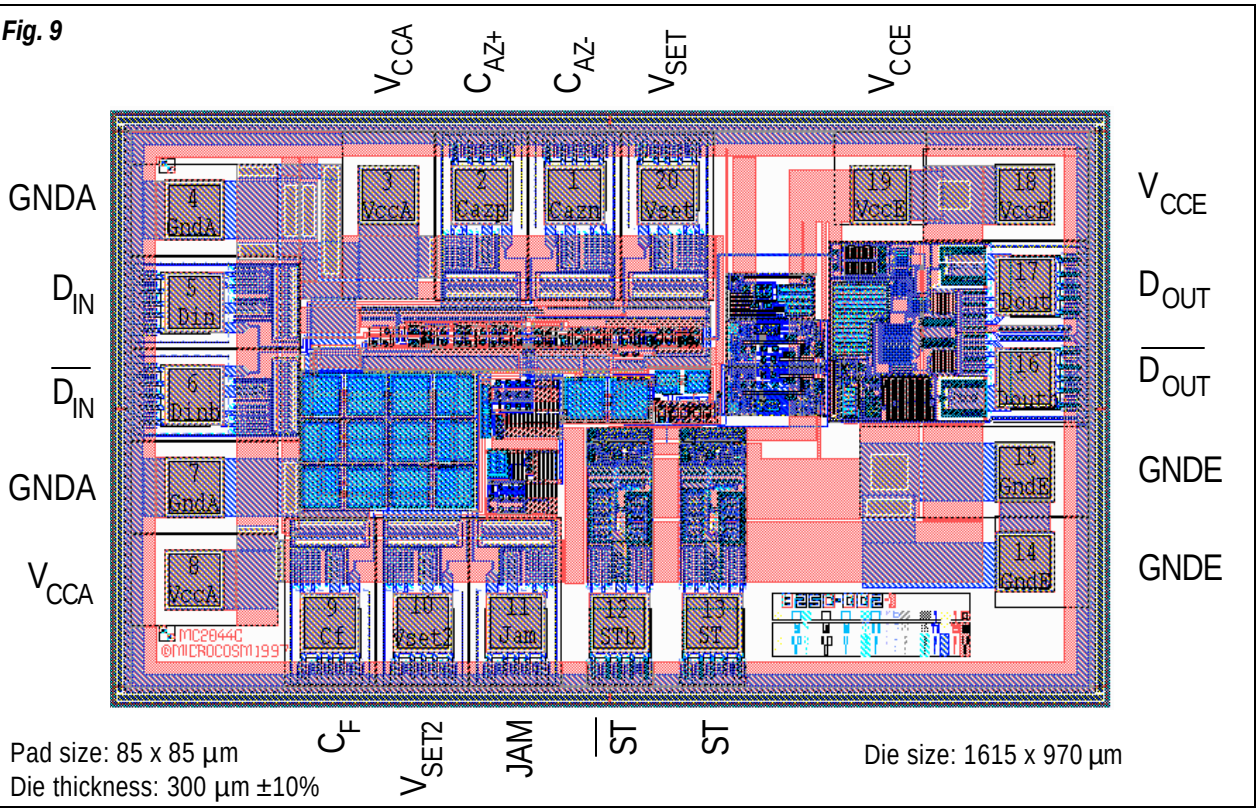
Differences between die and packaged parts

The die has two V_{SET} pads. Connect one or the other, but not both.

There are two sets of V_{CCA} and GNDA pads on the left of the die. Although two pairs are provided only one pair need be connected. On the TSSOP package, pairs of V_{CCE} and GNDE pins are connected.

BARE DIE INFORMATION

Fig. 9



Pad size: 85 x 85 µm
Die thickness: 300 µm ±10%

Die size: 1615 x 970 µm

TABLE 8 PAD CENTERS

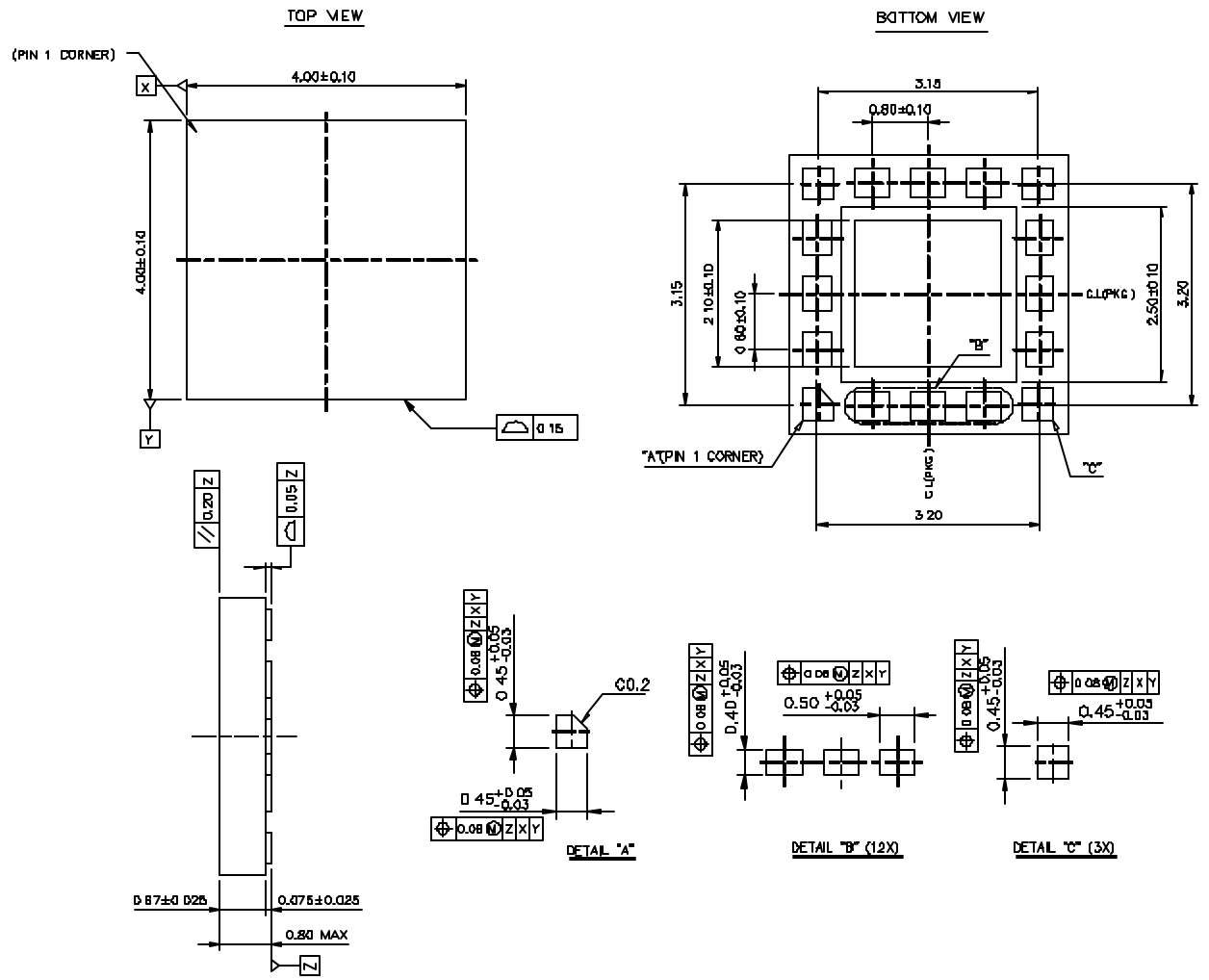
Description	X	Y
C_{AZ}-	-55	350
C_{AZ}+	-205	350
V_{CCA}	-360	350
GNDA	-670	320
D_{IN}	-670	170
$\overline{D_{IN}}$	-670	20
GNDA	-670	-130
V_{CCA}	-670	-280
C_F	-450	-350
V_{SET2}	-300	-350

Description	X	Y
JAM	-150	-350
$\overline{ST}$	15	-350
ST	165	-350
GNDE	670	-250
GNDE	670	-100
$\overline{D_{OUT}}$	670	50
D_{OUT}	670	200
V_{CCE}	670	350
V_{CCE}	440	350
V_{SET}	90	350

Note: Pad coordinates are in µm, and are measured from the center of the die to the center of the pad.

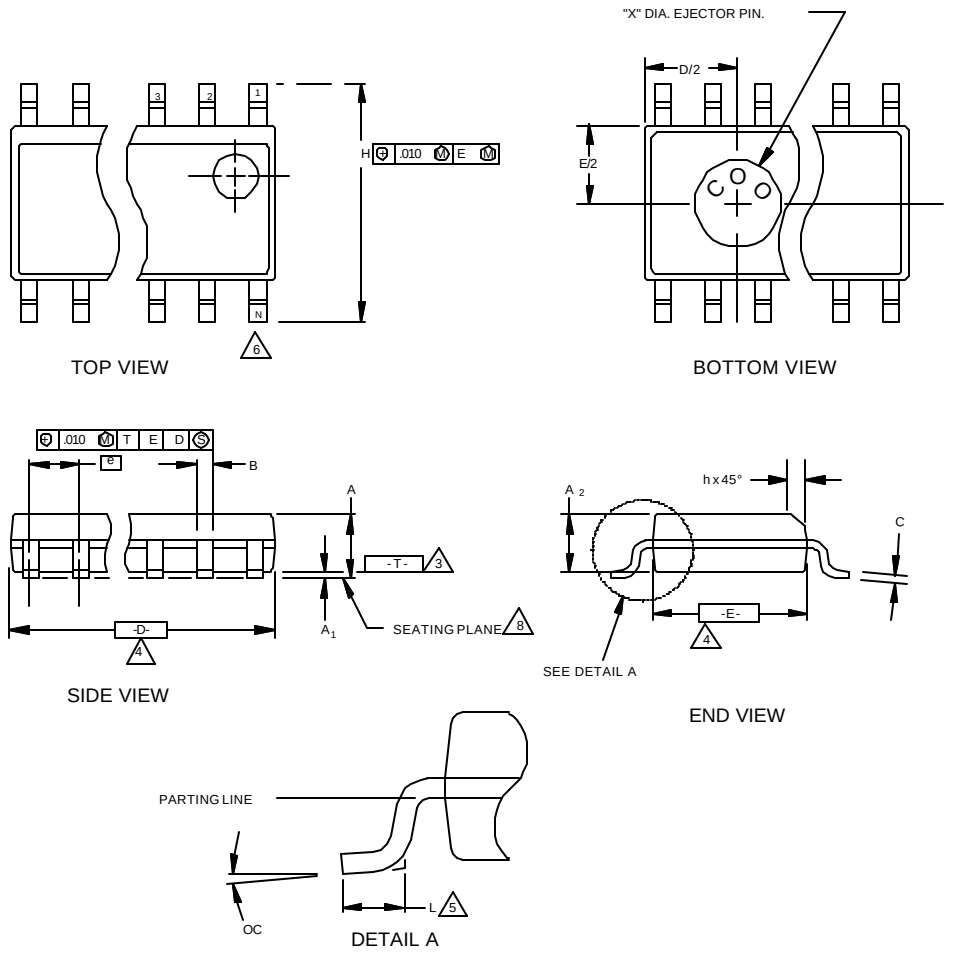
BCC++16L PACKAGE OUTLINE

Fig. 10



SOIC16 PACKAGE INFORMATION

Fig. 11



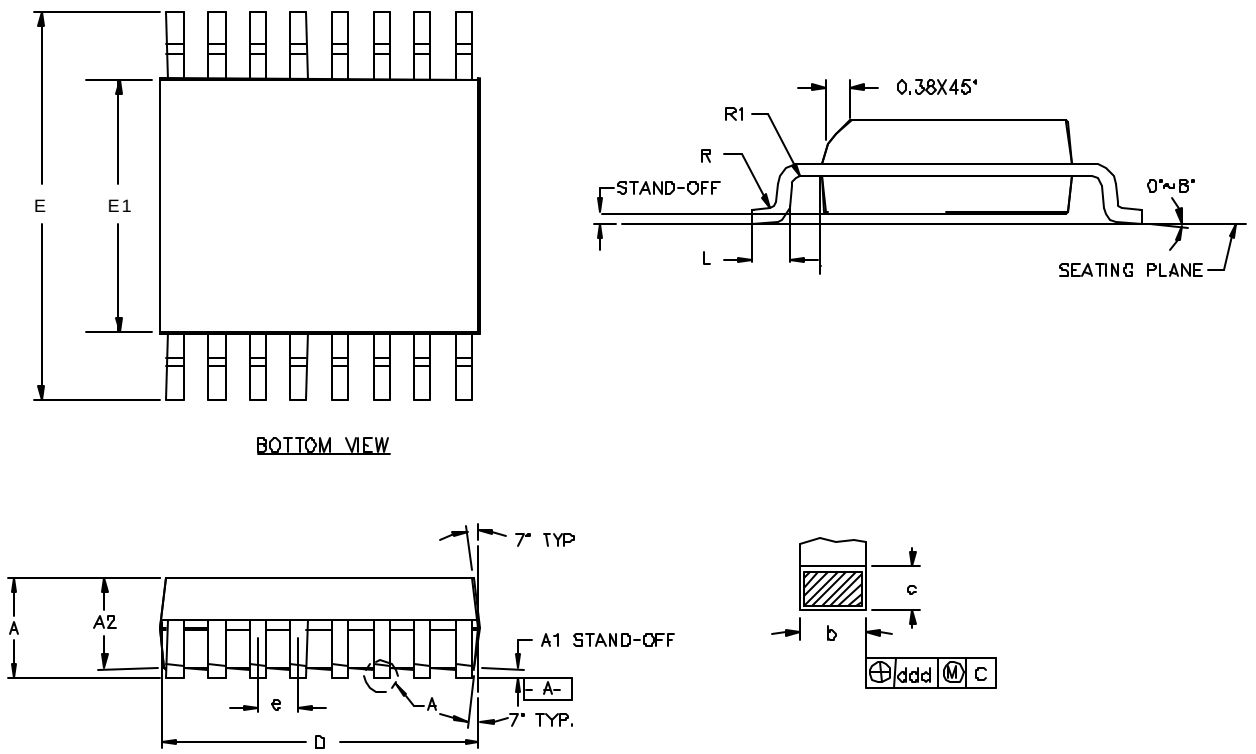
NOTES:

2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES AT END AND .010 INCHES AT WINDOW
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
11. CONTROLLING DIMENSION: INCHES.
12. THIS PART IS COMPLIANT WITH JEDEC STANDARD MS-012, VARIATION AA, AB & AC.

Note: Please see dimensions in Table 9.

QSOP16 PACKAGE INFORMATION

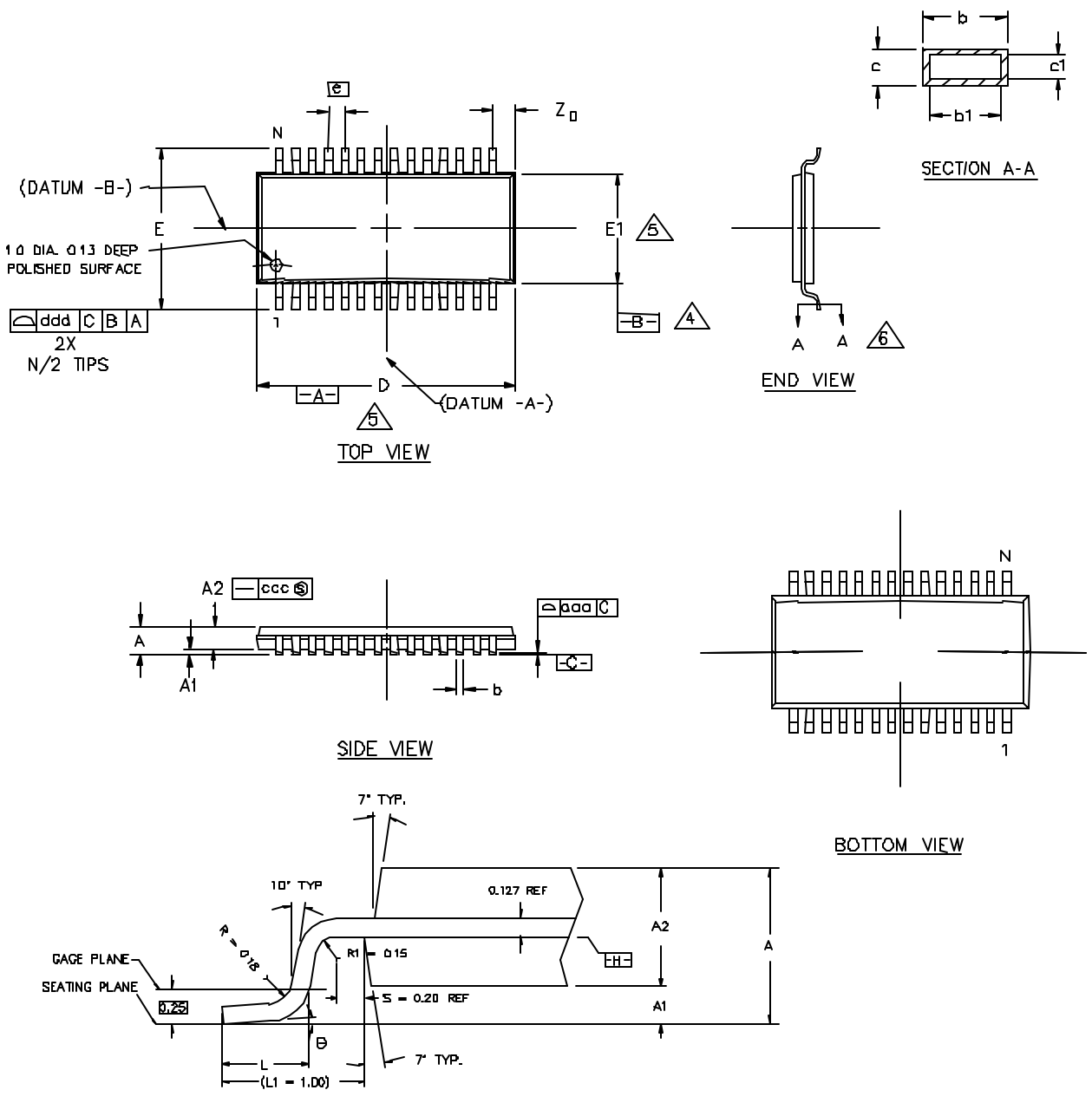
Fig.12



Note: Please see dimensions in Table 10.

TSSOP20 PACKAGE INFORMATION

Fig.11



Note: Please see dimensions in Table 11.

PACKAGE DIMENSIONS

TABLE 9 SOIC16 DIMENSIONS

Symbol	Min.	Nom.	Max.
A	1.55	1.63	1.73
A1	0.127	0.15	0.25
A2	1.40	1.47	1.55
B	0.35	0.41	0.49
C	0.19	0.20	0.25
D	9.80	9.93	9.98
E	3.81	3.94	3.99
e		1.27 BSC	
H	5.84	5.99	6.20
h	0.25	0.33	0.41
L	0.41	0.64	0.89
N		16	
α	0°	5°	8°
X	2.16	2.36	2.54

TABLE 10 QSOP16 DIMENSIONS

Symbol	Tols/N	QSOP16
A	MAX.	1.60
A1	±.05	0.1
A2	±.05	1.40
D	±.05	4.95
E	±.10	6.00
E1	±.05	3.90
L	±.15	0.60
ccc	MAX.	0.080
ddd	MAX.	0.10
e	BASIC	0.635
b	±.025	0.224
c	±.02	0.22
R	±.05	0.25
R1	Min.	0.20

TABLE 11 TSSOP20 DIMENSIONS

Symbol	Tols/leads	TSSOP20L
A	MAX	1.20
A1		0.5MIN/.10MAX.
A2	NOM	.90
D	±.05	6.50
E	±.10	6.40
E1	±.10	4.40
L	+.15/-.10	.60
L1	REF.	1.00
Zp	REF.	.325
e	BASIC	.65
b	±.05	.22
c		.13MIN/.20MAX
e	±4°	4°
aaa	MAX.	.10
bbb	MAX.	.10
ccc	MAX	.05
ddd	MAX.	.20

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