M58WR016KU M58WR016KL
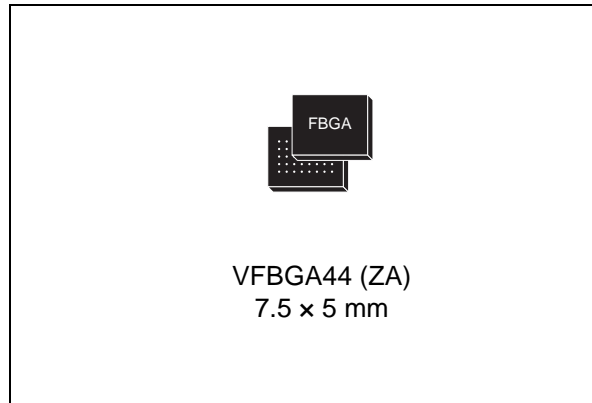# M58WR032KU M58WR032KL

16- or 32-Mbit (×16, Mux I/O, Multiple Bank, Burst) 1.8 V supply Flash memories

Data Brief

Features

- Supply voltage
  - V_{DD} = 1.7 V to 2 V for Program, Erase and Read
  - V_{DDQ} = 1.7 V to 2 V for I/O buffers
  - V_{PP} = 9 V for fast Program
- Multiplexed address/data
- Synchronous / Asynchronous Read
  - Synchronous Burst Read mode: 86 MHz
  - Random access: 60 ns, 70 ns
- Synchronous Burst Read Suspend
- Programming time
  - 10 µs by word typical for Factory Program
  - Double/Quadruple Word Program option
  - Enhanced Factory Program options
- Memory blocks
  - Multiple Bank memory array: 4 Mbit Banks
  - Parameter Blocks (top or bottom location)
- Dual operations
  - Program Erase in one Bank while Read in others
  - No delay between Read and Write operations
- Block locking
  - All blocks locked at Power up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for Block Lock-Down
- Security
  - 128 bit user programmable OTP cells
  - 64 bit unique device number
- Common Flash Interface (CFI)
- 100 000 program/erase cycles per block

VFBGA44 (ZA)
7.5 × 5 mm

- Electronic signature
  - Manufacturer Code: 20h
  - Top device code,
    M58WR016KU: 8823h
    M58WR032KU: 8828h
  - Bottom device code,
    M58WR016KL: 8824h
    M58WR032KL: 8829h
- ECOPACK® packages available

For further information contact your local STMicroelectronics sales office.

www.st.com

1   Description

The M58WR016KU/L and M58WR032KU/L are 16-Mbit (1 Mbit ×16) and 32- Mbit (2 Mbit ×16) non-volatile Flash memories, respectively. In the rest of the document, they will be referred to as M58WRxxxKU/L unless otherwise specified.

The M58WRxxxKU/L may be erased electrically at block level and programmed in-system on a word-by-word basis using a 1.7 V to 2 V V_{DD} supply for the circuitry and a 1.7 V to 2 V V_{DDQ} supply for the Input/Output pins. An optional 9 V V_{PP} power supply is provided to speed up customer programming.

The first sixteen address lines are multiplexed with the Data Input/Output signals on the multiplexed address/data bus ADQ0-ADQ15. The remaining address lines, A16-Amax, are the Most Significant Bit addresses.

The device features an asymmetrical block architecture:

● the M58WR016KU/L have an array of 39 blocks, and are divided into 4 Mbit banks. There are 3 banks each containing 8 main blocks of 32 KWords, and one parameter bank containing 8 parameter blocks of 4 KWords and 7 main blocks of 32 KWords.

● the M58WR032KU/L have an array of 71 blocks, and are divided into 4 Mbit banks. There are 7 banks each containing 8 main blocks of 32 KWords, and one parameter bank containing 8 parameter blocks of 4 KWords and 7 main blocks of 32 KWords

The Multiple Bank Architecture allows Dual Operations, while programming or erasing in one bank, Read operations are possible in other banks. Only one bank at a time is allowed to be in Program or Erase mode. It is possible to perform burst reads that cross bank boundaries. The Parameter Blocks are located at the top of the memory address space for the M58WR016KU and M58WR032KU, and at the bottom for the M58WR016KL and M58WR032KL.

Each block can be erased separately. Erase can be suspended, in order to perform program in any other block, and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100 000 cycles using the supply voltage V_{DD}. There are two Enhanced Factory programming commands available to speed up programming.

Program and Erase commands are written to the Command Interface of the memory. An internal Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports synchronous burst read and asynchronous read from all blocks of the memory array; at power-up the device is configured for asynchronous read. In synchronous burst mode, data is output on each clock cycle at frequencies of up to 86 MHz. The synchronous burst read operation can be suspended and resumed.

The device features an Automatic Standby mode. When the bus is inactive during Asynchronous Read operations, the device automatically switches to the Automatic Standby mode. In this condition the power consumption is reduced to the standby value I_{DD4} and the outputs are still driven.

The M58WRxxxKU/L features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at Power-Up.

The device includes a Protection Register to increase the protection of a system's design. The Protection Register is divided into two segments: a 64 bit segment containing a unique device number written by ST, and a 128 bit segment One-Time-Programmable (OTP) by the user. The user programmable segment can be permanently protected.

The memory is available in a VFBGA44 7.5 × 5 mm, 10 × 4 active ball array, 0.5 mm pitch package. It is supplied with all the bits erased (set to '1').

Figure 1.   Logic diagram
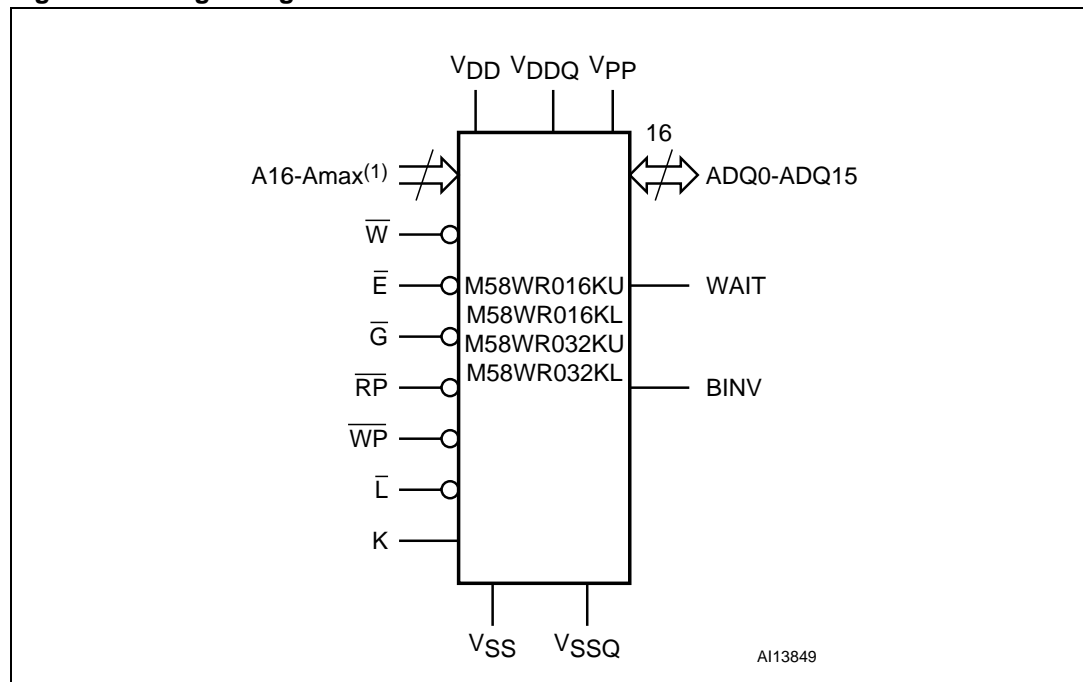
1.   Amax is equal to A19 in the M58WR016KU/L and, to A20 in the M58WR032KU/L.

Table 1.   Signal names

Signal name	Function	Direction
A16-Amax[1]	Address inputs	Inputs
ADQ0-ADQ15	Data Input/Outputs or Address Inputs, Command Inputs	I/O
$\overline{E}$	Chip Enable	Input
$\overline{G}$	Output Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{RP}$	Reset/Power-down	Input
$\overline{WP}$	Write Protect	Input
K	Clock	Input
$\overline{L}$	Latch Enable	Input
WAIT	Wait	Output
BINV	Bus Invert	Input
V_{DD}	Supply voltage	
V_{DDQ}	Supply voltage for input/output buffers	
V_{PP}	Optional supply voltage for fast Program & Erase	
V_{SS}	Ground	
V_{SSQ}	Ground input/output supply	
NC	Not connected internally	

1.   Amax is equal to A19 in the M58WR016KU/L and, to A20 in the M58WR032KU/L.

**Figure 2.   VFBGA44 connections (top view through package)**
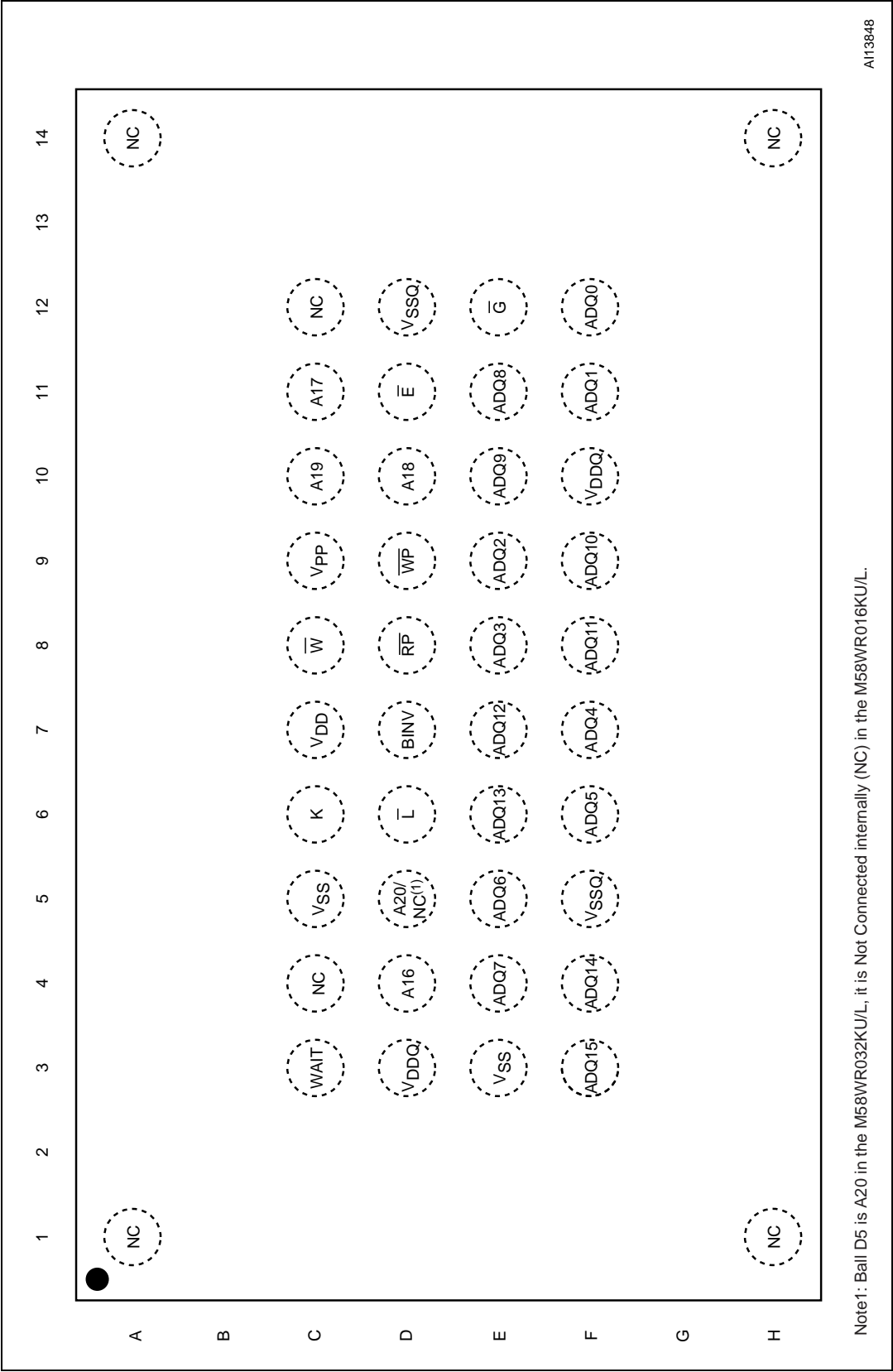
2   Package mechanical

In order to meet environmental requirements, ST offers the M58WRxxxKU/L in ECOPACK®
packages. These packages have a Lead-free second-level interconnect. The category of
Second-Level Interconnect is marked on the package and on the inner box label, in
compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

**Figure 3.   VFBGA44 7.5 × 5 mm, 10 × 4 ball array, 0.50 mm pitch, bottom view
package outline**

BGA-Z52
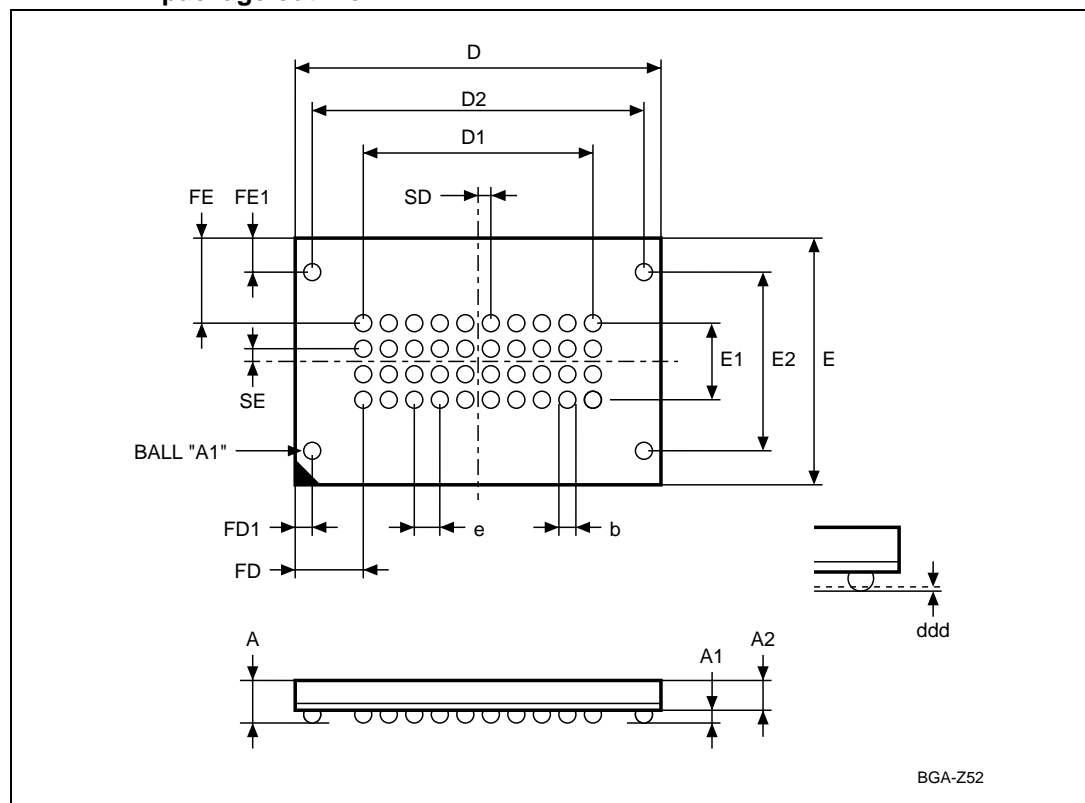
1.   Drawing is not to scale.

Table 2.   VFBGA44 7.5 × 5 mm, 10 × 4 ball array, 0.50mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.000			0.0394
A1		0.150			0.0059	
A2	0.660			0.0260		
b	0.300	0.250	0.350	0.0118	0.0098	0.0138
D	7.500	7.400	7.600	0.2953	0.2913	0.2992
D1	4.500			0.1772		
D2	6.500			0.2559		
ddd			0.080			0.0031
E	5.000	4.900	5.100	0.1969	0.1929	0.2008
E1	1.500			0.0591		
E2	3.500			0.1378		
e	0.500	–	–	0.0197	–	–
FD	1.500			0.0591		
FD1	0.500			0.0197		
FE	1.750			0.0689		
FE1	0.750			0.0295		
SD	0.250			0.0098		
SE	0.250			0.0098		

3 Part numbering

Table 3.   Ordering information scheme

Example: M58 W R 032 K U 70 ZA 6 E

Device Type

M58

Architecture

W = Multiple Bank, Burst Mode

Operating Voltage

R = V_{DD} = V_{DDQ} = 1.7 V to 2 V

Density

016 = 16 Mbit (×16)

032 = 32 Mbit (×16)

Technology

K = 65 nm technology

Parameter Location

U = Top Boot, Mux I/O

L = Bottom Boot, Mux I/O

Speed

60 = 60 ns

70 = 70 ns

Package

ZA = VFBGA44 7.5 x 5 mm, 0.50 mm pitch

Temperature Range

6 = –40 to 85 °C

Option

E = ECOPACK® Package, Standard Packing

U = ECOPACK® Package, Tape & Reel Packing, 16mm

Devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc.), Daisy chain ordering information, or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

4 Revision history

Table 4. Document revision history

Date	Revision	Changes
30-Jan-2007	1	Initial release.

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