

Hex Buffer

MC14049B, MC14050B

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage, V_{DD} .

The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS-to-TTL/DTL converter ($V_{DD} = 5.0\text{ V}$, $V_{OL} \leq 0.4\text{ V}$, $I_{OL} \geq 3.2\text{ mA}$).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

Features

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- V_{IN} can exceed V_{DD}
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

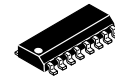
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient) per Pin	± 10	mA
I_{out}	Output Current (DC or Transient) per Pin	± 45	mA
P_D	Power Dissipation, per Package (Note 1) (Plastic) (SOIC)	825 740	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: See Figure 3.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18\text{ V}$ and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

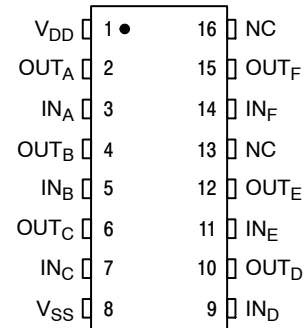


SOIC-16
D SUFFIX
CASE 751B

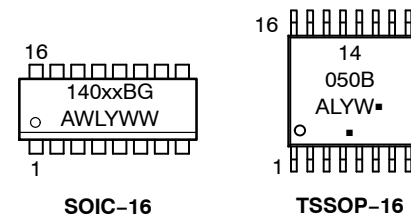


TSSOP-16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT



MARKING DIAGRAMS



xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Indicator

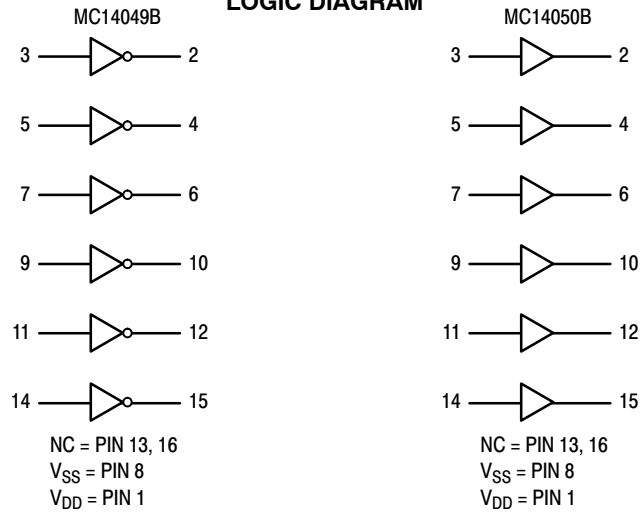
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14049B, MC14050B

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]
MC14049BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14049BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14049BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14050BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14050BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14050BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14050BDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC14049B, MC14050B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} V _{in} = 0	“0” Level V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
	“1” Level V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V _O = 4.5 Vdc) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc) (V _O = 0.5 Vdc) (V _O = 1.0 Vdc) (V _O = 1.5 Vdc)	“0” Level V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
	“1” Level V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source I _{OH}	5.0	–1.6	–	–1.25	–2.5	–	–1.0	–	mAdc
		10	–1.6	–	–1.30	–2.6	–	–1.0	–	
		15	–4.7	–	–3.75	–10	–	–3.0	–	
	Sink I _{OL}	5.0	3.75	–	3.2	6.0	–	2.6	–	mAdc
		10	10	–	8.0	16	–	6.6	–	
		15	30	–	24	40	–	19	–	
Input Current	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	10	20	–	–	pF
Quiescent Current (Per Package)	I _{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, per package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (1.8 μA/kHz) f + I _{DD} I _T = (3.5 μA/kHz) f + I _{DD} I _T = (5.3 μA/kHz) f + I _{DD}							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

3. The formulas given are for the typical characteristics only at +25°C

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

Where: I_T is in μA (per Package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency and k = 0.002.

MC14049B, MC14050B

AC SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = +25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time $t_{TLH} = (0.7 \text{ ns/pF}) C_L + 65 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$	t_{TLH}	5.0 10 15	– – –	100 50 40	160 80 60	ns
Output Fall Time $t_{THL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{THL} = (0.06 \text{ ns/pF}) C_L + 17 \text{ ns}$ $t_{THL} = (0.04 \text{ ns/pF}) C_L + 13 \text{ ns}$	t_{THL}	5.0 10 15	– – –	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.33 \text{ ns/pF}) C_L + 63.5 \text{ ns}$ $t_{PLH} = (0.19 \text{ ns/pF}) C_L + 30.5 \text{ ns}$ $t_{PLH} = (0.06 \text{ ns/pF}) C_L + 27 \text{ ns}$	t_{PLH}	5.0 10 15	– – –	80 40 30	140 80 60	ns
Propagation Delay Time $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{PHL} = (0.05 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{PHL}	5.0 10 15	– – –	40 20 15	80 40 30	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

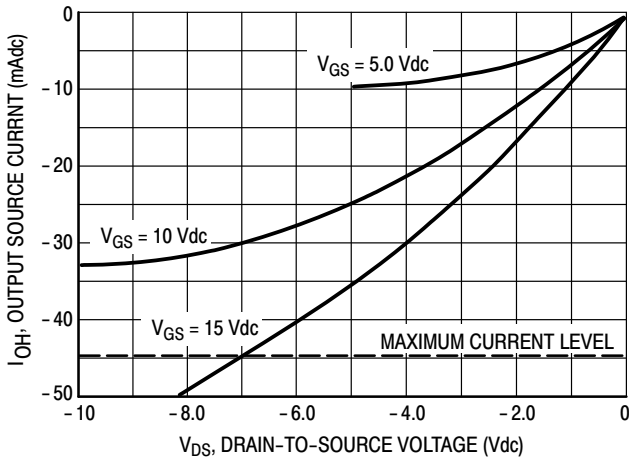
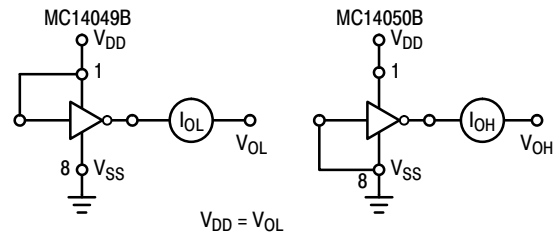
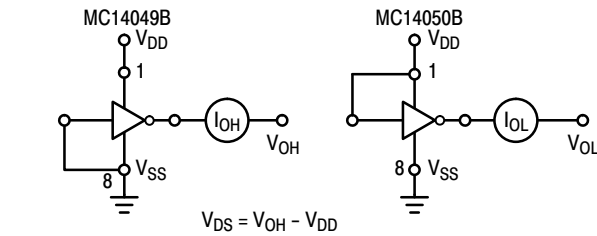


Figure 1. Typical Output Source Characteristics

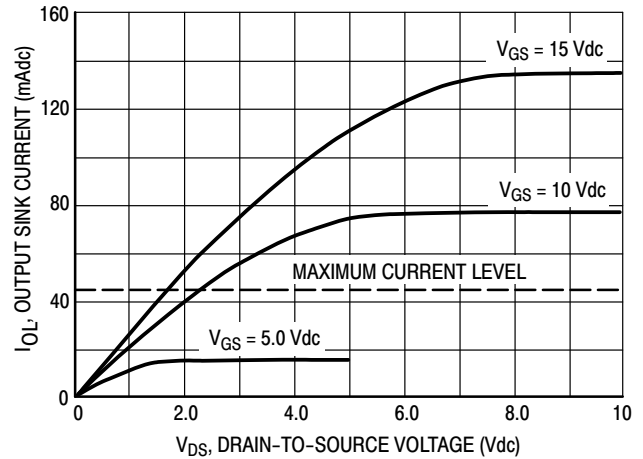


Figure 2. Typical Output Sink Characteristics

MC14049B, MC14050B

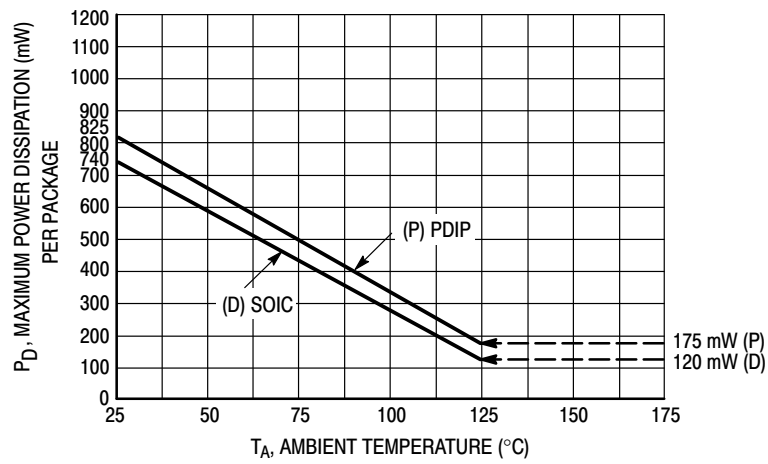


Figure 3. Ambient Temperature Power Derating

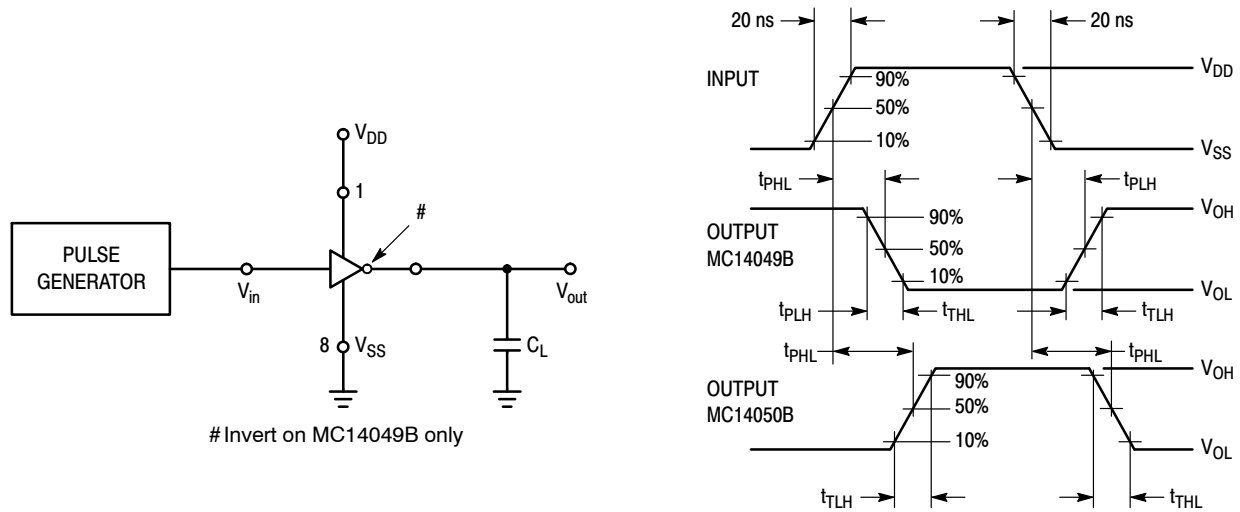
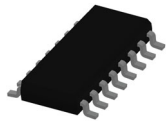


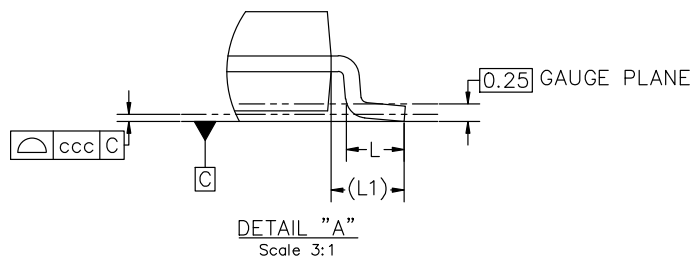
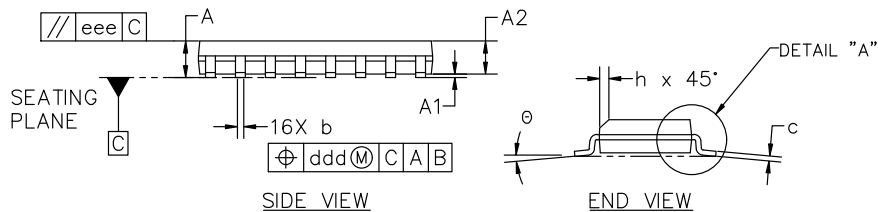
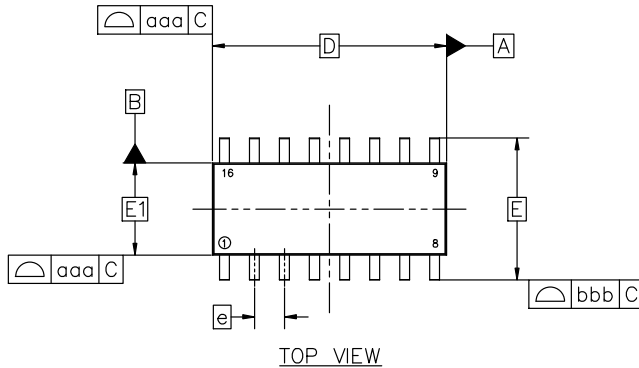
Figure 4. Switching Time Test Circuit and Waveforms


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

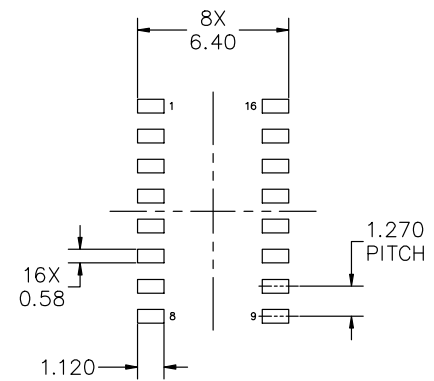
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

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AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERM/D

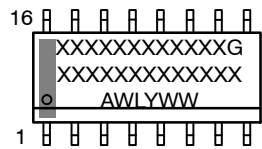
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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC
MARKING DIAGRAM*

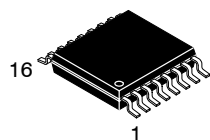


XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

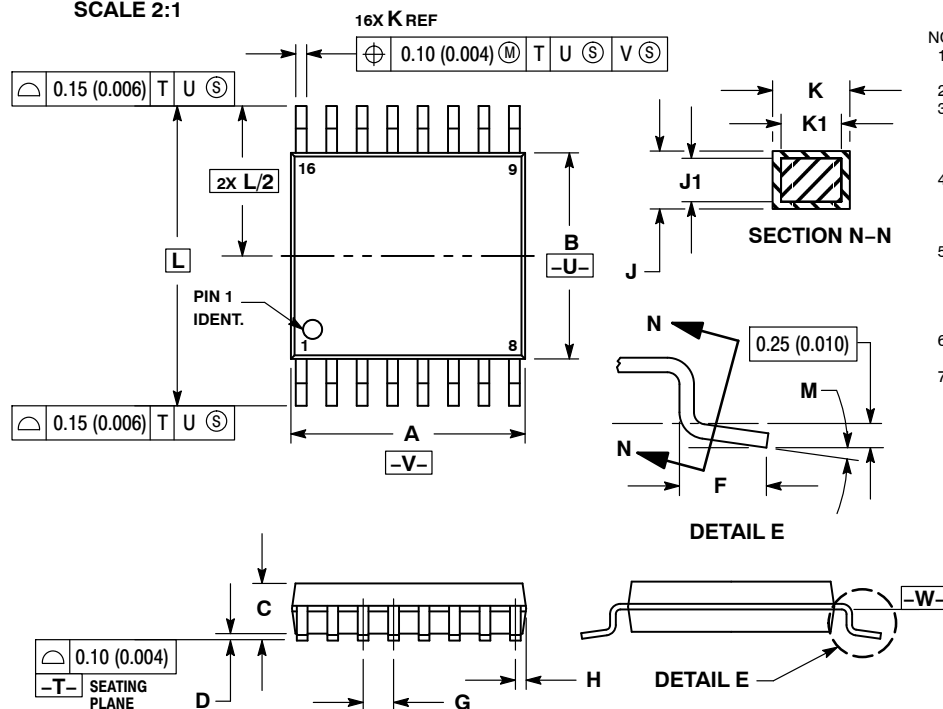
STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

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TSSOP-16 WB
CASE 948F
ISSUE B

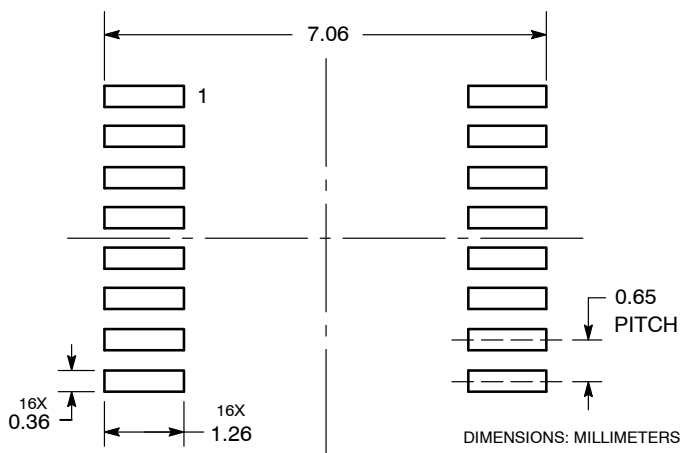
DATE 19 OCT 2006



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

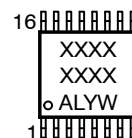
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual. SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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